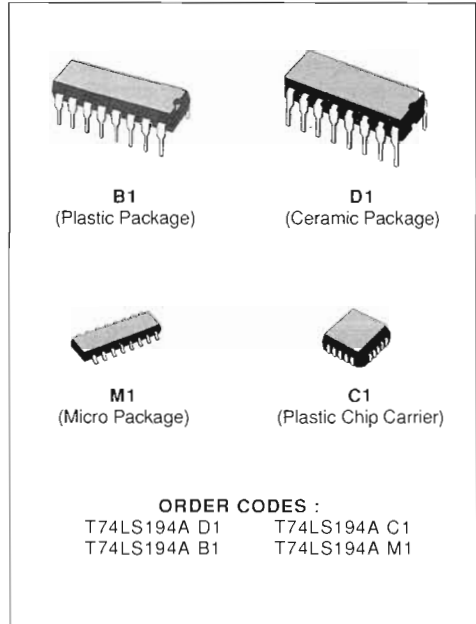
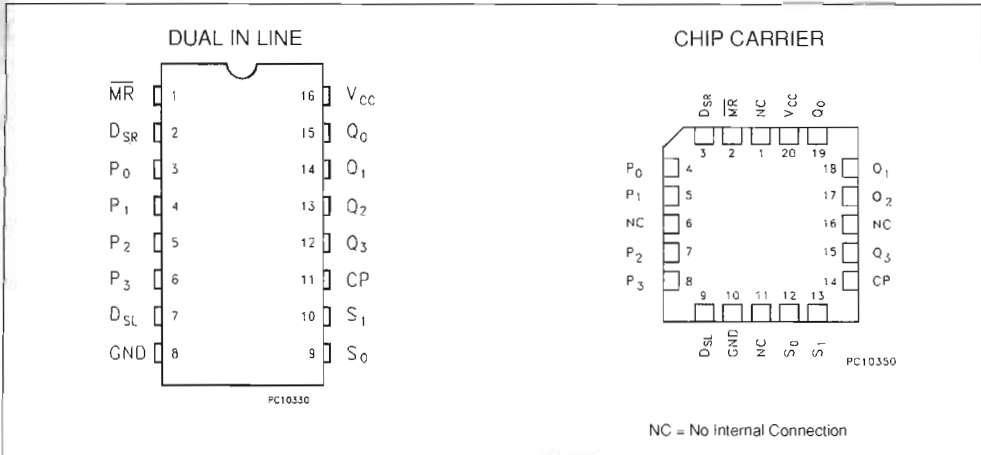


UNIVERSAL 4-BIT SHIFT REGISTER

- TYPICAL SHIFT REGISTER FREQUENCY OF 40 MHz
- ASYNCHRONOUS MASTER RESET
- HOLD (DO NOTHING) MODE
- FULLY SYNCHRONOUS SERIAL OR PARALLEL DATA TRANSFERS
- INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS
- FULLY TTL AND CMOS COMPATIBLE

DESCRIPTION

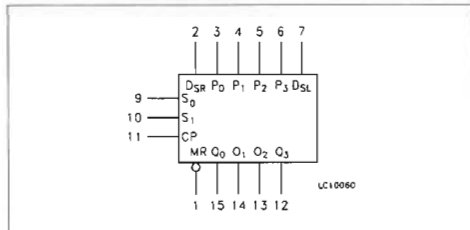
The T74LS194A is a High Speed Bidirectional Universal Shift Register. As a high speed multifunctional sequential building block, it is useful in a wide variety of applications. It may be used in serial-serial, shift left, shift right, serial-parallel, parallel-serial and parallel-parallel data register transfers. The LS194A is similar in operation to be LS195 Universal Shift Register, with added features of shift left without external connections and hold (do nothing) modes of operation. It utilizes the Schottky diode clamped process to achieve high speed and is fully compatible with all TTL families.


PIN CONNECTION (top view)


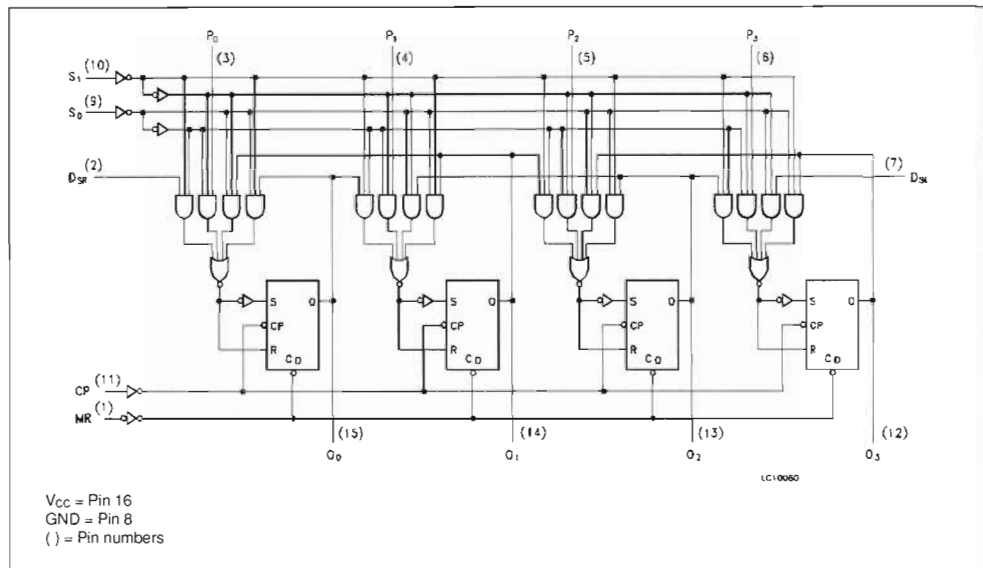
PIN NAMES

S ₀ -S ₃	Mode Control to Input
P ₀ -P ₃	Parallel Data Inputs
D _{SR}	Serial (Shift Right) Data Input
D _{SL}	Serial (Shift Left) Data Input
CP	Clock (Active HIGH Going Edge) Input
MR	Master Reset (Active LOW) Input
Q ₀ -Q ₃	Parallel Outputs

LOGIC SYMBOL



LOGIC DIAGRAM



TRUTH TABLE

OPERATING MODE	INPUTS						OUTPUTS			
	MR	S _r	S ₀	D _{SR}	D _{SL}	P _n	Q ₀	Q ₁	Q ₂	Q ₃
Reset	L	X	X	X	X	X	L	L	L	L
Hold	H	l	l	X	X	X	q ₀	q ₁	q ₂	q ₃
Shift Left	H	h	l	X	l	X	q ₁	q ₂	q ₃	q ₃
	H	h	l	X	h	X	q ₁	q ₂	q ₃	H
Shift Right	H	l	h	l	X	X	L	q ₀	q ₁	q ₂
	H	l	h	h	X	X	H	q ₀	q ₁	q ₂
Paralled Load	H	h	h	X	X	P _n	P ₀	P ₁	P ₂	P ₃

L = LOW Voltage Level
 H = HIGH Voltage Level
 X = Don't Care
 l = LOW voltage level one set-up time prior to the LOW to HIGH clock transition
 h = HIGH voltage level one set-up time prior to the LOW to HIGH clock transition
 Pn (qn) = Lower case letters indicate the state of the referenced input (or output) one set-up time prior to the LOW to HIGH clock transition.

FUNCTIONAL DESCRIPTION

The Logic Diagram and Truth Table indicate the functional characteristics of the LS194A 4-Bit Bidirectional Shift Register. The LS194A is similar in operation to the LS195A Universal Shift Register when used in serial or parallel data register transfers. Some of the common features of the two devices are described below:

- 1) All data and mode control inputs are edge-triggered, responding only to the LOW to HIGH transition of the clock (CP). The only timing restriction, therefore, is that the mode control and selected data inputs must be stable one set-up time prior to the positive transition of the clock pulse.
- 2) The register is fully synchronous, with all operations taking place in less than 15 ns (typical) making the device especially useful for implementing very high speed CPUs, or the memory buffer registers.
- 3) The four parallel data inputs (P₀, P₁, P₂, P₃) are D-type inputs. When both S₀ and S₁ are HIGH, the data appearing on P₀, P₁, P₂ and P₃ inputs is transferred to the Q₀, Q₁, Q₂ and Q₃ outputs respectively following the next

LOW to HIGH transition of the clock.

- 4) The asynchronous Master Reset (\overline{MR}), when LOW, overrides all other input conditions and forces the Q outputs LOW.

Special logic features of the LS194A design which increase the range of application are described below:

- 1) Two mode control inputs (S₀, S₁) determine the synchronous operation of the devices. As shown in the Mode Selection Table, data can be entered and shifted from left to right (shift right, Q₀ -> Q₁, etc.) or right to left (shift left, Q₃ -> Q₂, etc.), or parallel data can be entered loading all four bits of the register simultaneously. When both S₀ and S₁ are LOW, the existing data is retained in a "do nothing" mode without restricting the HIGH to LOW clock transition.
- 2) D-type serial data inputs (D_{SR}, D_{SL}) are provided on both the first and last stages to allow multistage shift right or shift left data transfers without interfering with parallel load operation.

ABSOLUTE MAXIMUM RATING

Symbol	Parameter	Value	Unit
V _{CC}	Supply Voltage	- 0.5 to 7	V
V _I	Input Voltage, Applied to Input	- 0.5 to 15	V
V _O	Output Voltage, Applied to Output	- 0.5 to 10	V
I _I	Input Current, Into Inputs	- 30 to 5	mA
I _O	Output Current, Into Outputs	50	mA

Stresses in excess of those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions in excess of those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

GUARANTEED OPERATING RANGE

Part Numbers	Supply Voltage			Temperature
	Min.	Typ.	Max.	
T74LS194AXX	4.75 V	5.0 V	5.25 V	0 °C to + 70 °C

XX = package type.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

Symbol	Parameter	Limits			Test Condition (note 1)	Unit	
		Min.	Typ. (*)	Max.			
V _{IH}	Input HIGH Voltage	2.0			Guaranteed Input HIGH Voltage for All Input	V	
V _{IL}	Input LOW Voltage			0.8	Guaranteed Input LOW Voltage for All Input	V	
V _{CD}	Input Clamp Diode Voltage		- 0.65	- 1.5	V _{CC} = MIN, I _{IN} = -18 mA	V	
V _{OH}	Output HIGH Voltage	2.7	3.4		V _{CC} = MIN, I _{OH} = - 400 μ A V _{IN} = V _{IH} or V _{IL} per Truth Table	V	
V _{OL}	Output LOW Voltage		0.25	0.4	I _{OL} = 4.0 mA	V _{CC} = MIN V _{IN} = V _{IH} or V _{IL} per Truth Table	V
			0.35	0.5	I _{OL} = 8.0 mA		V
I _{IH}	Input HIGH Current			20 0.1	V _{CC} = MAX, V _{IN} = 2.7 V V _{CC} = MAX, V _{IN} = 7.0 V	μ A mA	
I _{IL}	Input LOW Current			- 0.4	V _{CC} = MAX, V _{IN} = 0.4 V	mA	
I _{OS}	Output Short Circuit Current (note 2)	- 20		- 100	V _{CC} = MAX, V _{OUT} = 0 V	mA	
I _{CC}	Power Supply Current		15	23	V _{CC} = MAX	mA	

Notes : 1. Conditions for testing, not shown in the Table, are chosen to guarantee operation under "worst case" conditions
 2. Not more than one output should be shorted at a time.
 (*) Typical values are at V_{CC} = 5.0 V, T_A = 25 °C.

AC CHARACTERISTICS: T_A = 25 °C

Symbol	Parameter	Limits			Test Conditions	Units
		Min.	Typ.	Max.		
f _{MAX}	Shift Frequency	25	36		Figures 1	MHz
t _{PLH}	Propagation Delay, Clock to Outputs		14	22	Figures 1	V _{CC} = 5.0 V C _L = 15 pF
t _{PHL}			17	26		
t _{PHL}	Propagation Delay, MR to Outputs		19	30	Figures 2	

AC SET-UP REQUIREMENTS: T_A = 25 °C

Symbol	Parameter	Limits			Test Conditions	Units
		Min.	Typ.	Max.		
t _w (CP)	Clock Pulse Width	20			Figure 1	ns
t _s (Data)	Set-Up Time Data to Clock	20			Figure 3	ns
t _h (Data)	Hold Time Data to Clock	0			Figure 4	ns
t _s (S)	Set-Up Time Mode Control to Clock	30				ns
t _h (S)	Hold Time Mode Control to Clock	0				ns
t _w (MR)	Master Reset Pulse Width	20			Figure 2	ns
t _{rec} (MR)	Recovery Time Master Reset to Clock	25				ns

DEFINITION OF TERMS:

SET-UP TIME (t_s): is defined as the minimum time required for the correct logic level to be present at the logic input prior to the clock transition from LOW to HIGH in order to be recognized and transferred to the outputs.

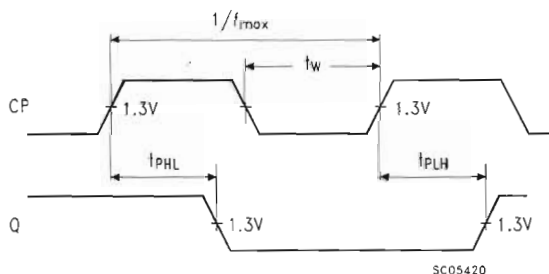
HOLD TIME (t_h): is defined as the minimum time following the clock transition from LOW to HIGH at which the logic level must be maintained at the input

in order to ensure continued recognition. A negative **HOLD TIME** indicates that the correct logic level may be relaxed prior to the clock transition from LOW to HIGH and still be recognized.

RECOVERY TIME (t_{rec}): is defined as the minimum time required between the end of the reset pulse and the clock transition from LOW to HIGH in order to recognize and transfer HIGH Data to the Q outputs.

AC WAVEFORMS

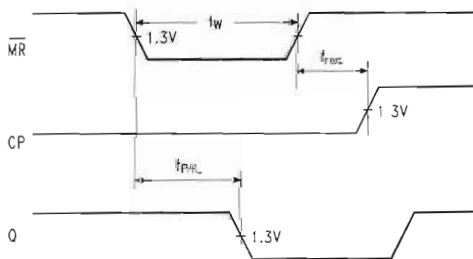
Figure 1: Clock to Output Delays Clock Pulse Width and f_{max}



SC05420

Other Conditions: $S_1 = L$, $\overline{MR} = H$, $S_0 = \overline{K}$

Figure 2: Master Reset Pulse Width, Master Reset to Output Delay and Master Reset to Clock Recovery Time



SC05410

Other Conditions: $S_0, S_1 = H$, $P_0 = P_1 = P_2 = P_3 = H$

The shaded areas indicate when the input is permitted to change for predictable output performance.

Figure 3: Set-up (t_s) and Hold (t_h) Time for Serial Data (D_{SR} , D_{SL}) and Parallel Data (P_0 , P_1 , P_2 , P_3)

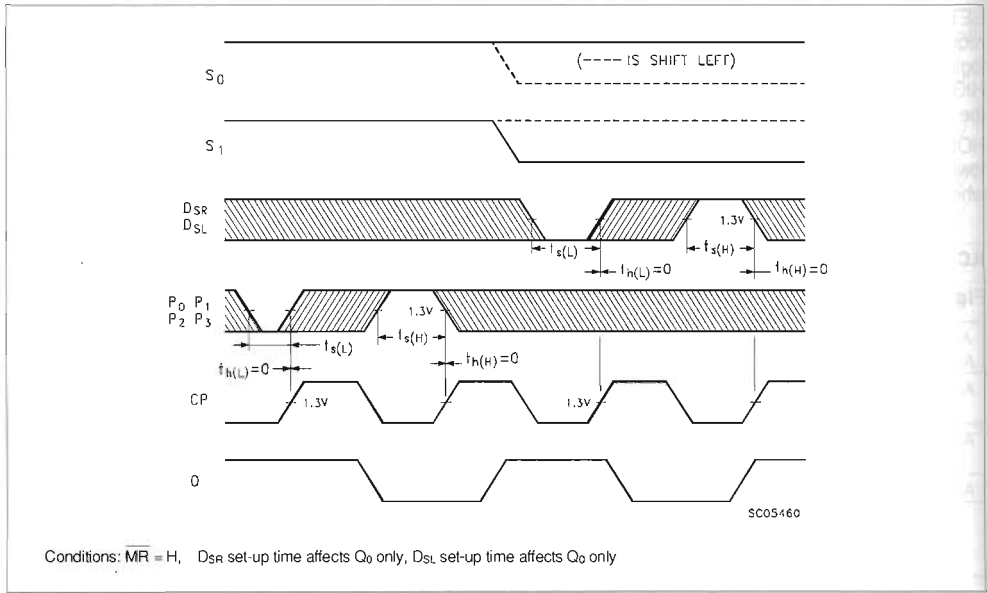
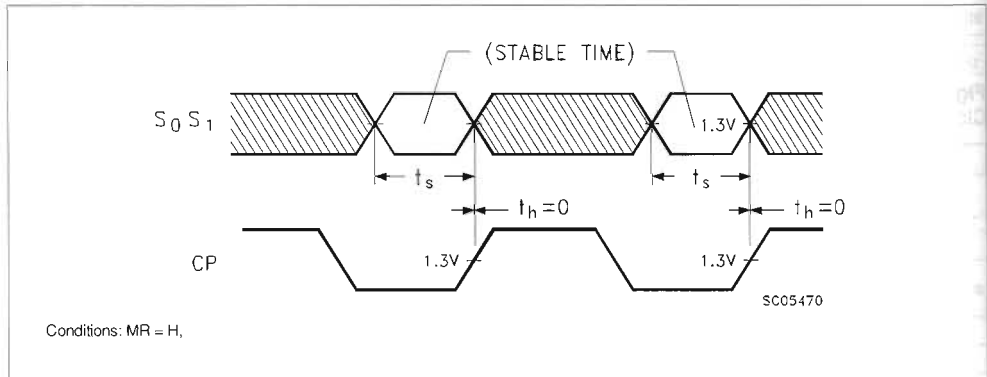


Figure 4: Set-up (t_s) and Hold (t_h) Time for S Input



The shaded areas indicate when the input is permitted to change for predictable output performance.