

## CMOS 0 to 33 MHz Programmable 8-bit Microcontroller

### Description

TEMIC's TSC87C52 is high performance CMOS EPROM version of the 80C52 CMOS single chip 8 bit microcontroller.

The fully static design of the TSC87C52 allows to reduce system power consumption by bringing the clock frequency down to any value, even DC, without loss of data.

The TSC87C52 retains all the features of the 80C52 with some enhancement: 8 K bytes of internal code memory (EPROM); 256 bytes of internal data memory (RAM); 32 I/O lines; three 16 bit timers one with count-down and clock-out capability; a 6-source, 2-level interrupt

structure; a full duplex serial port with framing error detection; a power off flag; and an on-chip oscillator.

The TSC87C52 has 2 software-selectable modes of reduced activity for further reduction in power consumption. In the idle mode the CPU is frozen while the RAM, the timers, the serial port and the interrupt system continue to function. In the power down mode the RAM is saved and all other functions are inoperative.

The TSC87C52 is manufactured using non volatile SCMOS process which allows it to run up to:

- 33 MHz with  $VCC = 5 V \pm 10\%$ .
- 16 MHz with  $2.7 V < VCC < 5.5 V$ .

### Features

- 8 Kbytes of EPROM
  - Improved Quick Pulse programming algorithm
  - Secret ROM by encryption
- 256 bytes of RAM
- 64 Kbytes program memory space
- 64 Kbytes data memory space
- 32 programmable I/O lines
- Three 16 bit timer/counters including enhanced timer 2
- Programmable serial port with framing error detection
- Power control modes
- Two-level interrupt priority
- Fully static design
- 0.8 $\mu$  SCMOS non volatile process
- ONCE Mode
- Enhanced Hooks system for emulation purpose
- Available temperature ranges:
  - commercial
  - industrial
- Available packages:
  - PDIP40 (OTP)
  - PLCC44 (OTP)
  - PQFP44 (OTP)
  - CQPJ44 (UV erasable)
  - CERDIP40 (UV erasable)

## Block Diagram

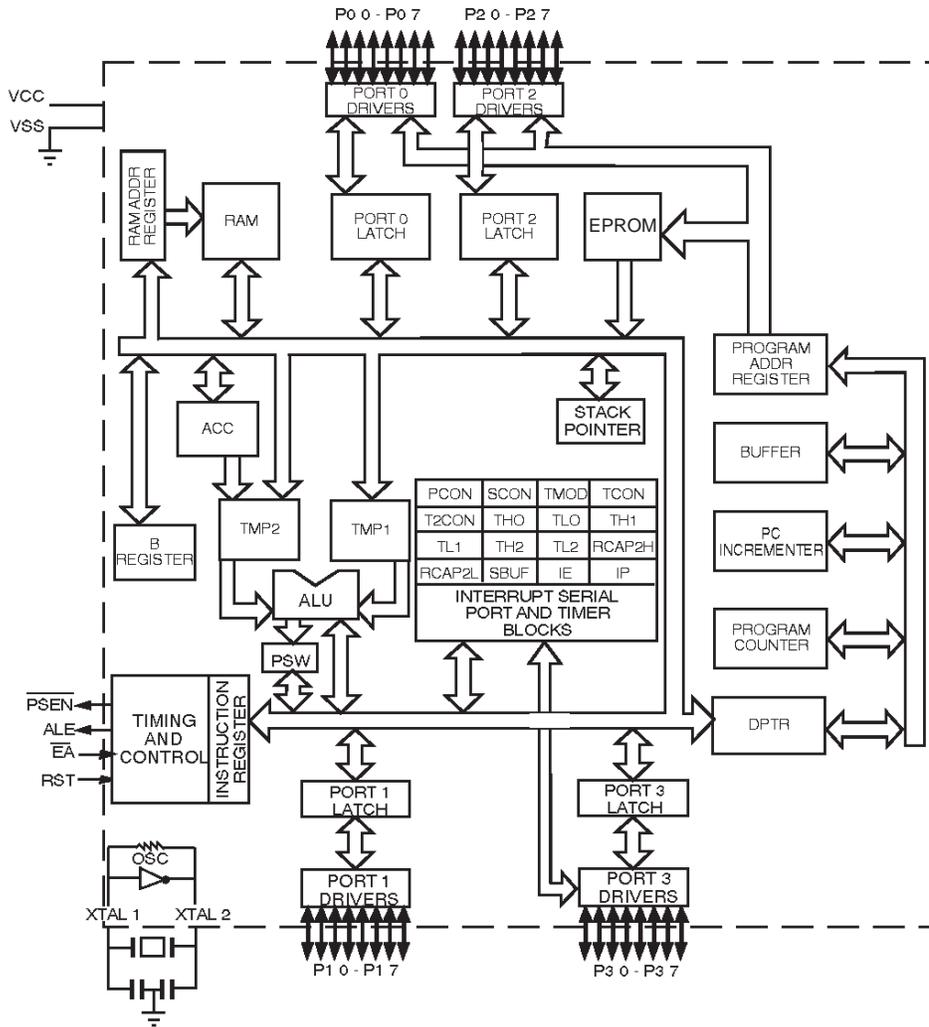


Figure 1 TSC87C52 Block diagram



## Pin Description

### VSS

Circuit ground potential.

### VSS1

Secondary ground (not on DIP). Provided to reduce ground bounce and improve power supply by-passing.

Note: This pin is not a substitute for the VSS pin. Connection is not necessary for proper operation.

### VCC

Supply voltage during normal, Idle, and Power Down operation.

### Port 0

Port 0 is an 8 bit open drain bi-directional I/O port. Port 0 pins that have 1's written to them float, and in that state can be used as high-impedance inputs.

Port 0 is also the multiplexed low-order address and data bus during accesses to external Program and Data Memory. In this application it uses strong internal pullups when emitting 1's.

Port 0 can sink eight LS TTL inputs.

Port 0 is used as data bus during EPROM programming and program verification.

### Port 1

Port 1 is an 8 bit bi-directional I/O port with internal pullups. Port 1 pins that have 1's written to them are pulled high by the internal pullups, and in that state can be used as inputs. As inputs, Port 1 pins that are externally being pulled low will source current (IIL, in the DC parameters section) because of the internal pullups.

Port 1 can sink/ source three LS TTL inputs. It can drive CMOS inputs without external pullups.

Port1 also serves the functions of the following special features of the TSC87C52 as listed below:

Port Pin	Alternate Function
P1.0	T2 (External Count input to Timer/Counter 2), Clock-Out
P1.1	T2EX (Timer/Counter 2 Capture/Reload Trigger and direction Control)

Port 1 receives the low-order address byte during EPROM programming and program verification.

### Port 2

Port 2 is an 8 bit bi-directional I/O port with internal pullups. Port 2 pins that have 1's written to them are pulled high by the internal pullups, and in that state can be used as inputs. As inputs, Port 2 pins that are externally being pulled low will source current (IIL, in the DC parameters section) because of the internal pullups.

Port 2 emits the high-order address byte during fetches from external Program Memory and during accesses to external Data Memory that use 16 bit addresses (MOVX @DPTR). In this application, it uses strong internal pullups when emitting 1's. During accesses to external Data Memory that use 8 bit addresses (MOVX @Ri), Port 2 emits the contents of the P2 Special Function Register.

Port 2 can sink/source three LS TTL inputs. It can drive CMOS inputs without external pullups.

Some Port 2 pins receive the high-order address bits and control signals during EPROM programming and program verification.

### Port 3

Port 3 is an 8 bit bi-directional I/O port with internal pullups. Port 3 pins that have 1's written to them are pulled high by the internal pullups, and in that state can be used as inputs. As inputs, Port 3 pins that are externally being pulled low will source current (IIL, in the DC parameters section) because of the pullups.

Port 3 also serves the functions of various special features of the TEMIC's C51 Family, as listed below:

Port Pin	Alternate Function
P3.0	RxD (serial input port)
P3.1	TxD (serial output port)
P3.2	$\overline{\text{INT0}}$ (external interrupt 0)
P3.3	$\overline{\text{INT1}}$ (external interrupt 1)
P3.4	T0 (Timer 0 external input)
P3.5	T1 (Timer 1 external input)
P3.6	$\overline{\text{WR}}$ (external Data Memory write strobe)
P3.7	$\overline{\text{RD}}$ (external Data Memory read strobe)

Port 3 can sink/source three LS TTL inputs. It can drive CMOS inputs without external pullups. Some Port 3 pins receive control signals during EPROM programming and program verification.

## RST

A high level on this pin for two machine cycles while the oscillator is running resets the device. An internal pull-down resistor permits Power-On reset using only a capacitor connected to  $V_{CC}$ . The port pins will be driven to their reset condition when a minimum  $V_{IH1}$  voltage is applied whether the oscillator is started or not (asynchronous reset).

## ALE/ $\overline{\text{PROG}}$

Address Latch Enable output for latching the low byte of the address during accesses to external memory. ALE is activated as though for this purpose at a constant rate of 1/6 the oscillator frequency except during an external data memory access at which time one ALE pulse is skipped.

ALE can sink/source 8 LS TTL inputs. It can drive CMOS inputs without external pullup.

If desired, to reduce EMI, ALE operation can be disabled by setting bit 0 of SFR location 8Eh (MSCON). With this bit set, the pin is weakly pulled high. However, ALE remains active during MOVX, MOVC instructions and external fetches. Setting the ALE disable bit has no effect if the microcontroller is in external execution mode ( $\overline{\text{EA}}=0$ ).

Throughout the remainder of this datasheet, ALE will refer to the signal coming out of the ALE/ $\overline{\text{PROG}}$  pin, and the pin will be referred to as the ALE/ $\overline{\text{PROG}}$  pin.

## $\overline{\text{PSEN}}$

Program Store Enable output is the read strobe to external Program Memory.  $\overline{\text{PSEN}}$  is activated twice each machine cycle during fetches from external Program Memory. (However, when executing out of external Program Memory, two activations of  $\overline{\text{PSEN}}$  are skipped during each access to external Data Memory).  $\overline{\text{PSEN}}$  is not activated during fetches from internal Program Memory.  $\overline{\text{PSEN}}$  can sink/source 8 LS TTL inputs. It can drive CMOS inputs without an external pullup.

## $\overline{\text{EA}}/\text{VPP}$

External Access enable.  $\overline{\text{EA}}$  must be strapped to VSS in order to enable the device to fetch code from external Program Memory locations 0000h to FFFFh. Note however, that if any of the Security bits are programmed,  $\overline{\text{EA}}$  will be internally latched on reset.

$\overline{\text{EA}}$  should be strapped to VCC for internal program execution.

This pin also receives the programming supply voltage (VPP) during EPROM programming.

## XTAL1

Input to the inverting amplifier that forms the oscillator. Receives the external oscillator signal when an external oscillator is used.

## XTAL2

Output from the inverting amplifier that forms the oscillator. This pin should be floated when an external oscillator is used.

## New and Enhanced Features

In comparison to the original 80C52, the TSC87C52 implements some new and enhanced features. The new features are the Power Off Flag, the ONCE mode and the ALE disabling. The enhanced features are located in the UART and the Timer 2.

### Power Off Flag

The Power Off Flag allows the user to distinguish between a ‘cold start’ reset and a ‘warm start’ reset.

A cold start reset is one that is coincident with VCC being turned on to the device after it was turned off. A warm start reset occurs while VCC is still applied to the device and could be generated for example by an exit from Power Down.

The Power Off Flag (POF) is located in PCON at bit location 4 (see Table 1). POF is set by hardware when VCC rises from 0 to its nominal voltage. The POF can be set or cleared by software allowing the user to determine the type of reset.

**Table 1 PCON – Power Control Register (87h)**

7	6	5	4	3	2	1	0
SMOD1	SMOD0	–	POF	GF1	GF0	PD	IDL

Symbol	Description
SMOD1	<b>Serial Port Mode bit 1, new name of SMOD bit</b> Set to select double baud rate in mode 1,2 or 3.
SMOD0	<b>Serial Port Mode bit 0</b> Set to select FE bit in SCON. Clear to select SM0 bit in SCON.
–	<b>Reserved</b> Do not write 1 in this bit.
POF	<b>Power Off Flag</b> Set by hardware when VCC rises from 0 to its nominal voltage. Can also be set by software. Clear by software to recognize next reset type.
GF1	<b>General purpose Flag</b> Set by software for general purpose usage. Clear by software for general purpose usage.
GF0	<b>General purpose Flag</b> Set by software for general purpose usage. Clear by software for general purpose usage.
PD	<b>Power Down mode bit</b> Set to enter power down mode. Clear by hardware when reset occurs.
IDL	<b>Idle mode bit</b> Set to enter idle mode. Clear by hardware when interrupt or reset occur.

The reset value of PCON is 00XX 0000b.

### ONCE Mode

The ONCE mode facilitates testing and debugging of systems using TSC87C52 without the TSC87C52 having to be removed from the circuit. The ONCE mode is invoked by driving certain pins of the TSC87C52, the following sequence must be exercised.

- Pull ALE low while the device is in reset (RST high) and  $\overline{\text{PSEN}}$  is high.
- Hold ALE low as RST is deactivated.

While the TSC87C52 is in ONCE mode, an emulator or test CPU can be used to drive the circuit. Table 2 shows the status of the port pins during ONCE mode.

Normal operation is restored when normal reset is applied.

**Table 2 External pin status during ONCE mode**

ALE	$\overline{\text{PSEN}}$	Port 0	Port 1	Port 2	Port 3	XTAL1/2
Weak pull-up	Weak pull-up	Float	Weak pull-up	Weak pull-up	Weak pull-up	Active

## ALE Disabling

The ALE signal is used to demultiplex address and data buses on port 0 when used with external program or data memory. Nevertheless, during internal code execution, ALE signal is still generated. In order to reduce EMI, ALE signal should be disabled by setting AO bit.

The AO bit is located in MCON at bit location 0 (see Table 3). As soon as AO is set, ALE is no longer output but remains active during MOVX and MOVC instructions and external fetches. During ALE disabling, ALE pin is weakly pulled high.

**Table 3 MCON – Miscellaneous Control Register (8Eh)**

7	6	5	4	3	2	1	0
–	–	–	–	–	–	–	AO

Symbol	Description
–	<b>Reserved</b> Do not write 1 in these bits.
AO	<b>ALE Output bit</b> Set to disable ALE operation during internal fetches. Clear to restore ALE operation during internal fetches.

The reset value of MCON is XXXX XXX0b.

## UART

The UART in the TSC87C52 operates identically to the UART in the 80C51 but includes the following enhancement. For a complete understanding of the TSC87C52 UART please refer to the description in the 80C51 Hardware Description Guide.

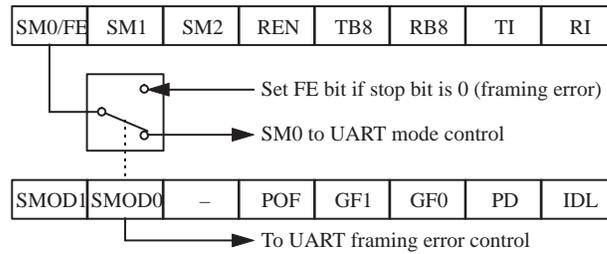
### Framing Error Detection

Framing error detection allows the serial port to check for missing stop bits in the communication in mode 1, 2 or 3. A missing stop bit can be caused for example by noise on the serial lines or transmission by two CPUs simultaneously.

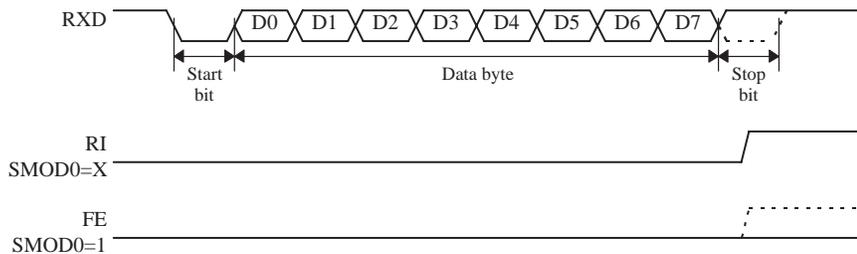
If a stop bit is missing a Framing Error bit (FE) is set. The FE bit can be checked in software after each reception to detect communication errors. Once set, the FE bit must be cleared in software. A valid stop bit will not clear FE.

The FE bit is located in SCON at bit location 7. It shares the same bit location as SM0 (see Table 4). The new control bit SMOD0 in PCON (see Table 1) determines whether the SM0 or FE bit is accessed (see Figure 3), so whether the framing error detection is enabled or not. If SMOD0 is set then SCON.7 functions as FE, if SMOD0 is cleared then SCON.7 functions as SM0. Once set, the FE bit must be cleared by software. A valid stop bit will not clear FE. When UART is in mode 1 (8-bit mode), RI flag is set during stop bit whether or not framing error is enabled (see Figure 4).

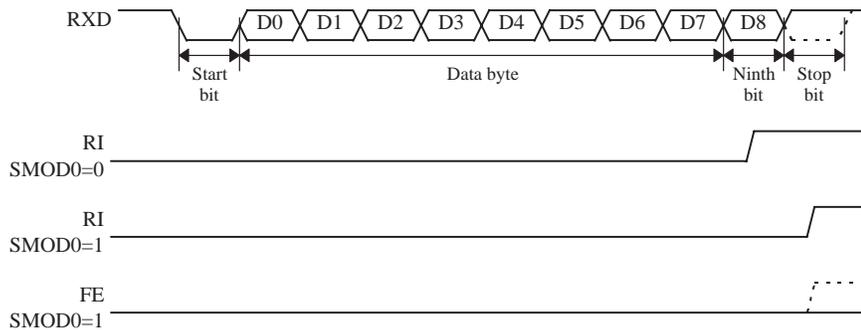
When in mode 2 and 3 (9-bit mode), RI flag is set during stop bit if framing error is enabled or during ninth bit if not (see Figure 5).



**Figure 3 Framing error block diagram**



**Figure 4 Enhanced UART timing diagram in mode 1**



**Figure 5 Enhanced UART timing diagram in mode 2 and 3**

**Table 4 SCON – Serial Control Register (98h)**

7	6	5	4	3	2	1	0
SM0/FE	SM1	SM2	REN	TB8	RB8	TI	RI

Symbol	Description
FE	<b>Framing Error bit (SMOD0 bit set)</b> Set by hardware when an invalid stop bit is detected. Clear to reset the error state, not cleared by a valid stop bit.
SM0	<b>Serial Mode bit 0 (SMOD0 bit cleared)</b> Used with SM1 to select serial mode.
SM1	<b>Serial Mode bit 1</b> Used with SM0 to select serial mode.
SM2	<b>Multiprocessor Communication Enable bit</b> Set to enable multiprocessor communication feature in mode 2 and 3. Clear to disable multiprocessor communication feature.

Symbol	Description
REN	<b>Serial Reception Enable bit</b> Set to enable serial reception. Clear to disable serial reception.
TB8	<b>Ninth bit to transmit in mode 2 and 3</b> Set to transmit a logic 1 in the 9th bit. Clear to transmit a logic 0 in the 9th bit.
RB8	<b>Ninth bit received in mode 2 and 3</b> Set by hardware if 9th bit received is logic 1. Clear by hardware if 9th bit received is logic 0.
TI	<b>Transmit Interrupt Flag</b> Set by hardware at the end of the 8th bit time in mode 0 or at the beginning of the stop bit in the other modes. Clear to acknowledge interrupt.
RI	<b>Receive Interrupt Flag</b> Set by hardware at the end of the 8th bit time in mode 0, see Figure 4 and Figure 5 in the other modes. Clear to acknowledge interrupt.

The reset value of SCON is 0000 0000b.

## Timer 2

The Timer 2 in the TSC87C52 operates identically to the Timer 2 in the 80C52 but includes the following enhancements. For a complete understanding of the TSC87C52 Timer 2 please refer to the description in the 80C51 Hardware Description Guide.

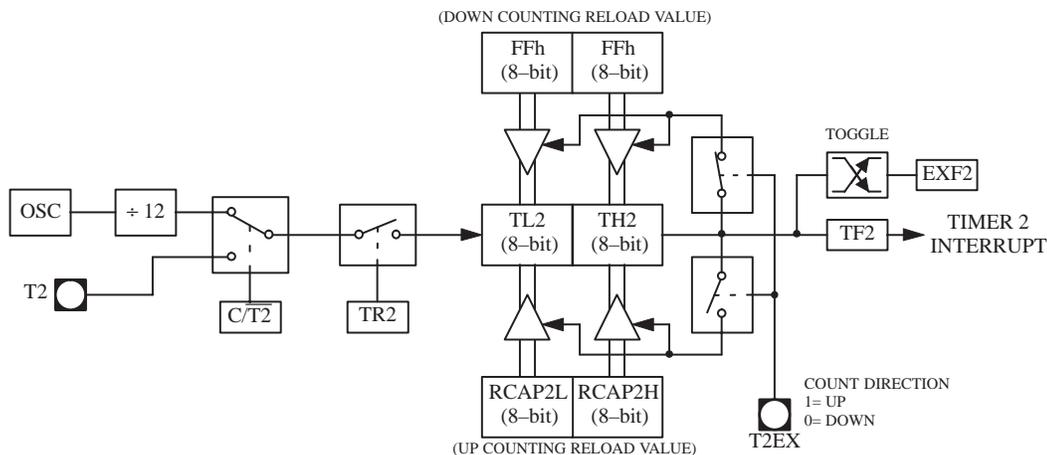
### Auto-reload (up or down counter)

Enhanced Timer 2 can now be programmed to count up or down when configured in its 16-bit auto-reload mode. This feature is controlled by the DCEN (Down Counter Enable) bit. DCEN is located in T2MOD at bit location 0 (see Table 5). Setting the DCEN bit enables Timer 2 to count up or down as shown in Figure 6. In this mode the T2EX pin controls the direction of count.

A logic 1 at T2EX makes Timer 2 count up. The timer will overflow at FFFFh and set the TF2 bit. This overflow also causes the 16-bit value in RCAP2H and RCAP2L to be reloaded into the timer registers, TH2 and TL2, respectively.

A logic 0 at T2EX makes Timer 2 count down. Now the timer underflows when TH2 and TL2 equal the values stored in RCAP2H and RCAP2L. The underflow sets the TF2 bit and causes FFFFh to be reloaded into the timer registers.

The EXF2 bit toggles whenever Timer 2 overflows or underflows. In this operating mode, EXF2 does not flag an interrupt.



**Figure 6 Timer 2 Auto-Reload Mode Up/Down Counter**



## EPROM

### EPROM Structure

The TSC87C52 EPROM is divided in two different arrays:

- the code array: 8 Kbytes.
- the encryption array: 64 bytes.

In addition a third non programmable array is implemented:

- the signature array: 4 bytes.

### EPROM Lock System

The program Lock system, when programmed, protects the on-chip program against software piracy.

### Encryption Array

Within the EPROM array are 64 bytes of encryption array that are initially unprogrammed (all 1's). Every time a byte is addressed during program verify, 6 address lines are used to select a byte of the encryption array. This byte is then exclusive-NOR'ed (XNOR) with the code byte, creating an encryption verify byte. The algorithm, with the encryption array in the unprogrammed state, will return the code in its original, unmodified form.

When using the encryption array, one important factor needs to be considered. If a byte has the value FFh, verifying the byte will produce the encryption byte value. If a large block (>64 bytes) of code left unprogrammed, a verification routine will display the content of the encryption array. For this reason all the unused code bytes should be programmed with random values. This will ensure program protection.

### EPROM Programming

#### Set-up modes

In order to program and verify the EPROM or to read the signature bytes, the TSC87C52 is placed in specific set-up modes (see Figure 8).

Control and program signals must be held at the levels indicated in Table 6.

#### Definition of terms

**Address Lines:** P1.0–P1.7, P2.0–P2.4 respectively for A0–A12

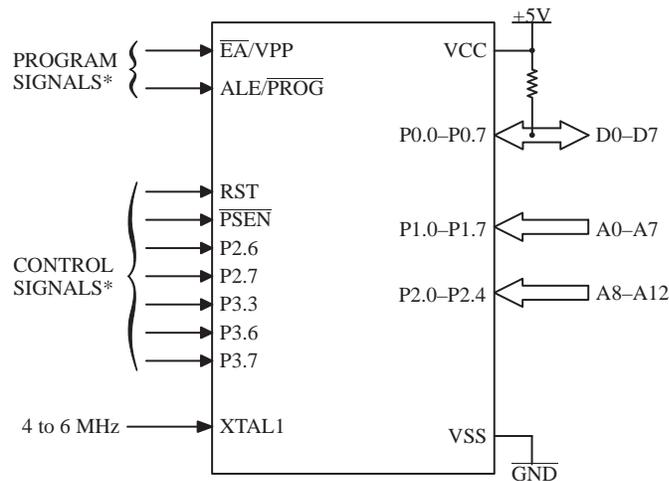
**Data Lines:** P0.0–P0.7 for D0–D7

**Control Signals:** RST,  $\overline{\text{PSEN}}$ , P2.6, P2.7, P3.3, P3.6, P3.7.

**Program Signals:** ALE/ $\overline{\text{PROG}}$ ,  $\overline{\text{EA}}$ /VPP.

**Table 6 EPROM Set-up Modes**

Mode	RST	PSEN	ALE/ PROG	EA/VPP	P2.6	P2.7	P3.3	P3.6	P3.7
Program Code data	1	0		12.75V	0	1	1	1	1
Verify Code data	1	0	1	1	0		0	1	1
Program Encryption Array Address 0–3Fh	1	0		12.75V	0	1	1	0	1
Read Signature Bytes	1	0	1	1	0		0	0	0



\* See Table 6 for proper value on these inputs

**Figure 8 Set-up modes configuration**

## Programming algorithm

The Improved Quick Pulse algorithm is based on the Quick Pulse algorithm and decreases the number of pulses applied during byte programming from 25 to 5.

To program the TSC87C52 the following sequence must be exercised:

- Step 1: Input the valid address on the address lines.
- Step 2: Input the appropriate data on the data lines.
- Step 3: Activate the combination of control signals.
- Step 4: Raise  $\overline{EA}/VPP$  from VCC to VPP (typical 12.75V).
- Step 5: Pulse  $\overline{ALE}/\overline{PROG}$  5 times.

Repeat step 1 through 5 changing the address and data for the entire array or until the end of the object file is reached (see Figure 9).

## Verify algorithm

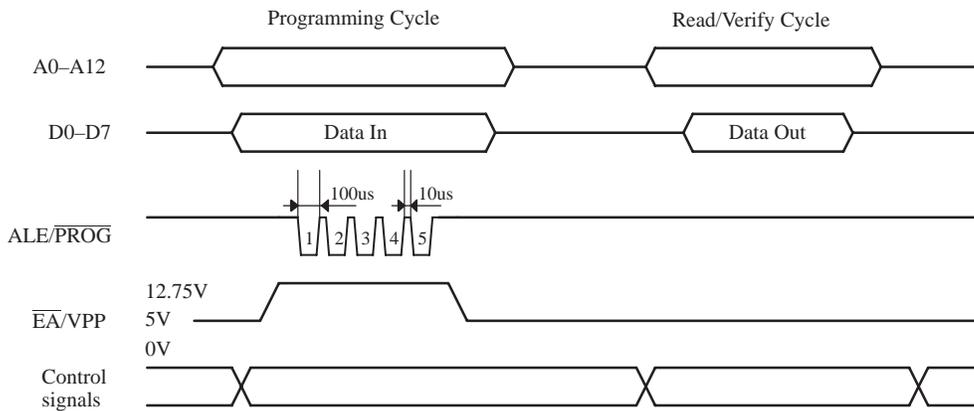
Code array verify must be done after each byte or block of bytes is programmed. In either case, a complete verify of the programmed array will ensure reliable programming of the TSC87C52.

To verify the TSC87C52 code the following sequence must be exercised :

- Step 1: Activate the combination of program signals.
- Step 2: Input the valid address on the address lines.
- Step 3: Input the appropriate data on the data lines.
- Step 4: Activate the combination of control signals.

Repeat step 2 through 4 changing the address and data for the entire array (see Figure 9).

The encryption array cannot be directly verified. Verification of the encryption array is done by observing that the code array is well encrypted.



**Figure 9 Programming and verification signal's waveform**

### Signature bytes

The TSC87C52 has four signature bytes in location 30h, 31h, 60h and 61h. To read these bytes follow the procedure for EPROM verify but activate the control lines provided in Table 6 for Read Signature Bytes. Table 7 shows the content of the signature byte for the TSC87C52.

**Table 7 Signature bytes content**

Location	Contents	Comment
30h	58h	Customer selection byte: TEMIC
31h	58h	Family selection byte: C51
60h	ADh	TSC87C52
61h	XXh	Product revision number

### EPROM Erasure (Windowed Packages Only)

Erasing the EPROM erases the code array and also the encryption array returning the parts to full functionality.

Erasure leaves all the EPROM cells in a 1's state.

### Erasure Characteristics

The recommended erasure procedure is exposure to ultraviolet light (at 2537 Å) to an integrated dose at least 15 W-sec/cm<sup>2</sup>. Exposing the EPROM to an ultraviolet lamp of 12,000 μW/cm<sup>2</sup> rating for 30 minutes, at a distance of about 25 mm, should be sufficient.

Erasure of the EPROM begins to occur when the chip is exposed to light with wavelength shorter than approximately 4,000 Å. Since sunlight and fluorescent lighting have wavelengths in this range, exposure to these light sources over an extended time (about 1 week in sunlight, or 3 years in room-level fluorescent lighting) could cause inadvertent erasure. If an application subjects the device to this type of exposure, it is suggested that an opaque label be placed over the window.

## Electrical Characteristics

### Absolute Maximum Ratings<sup>(1)</sup>

Ambient Temperature Under Bias:

C = commercial . . . . . 0°C to 70°C

I = industrial . . . . . -40°C to 85°C

Storage Temperature . . . . . -65°C to + 150°C

Voltage on VCC to VSS . . . . . -0.5 V to + 7 V

Voltage on VPP to VSS . . . . . -0.5 V to + 13 V

Voltage on Any Pin to VSS . . . -0.5 V to VCC + 0.5 V

Power Dissipation . . . . . 1 W<sup>(2)</sup>

### Notice:

1. Stresses at or above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

2. This value is based on the maximum allowable die temperature and the thermal resistance of the package.

## DC Parameters for Standard Voltage, commercial and industrial temperature range

TA = 0°C to +70°C; VSS = 0V; VCC = 5V ± 10%; F = 0 to 33 MHz.

TA = -40°C to +85°C; VSS = 0V; VCC = 5V ± 10%; F = 0 to 33 MHz.

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
VIL	Input Low Voltage	-0.5		0.2 VCC - 0.1	V	
VIH	Input High Voltage except XTAL1, RST	0.2 VCC + 0.9		VCC + 0.5	V	
VIH1	Input High Voltage, XTAL1, RST	0.7 VCC		VCC + 0.5	V	
VOL	Output Low Voltage, ports 1, 2, 3 <sup>(6)</sup>			0.3 0.45 1.0	V V V	IOL = 100µA <sup>(4)</sup> IOL = 1.6mA <sup>(4)</sup> IOL = 3.5mA <sup>(4)</sup>
VOL1	Output Low Voltage, port 0, ALE, $\overline{\text{PSEN}}$ <sup>(6)</sup>			0.3 0.45 1.0	V V V	IOL = 200µA <sup>(4)</sup> IOL = 3.2mA <sup>(4)</sup> IOL = 7.0mA <sup>(4)</sup>
VOH	Output High Voltage, ports 1, 2, 3	VCC - 0.3 VCC - 0.7 VCC - 1.5			V V V	IOH = -10µA IOH = -30µA IOH = -60µA VCC = 5V ± 10%
VOH1	Output High Voltage, port 0, ALE, $\overline{\text{PSEN}}$	VCC - 0.3 VCC - 0.7 VCC - 1.5			V V V	IOH = -200µA IOH = -3.2mA IOH = -7.0mA VCC = 5V ± 10%
RRST	RST Pulldown Resistor	50	90 <sup>(5)</sup>	200	kΩ	
IIL	Logical 0 Input Current ports 1, 2 and 3			-50	µA	Vin = 0.45V
ILI	Input Leakage Current			±10	µA	0.45 < Vin < VCC
ITL	Logical 1 to 0 Transition Current, ports 1, 2, 3			-650	µA	Vin = 2.0V
CIO	Capacitance of I/O Buffer			10	pF	fc = 1MHz, TA = 25°C
IPD	Power Down Current		10 <sup>(5)</sup>	50	µA	VCC = 2.0V to 5.5V <sup>(3)</sup>
ICC	Power Supply Current <sup>(7)</sup> Freq = 1 MHz   Icc op Icc idle Freq = 6 MHz   Icc op Icc idle  Freq ≥ 12 MHz Icc op = 1.25 Freq (MHz) + 5 mA  Icc idle = 0.36 Freq (MHz) + 2.7 mA		(5)  13@12MHz 16@16MHz 5.5@12MHz 7@16MHz	1.8 1 10 4	mA mA mA mA	VCC = 5.5V <sup>(1)</sup>  VCC = 5.5V <sup>(2)</sup>

## DC Parameters for Low Voltage, commercial and industrial temperature range

T<sub>A</sub> = 0°C to +70°C; V<sub>SS</sub> = 0V; V<sub>CC</sub> = 2.7V to 5V ± 10%; F = 0 to 16 MHz.

T<sub>A</sub> = -40°C to +85°C; V<sub>SS</sub> = 0V; V<sub>CC</sub> = 2.7V to 5V ± 10%; F = 0 to 16 MHz.

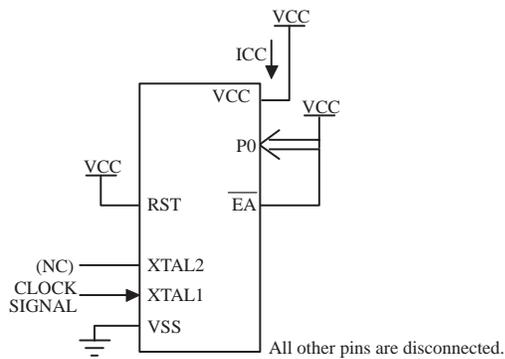
Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
VIL	Input Low Voltage	-0.5		0.2 VCC - 0.1	V	
VIH	Input High Voltage except XTAL1, RST	0.2 VCC + 0.9		VCC + 0.5	V	
VIH1	Input High Voltage, XTAL1, RST	0.7 VCC		VCC + 0.5	V	
VOL	Output Low Voltage, ports 1, 2, 3 <sup>(6)</sup>			0.45	V	IOL = 0.8mA <sup>(4)</sup>
VOL1	Output Low Voltage, port 0, ALE, PSEN <sup>(6)</sup>			0.45	V	IOL = 1.6mA <sup>(4)</sup>
VOH	Output High Voltage, ports 1, 2, 3	0.9 VCC			V	IOH = -10μA
VOH1	Output High Voltage, port 0, ALE, PSEN	0.9 VCC			V	IOH = -40μA
IIL	Logical 0 Input Current ports 1, 2 and 3			-50	μA	Vin = 0.45V
ILI	Input Leakage Current			±10	μA	0.45 < Vin < VCC
ITL	Logical 1 to 0 Transition Current, ports 1, 2, 3			-650	μA	Vin = 2.0V
RRST	RST Pulldown Resistor	50	90 <sup>(5)</sup>	200	kΩ	
CIO	Capacitance of I/O Buffer			10	pF	fc = 1MHz, T <sub>A</sub> = 25°C
IPD	Power Down Current		TBD <sup>(5)</sup>	TBD	μA	VCC = 2.0V to 5.5V <sup>(3)</sup>
ICC	Power Supply Current <sup>(7)</sup> Active Mode 16MHz Idle Mode 16MHz		TBD <sup>(5)</sup> TBD <sup>(5)</sup>	TBD TBD	mA mA	VCC = 3.3V <sup>(1)</sup> VCC = 3.3V <sup>(2)</sup>

### Notes for DC Electrical Characteristics

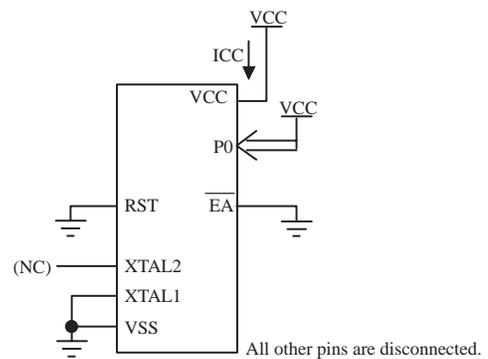
- Operating ICC is measured with all output pins disconnected; XTAL1 driven with TCLCH, TCHCL = 5 ns (see Figure 13), VIL = VSS + 0.5V, VIH = VCC - 0.5V; XTAL2 N.C.; EA = RST = Port 0 = VCC. ICC would be slightly higher if a crystal oscillator used (see NO TAG).
- Idle ICC is measured with all output pins disconnected; XTAL1 driven with TCLCH, TCHCL = 5ns, VIL = VSS + 0.5V, VIH = VCC - 0.5V; XTAL2 N.C.; Port 0 = VCC; EA = RST = VSS (see Figure 11).
- Power Down ICC is measured with all output pins disconnected; EA = VSS, PORT 0 = VCC; XTAL2 NC.; RST = VSS (see NO TAG).
- Capacitance loading on Ports 0 and 2 may cause spurious noise pulses to be superimposed on the VOLs of ALE and Ports 1 and 3. The noise is due to external bus capacitance discharging into the Port 0 and Port 2 pins when these pins make 1 to 0 transitions during bus operation. In the worst cases (capacitive loading 100pF), the noise pulse on the ALE line may exceed 0.45V with maxi VOL peak 0.6V. A Schmitt Trigger use is not necessary.
- Typicals are based on a limited number of samples and are not guaranteed. The values listed are at room temperature and 5V.
- Under steady state (non-transient) conditions, IOL must be externally limited as follows:

Maximum IOL per port pin:	10 mA
Maximum IOL per 8-bit port:	
Port 0:	26 mA
Ports 1, 2 and 3:	15 mA
Maximum total IOL for all output pins:	71 mA

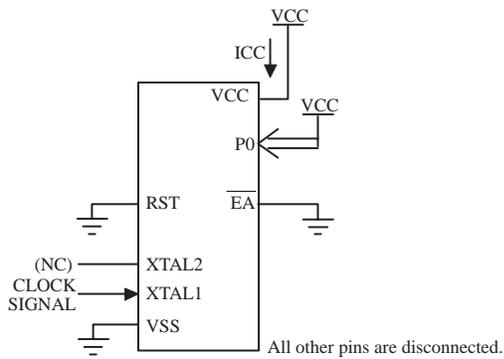
If IOL exceeds the test condition, VOL may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test conditions.
- For other values, please contact your sales office.



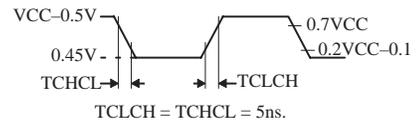
**Figure 10 ICC Test Condition, Active Mode**



**Figure 12 ICC Test Condition, Power Down Mode**



**Figure 11 ICC Test Condition, Idle Mode**



**Figure 13 Clock Signal Waveform for ICC Tests in Active and Idle Modes**

## AC Parameters

### Explanation of the AC Symbols

Each timing symbol has 5 characters. The first character is always a “T” (stands for time). The other characters, depending on their positions, stand for the name of a signal or the logical status of that signal. The following is a list of all the characters and what they stand for.

Example: TAVLL = Time for Address Valid to ALE Low.  
 TLLPL = Time for ALE Low to PSEN Low.

TA = 0 to +70°C; VSS = 0V VCC = 5V±10%; 0 to 12MHz

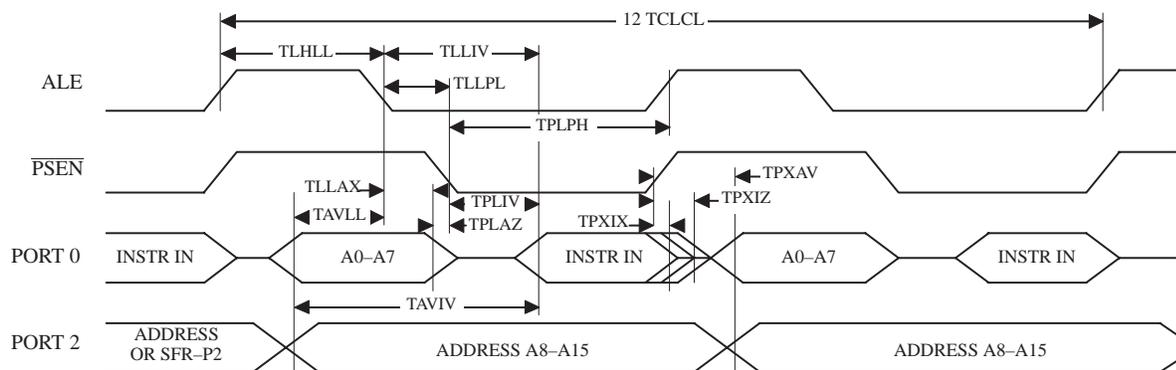
TA = -40°C to +85°C; VSS = 0V; VCC = 5V ± 10%; F = 0 to 12MHz.

(Load Capacitance for PORT 0, ALE and PSEN = 100pf; Load Capacitance for all other outputs = 80 pF.)

### External Program Memory Characteristics

Symbol	Parameter	0 to 12MHz		Units
		Min	Max	
TLHLL	ALE pulse width	2TCLCL - 40		ns
TAVLL	Address Valid to ALE	TCLCL - 40		ns
TLLAX	Address Hold After ALE	TCLCL - 30		ns
TLLIV	ALE to Valid Instruction In		4TCLCL - 100	ns
TLLPL	ALE to PSEN	TCLCL - 30		ns
TPLPH	PSEN Pulse Width	3TCLCL - 45		ns
TPLIV	PSEN to Valid Instruction In		3TCLCL - 105	ns
TPXIX	Input Instruction Hold After PSEN	0		ns
TPXIZ	Input Instruction Float After PSEN		TCLCL - 25	ns
TPXAV	PSEN to Address Valid	TCLCL - 8		ns
TAVIV	Address to Valid Instruction In		5TCLCL - 105	ns
TPXAV	PSEN Low to Address Float		10	ns

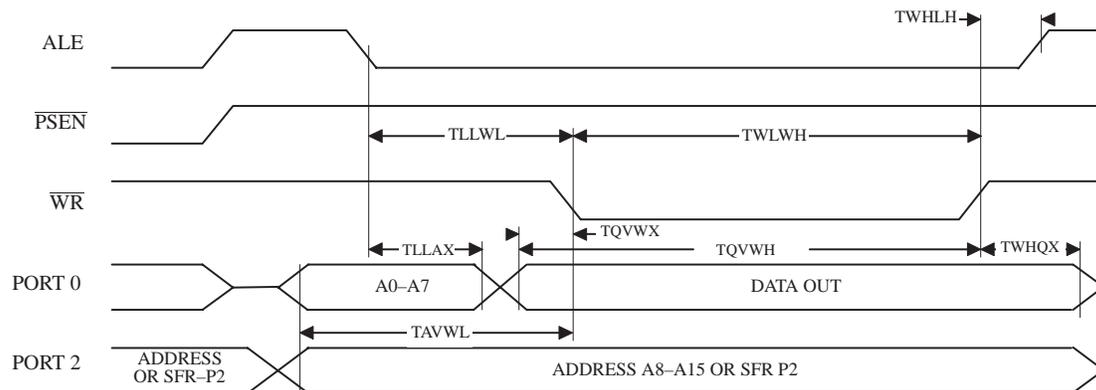
### External Program Memory Read Cycle



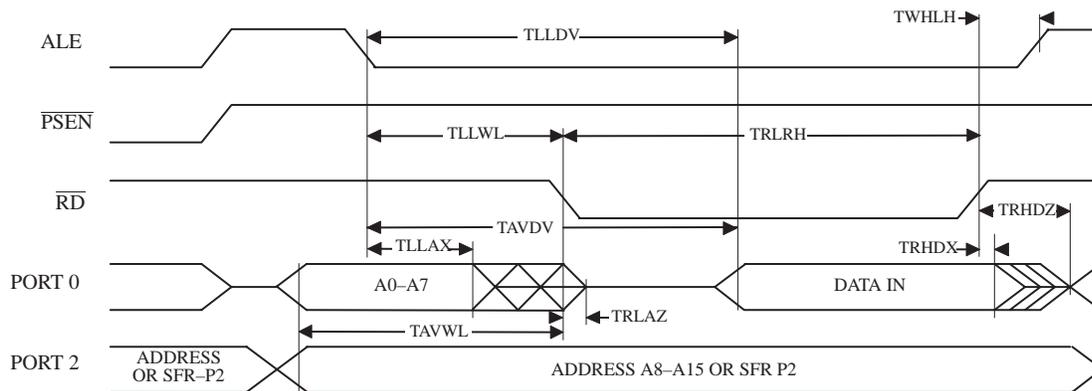
## External Data Memory Characteristics

Symbol	Parameter	0 to 12MHz		Units
		Min	Max	
TRLRH	$\overline{RD}$ Pulse Width	6TCLCL-100		ns
TWLWH	$\overline{WR}$ Pulse Width	6TCLCL-100		ns
TRLDV	$\overline{RD}$ to Valid Data In		5TCLCL-165	ns
TRHDX	Data Hold After $\overline{RD}$	0		ns
TRHDZ	Data Float After $\overline{RD}$		2TCLCL-60	ns
TLLDV	ALE to Valid Data In		8TCLCL-150	ns
TAVDV	Address to Valid Data In		9TCLCL-165	ns
TLLWL	ALE to $\overline{WR}$ or $\overline{RD}$	3TCLCL-50	3TCLCL+50	ns
TAVWL	Address to $\overline{WR}$ or $\overline{RD}$	4TCLCL-130		ns
TQVWX	Data Valid to $\overline{WR}$ Transition	TCLCL-50		ns
TQVWH	Data set-up to $\overline{WR}$ High	7TCLCL-150		ns
TWHQX	Data Hold After $\overline{WR}$	TCLCL-50		ns
TRLAZ	$\overline{RD}$ Low to Address Float		0	ns
TWHLH	$\overline{RD}$ or $\overline{WR}$ High to ALE high	TCLCL-40	TCLCL+40	ns

## External Data Memory Write Cycle



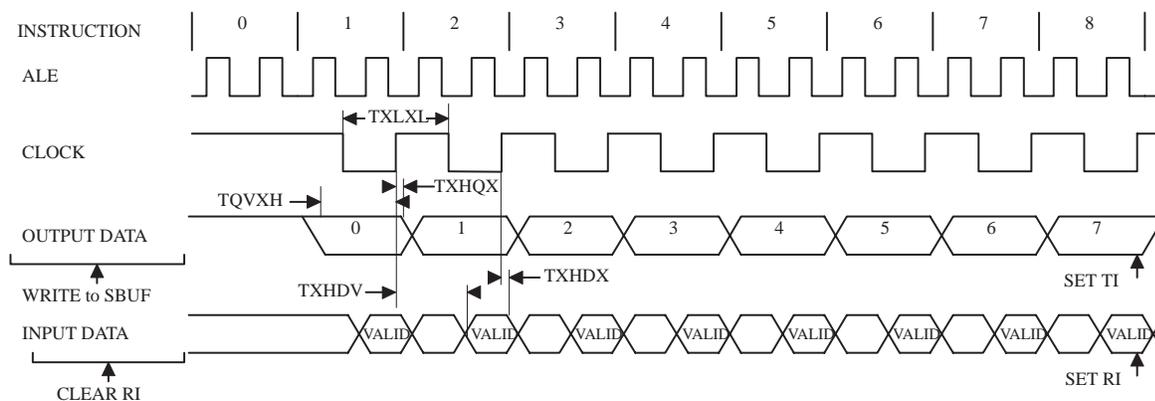
## External Data Memory Read Cycle



## Serial Port Timing – Shift Register Mode

Symbol	Parameter	0 to 12MHz		Units
		Min	Max	
TXLXL	Serial port clock cycle time	12TCLCL		ns
TQVHX	Output data set-up to clock rising edge	10TCLCL-133		ns
TXHQX	Output data hold after clock rising edge	2TCLCL-117		ns
TXHDX	Input data hold after clock rising edge	0		ns
TXHDV	Clock rising edge to input data valid		10TCLCL-133	ns

## Shift Register Timing Waveforms

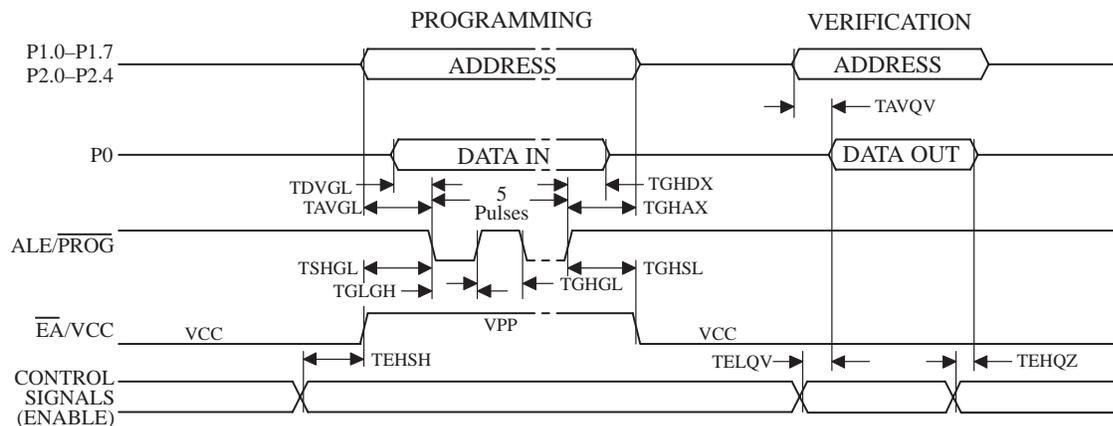


## EPROM Programming and Verification Characteristics

$T_A = 21^\circ\text{C}$  to  $27^\circ\text{C}$ ;  $V_{SS} = 0\text{V}$ ;  $V_{CC} = 5\text{V} \pm 10\%$ .

Symbol	Parameter	Min	Max	Units
VPP	Programming Supply Voltage	12.5	13	V
IPP	Programming Supply Current		75	mA
1/TCLCL	Oscillator Frequency	4	6	MHz
TAVGL	Address Setup to $\overline{\text{PROG}}$ Low	48 TCLCL		
TGHAX	Address Hold after $\overline{\text{PROG}}$	48 TCLCL		
TDVGL	Data Setup to $\overline{\text{PROG}}$ Low	48 TCLCL		
TGHDX	Data Hold after $\overline{\text{PROG}}$	48 TCLCL		
TEHSH	(Enable) High to VPP	48 TCLCL		
TSHGL	VPP Setup to $\overline{\text{PROG}}$ Low	10		$\mu\text{s}$
TGHSL	VPP Hold after $\overline{\text{PROG}}$	10		$\mu\text{s}$
TGLGH	$\overline{\text{PROG}}$ Width	90	110	$\mu\text{s}$
TAVQV	Address to Valid Data		48 TCLCL	
TELQV	ENABLE Low to Data Valid		48 TCLCL	
TEHQZ	Data Float after ENABLE	0	48 TCLCL	
TGHGL	$\overline{\text{PROG}}$ High to $\overline{\text{PROG}}$ Low	10		$\mu\text{s}$

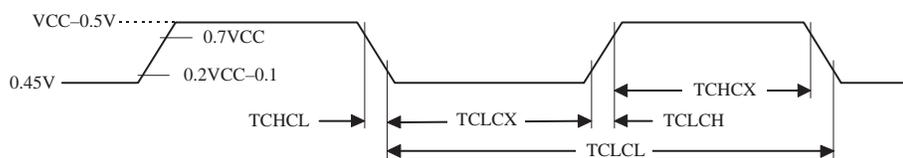
## EPROM Programming and Verification Waveforms



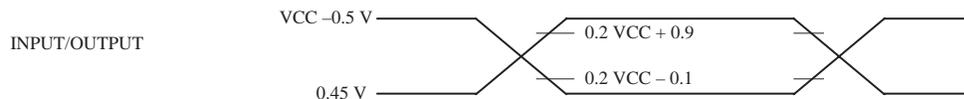
## External Clock Drive Characteristics (XTAL1)

Symbol	Parameter	Min	Max	Units
TCLCL	Oscillator Period	30		ns
TCHCX	High Time	5		ns
TCLCX	Low Time	5		ns
TCLCH	Rise Time		5	ns
TCHCL	Fall Time		5	ns

## External Clock Drive Waveforms

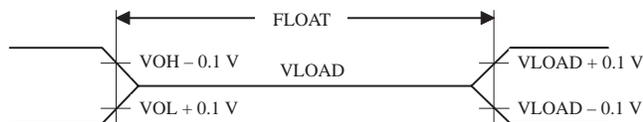


## AC Testing Input/Output Waveforms



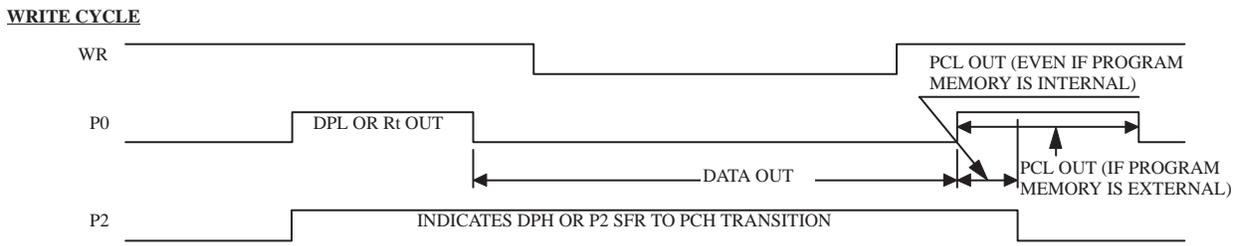
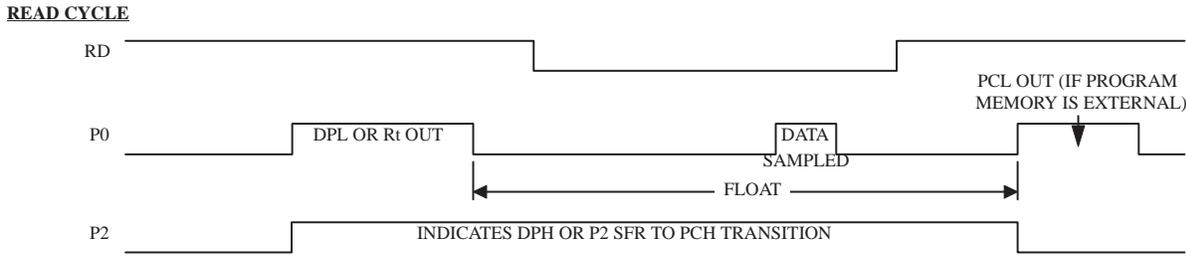
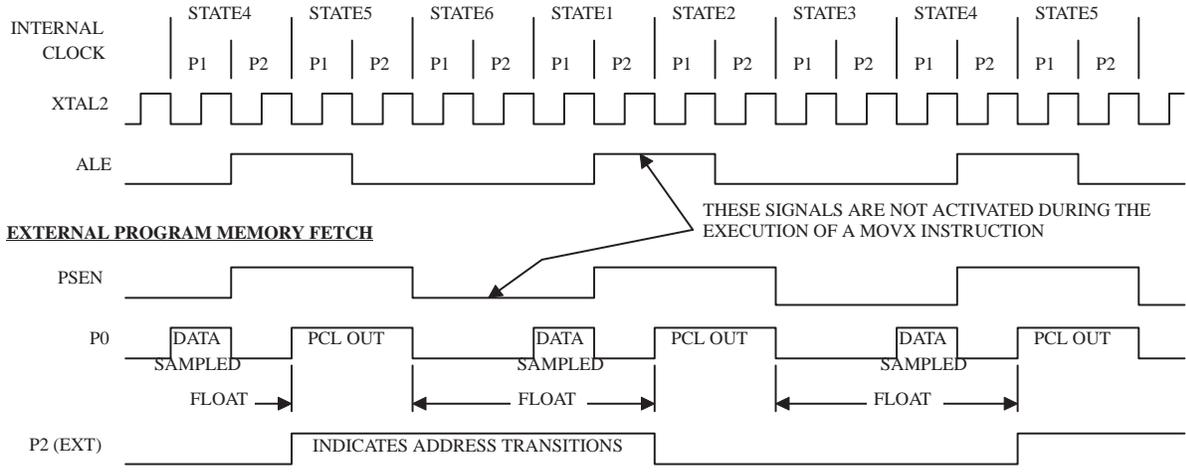
AC inputs during testing are driven at  $V_{CC} - 0.5$  for a logic "1" and  $0.45V$  for a logic "0". Timing measurement are made at  $V_{IH}$  min for a logic "1" and  $V_{IL}$  max for a logic "0".

## Float Waveforms



For timing purposes as port pin is no longer floating when a  $100\text{ mV}$  change from load voltage occurs and begins to float when a  $100\text{ mV}$  change from the loaded  $VOH/VOL$  level occurs.  $I_{OL}/I_{OH} \geq \pm 20\text{mA}$ .

**Clock Waveforms**



This diagram indicates when signals are clocked internally. The time it takes the signals to propagate to the pins, however, ranges from 25 to 125ns. This propagation delay is dependent on variables such as temperature and pin loading. Propagation also varies from output to output and component. Typically though (TA=25°C fully loaded) RD and WR propagation delays are approximately 50ns. The other signals are typically 85ns. Propagation delays are incorporated in the AC specifications.

## Ordering Information

