21010
1M (1,048,576 x 1) DYNAMIC RAM WITH FAST PAGE MODE

- **Performance Range**

Symbol	Parameter	21010-07	21010-08	Units
t_{RAC}	Access Time from $\overline{\text{RAS}}$	70	80	ns
t_{CAC}	Access Time from $\overline{\text{CAS}}$	20	25	ns
t_{RC}	Read Cycle Time	130	160	ns

- **Fast Page Mode Operation**
- **$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ Refresh Capability**
- **Common I/O Using "Early Write"**
- **Single 5V ± 10% Power Supply**
- **512 Cycles/8 ms refresh**
- **Available in Plastic DIP(P) and SOJ(T) Packages**

Intel's 21010 is a CMOS high speed 1,048,576 x 1 dynamic RAM optimized for high performance applications such as mainframes, graphics and microprocessor systems.

The 21010 features Fast Page Mode operation which allows high speed random access of memory cells within the same row.

$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh capability provides on-chip auto refresh as an alternative to $\overline{\text{RAS}}$ only refresh. All Inputs, Output and Clocks are fully CMOS and TTL compatible.

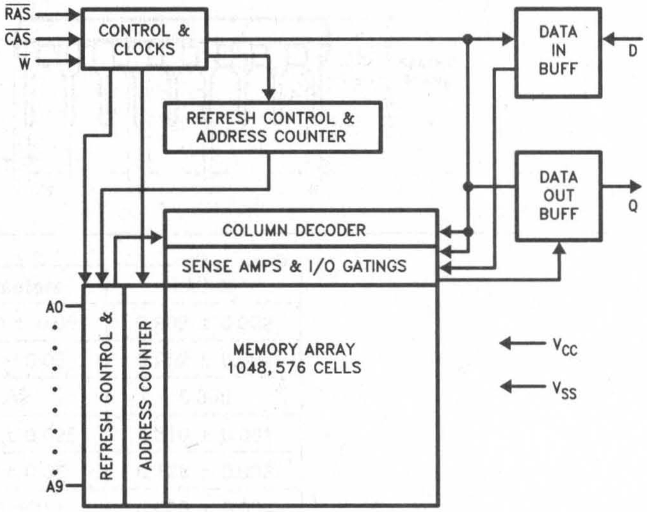

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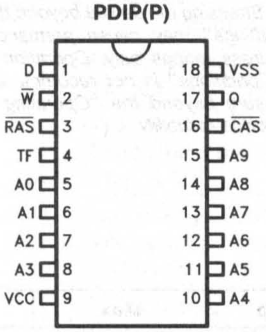
Figure 1. Block Diagram

PIN CONFIGURATION



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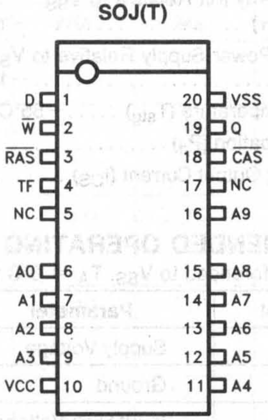

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NOTE:
T.F. = Test Function, Ground or No Connect

Pin Description

A_0–A_9	Address Inputs
$\overline{W}$	Read/Write Strobe
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
D	Data In
Q	Data Out
V_{SS}	Ground
V_{CC}	Power +5V

ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to V_{SS}
(V_{IN}, V_{OUT}) .... −1V to +7.0V
Voltage on Power Supply Relative to V_{SS}
(V_{CC}) .... −1V to +7.0V
Storage Temperature (T_{stg}) ..... −55°C to +125°C
Power Dissipation (P_d) .... 600 mW
Short Circuit Output Current (I_{OS}) .... 50 mA

NOTICE: This is a production data sheet. The specifications are subject to change without notice.

**WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

RECOMMENDED OPERATING CONDITIONS

(Voltage Referenced to V_{SS}. T_A = 0°C to +70°C)

Symbol	Parameter	Min	Typ	Max	Units
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
V_{SS}	Ground	0	0	0	V
V_{IH}	Input High Voltage	2.4		V_{CC} + 1	V
V_{IL}	Input Low Voltage	−1.0		0.8	V

NOTES:
1. V_{IL} (Min) = −1.0V for continuous DC level.
2. V_{IL} (Min) = −2.0V for pulse width < 20 ns.

Capacitance (T_A = 25°C)

Symbol	Parameter	Min	Max	Units
C_{in1}	Input Capacitance (A_0–A_9, D)		6	pF
C_{in2}	Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$)		7	pF
C_{out}	Output Capacitance (Q)		7	pF

DC AND OPERATING CHARACTERISTICS

(Recommended Operating Conditions unless Otherwise Noted)

Symbol	Parameter	Speed	Min	Max	Units
I_{CC1} I_{CC1}	Operating Current ($\overline{RAS}$ and $\overline{CAS}$ Cycling @ t_{RC} = Min	-07 -08		80 70	mA mA
I_{CC2}	Standby Current (TTL Power Supply Current)	-06		2	mA
I_{CC3} I_{CC3}	$\overline{RAS}$ Only Refresh Current ($\overline{CAS}$ = V_{IH}, $\overline{RAS}$ Cycling @ t_{RC} = Min	-07 -08		80 70	mA mA
I_{CC4} I_{CC4}	Fast Page Mode Current ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$ Cycling @ t_{PC} = Min	-07 -08		60 50	mA mA

DC AND OPERATING CHARACTERISTICS (Continued)

(Recommended Operating Conditions unless Otherwise Noted)

Symbol	Parameter	Speed	Min	Max	Units
I_{CC5}	Standby Current (CMOS Power Supply Current)			1	mA
I_{CC6}	$\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ Refresh Current (RAS and CAS Cycling @ t_{RC} = Min	-07 -08		80 70	mA mA
I_{IL}	Input Leakage Current (Any Input $0 < V_{IN} < 6.5V$ All Other Pins = 0V)		−10	10	μA
I_{OL}	Output Leakage Current (Data Out is Disabled and $0 < V_{OUT} < 5.5V$)		−10	10	μA
V_{OH}	Output High Voltage Level ($I_{OH} = -5$ mA)		2.4	—	V
V_{OL}	Output Low Voltage Level ($I_{OL} = 4.2$ mA)		—	0.4	V

NOTE:
ICC1, ICC3, ICC4, and ICC6 are dependent on output loading and cycle rates. Specified values are obtained with the output open. I_{CC} is specified as average current.

AC CHARACTERISTICS (See Notes 1, 2, 3)

(T_A = 0°C to +70°C, V_{CC} = 5V ±10%)

Symbol	Parameter	21010-07		21010-08		Units	Notes
		Min	Max	Min	Max		
t_{REF}	Time between Refresh		8		8	ms	
t_{RC}	Random R/W Cycle Time	130		160		ns	
t_{RWC}	RMW Cycle Time	155		185		ns	
t_{RAC}	Access Time from $\overline{\text{RAS}}$		70		80	ns	4, 7
t_{CAC}	Access Time from $\overline{\text{CAS}}$		20		25	ns	5, 7
t_{AA}	Access Time from Column Address		35		40	ns	6, 7
t_{CLZ}	$\overline{\text{CAS}}$ to Output in Low Z	0		0		ns	
t_{OFF}	Output Buffer Turn-Off Delay Time	0	20	0	20	ns	8
t_T	Transition Time	3	50	3	50	ns	
t_{RP}	$\overline{\text{RAS}}$ Precharge Time	50		70		ns	

AC CHARACTERISTICS (See Notes 1, 2, 3)

(T_A = 0°C to +70°C, V_{CC} = 5V ±10%) (Continued)

Symbol	Parameter	21010-07		21010-08		Units	Notes
		Min	Max	Min	Max		
t_{RAS}	$\overline{\text{RAS}}$ Pulse Width	70	10K	80	10K	ns	
t_{RSH}	$\overline{\text{RAS}}$ Hold Time	20		25		ns	
t_{CRP}	$\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ Precharge Time	10		10		ns	
t_{RCD}	$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ Delay Time	20	50	25	60	ns	
t_{CAS}	$\overline{\text{CAS}}$ Pulse Width	20	10K	25	10K	ns	
t_{CSH}	$\overline{\text{CAS}}$ Hold Time	70		80		ns	
t_{CPN}	$\overline{\text{CAS}}$ Precharge Time	10		10		ns	
t_{ASR}	Row Address Set-Up Time	0		0		ns	
t_{RAH}	Row Address Hold Time	15		15		ns	
t_{ASC}	Column Address Set-Up Time	0		0		ns	
t_{CAH}	Column Address Hold Time	15		20		ns	
t_{AR}	Column Address Time Referenced to $\overline{\text{RAS}}$	55		65		ns	
t_{RAD}	$\overline{\text{RAS}}$ to Column Address Delay Time	15	35	20	40	ns	11
t_{RAL}	Column Address to $\overline{\text{RAS}}$ Lead Time	35		40		ns	
t_{RCS}	Read Command Set-Up Time	0		0		ns	
t_{RRH}	Read Command Hold Time Referenced to $\overline{\text{RAS}}$	10		10		ns	12
t_{RCH}	Read Command Hold Time Referenced to $\overline{\text{CAS}}$	0		0		ns	12
t_{WCS}	Write Command Set-Up Time	0		0		ns	13
t_{WCH}	Write Command Hold Time	15		20		ns	

AC CHARACTERISTICS (See Notes 1, 2, 3)

(T_A = 0°C to +70°C, V_{CC} = 5V ±10%) (Continued)

Symbol	Parameter	21010-07		21010-08		Units	Notes
		Min	Max	Min	Max		
t_{WCR}	Write Command Referenced to $\overline{\text{RAS}}$	55		60		ns	
t_{WP}	$\overline{\text{WE}}$ Pulse Width	15		15		ns	
t_{RWL}	Write Command to $\overline{\text{RAS}}$ Lead Time	20		25		ns	
t_{CWL}	Write Command to $\overline{\text{CAS}}$ Lead Time	20		20		ns	
t_{DS}	D_{IN} Set-Up Time	0		0		ns	
t_{DH}	D_{IN} Hold Time	15		20		ns	
t_{DHR}	Data-In Hold Time Referenced to $\overline{\text{RAS}}$	55		60		ns	
t_{RWD}	$\overline{\text{RAS}}$ to $\overline{\text{WE}}$ Delay Time	70		80		ns	13
t_{CWD}	$\overline{\text{CAS}}$ to $\overline{\text{WE}}$ Delay Time	20		25		ns	13
t_{AWD}	Column Address to $\overline{\text{WE}}$ Delay Time	35		40		ns	
t_{RPC}	$\overline{\text{RAS}}$ Precharge Time to $\overline{\text{CAS}}$ Active Time	10		10		ns	
t_{CSR}	$\overline{\text{CAS}}$ Set-Up Time for $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ Refresh	10		10		ns	
t_{CHR}	$\overline{\text{CAS}}$ Hold Time for $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ Refresh	30		30		ns	
t_{CPT}	Refresh Counter Test $\overline{\text{CAS}}$ Precharge Time	35		40		ns	

AC CHARACTERISTICS (See Notes 1, 2, 3)

(T_A = 0°C to +70°C, V_{CC} = 5V ±10%) (Continued)

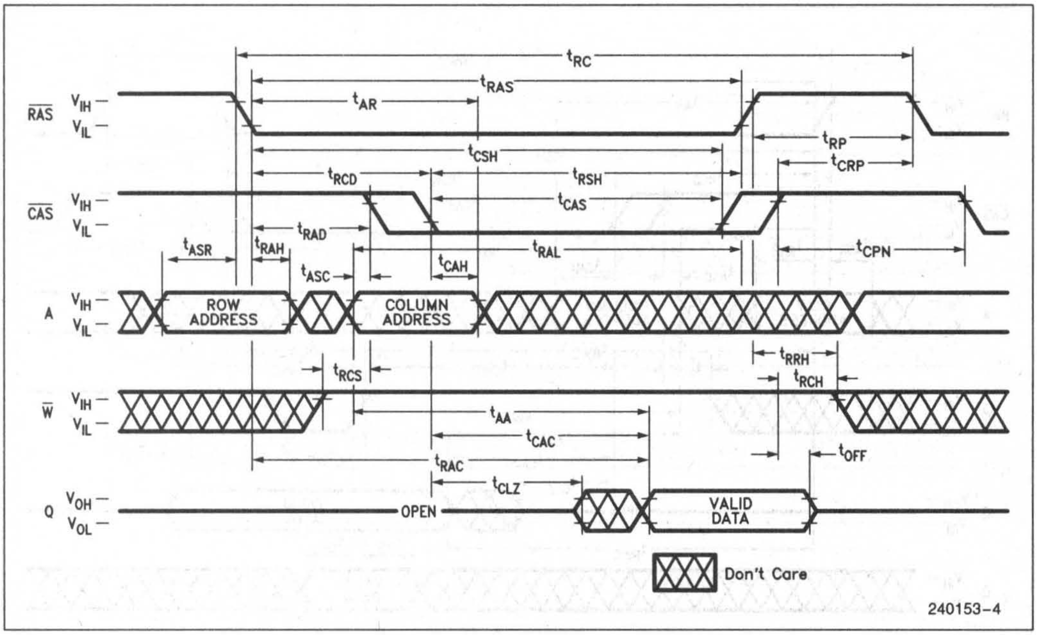
Symbol	Parameter	21010-07		21010-08		Units	Notes
		Min	Max	Min	Max		
FAST PAGE MODE							
t_{PC}	Fast Page Mode Cycle Time	50		55		ns	
t_{PRWC}	Fast Page Mode RMW Cycle Time	75		80		ns	
t_{CPA}	Access Time from $\overline{CAS}$ Precharge		40		45	ns	7, 14
t_{CP}	Fast Page Mode CAS Precharge Time	10		10		ns	
t_{RASP}	$\overline{RAS}$ Pulse Width (Fast Page Mode)	70	100K	80	100K	ns	

NOTES:

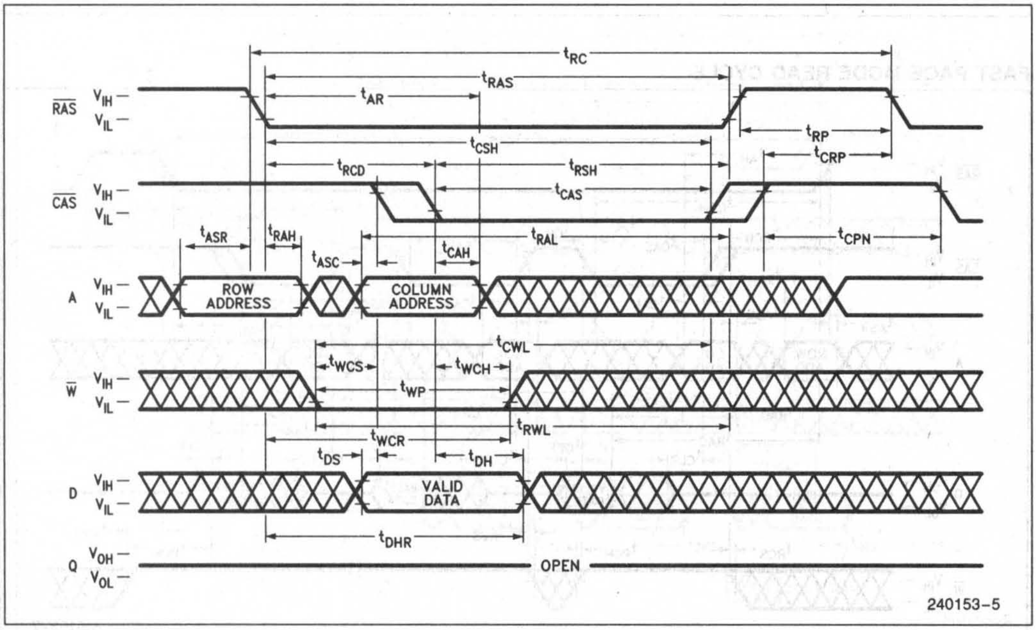
1. An initial pause of 200 μs is required after power-up followed by any 8 $\overline{RAS}$-only cycles before proper device operation is achieved.
2. A.C. characteristics assume t_T = 5 ns.
3. V_{IN} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} (min) and V_{IL} (max).
4. Assumes that $t_{RCD} \leq t_{RCD}$ (max), $t_{RAD} \leq t_{RAD}$ (max). If t_{RCD} (or t_{RAD}) is greater than the maximum recommended value shown in this table t_{RAC} will be increased by the amount that t_{RCD} (or t_{RAD}) exceeds the value shown.
5. If $t_{RCD} \geq t_{RCD}$ (max), $t_{RAD} \geq t_{RAD}$ (max), and $t_{ASC} \geq t_{AA} - t_{CAC} - t_T$ access time is t_{CAC}.
6. If $t_{RAD} \geq t_{RAD}$ (max) and $t_{ASC} \leq t_{AA} - t_{CAC} - t_T$, access time is t_{AA}.
7. Measured with a load equivalent to two TTL loads and 100 pF.
8. t_{OFF} is specified that output buffer changes to high impedance state.
9. Operation within the t_{RCD} (max) limit insures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, access time is controlled exclusively by t_{CAC} or t_{AA}.
10. t_{RCD} (min) = t_{RAH} (min) + 2 t_T + t_{ASC} (min).
11. Operation within the t_{RAD} (max) limit insures that t_{RAC} (max) can be met. t_{RAD} (max) is specified as a reference point only; if t_{RAD} is greater than the specified t_{RAD} (max) limit, access time is exclusively controlled by t_{CAC} or t_{AA}.
12. Either t_{RRH} or t_{RCH} must be specified for a read cycle.
13. t_{WCS}, t_{CWD}, t_{RWD}, and t_{AWD} are non-restrictive operating parameters. They are included in the Data Sheet as Electrical Characteristics only.
14. t_{CPA} is access time from the selection of a new column address (that is caused by changing CAS from "L" to "H").

TIMING DIAGRAMS

READ CYCLE

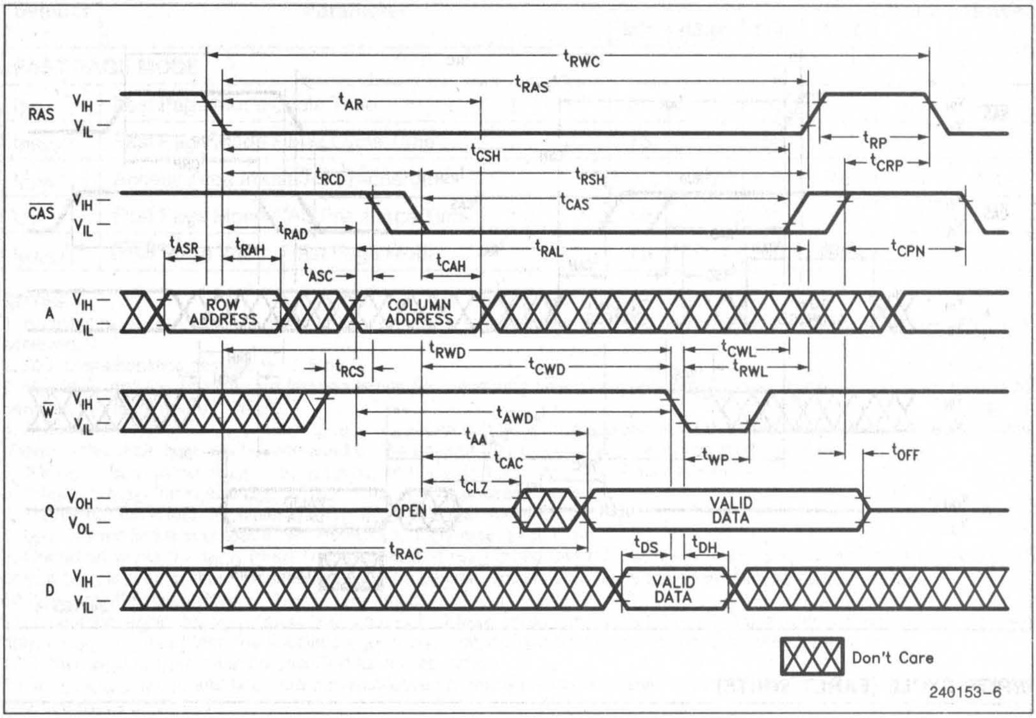


WRITE CYCLE (EARLY WRITE)



TIMING DIAGRAMS (Continued)

READ-WRITE/READ-MODIFY-WRITE CYCLE



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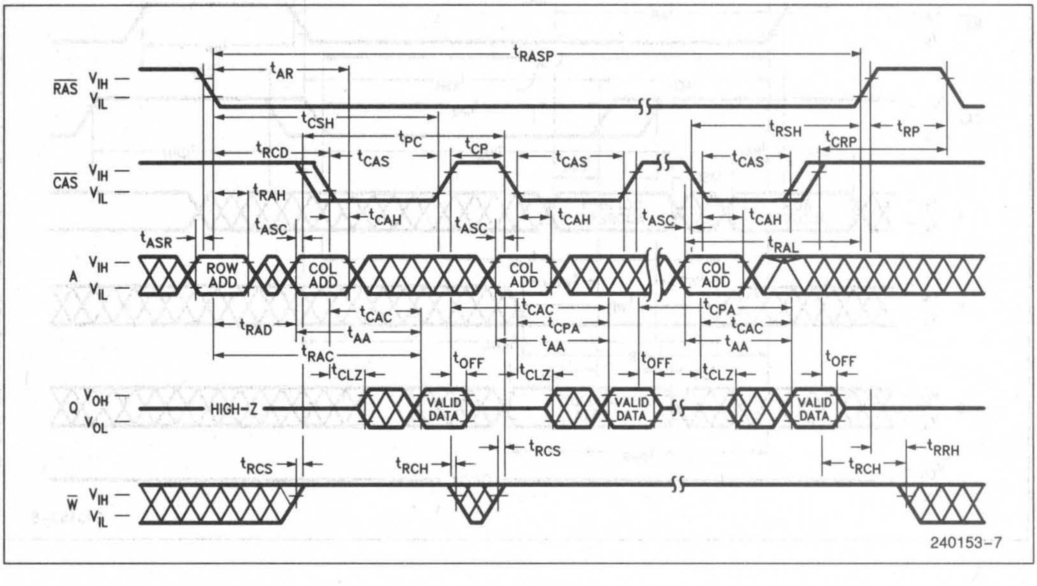
FAST PAGE MODE READ CYCLE



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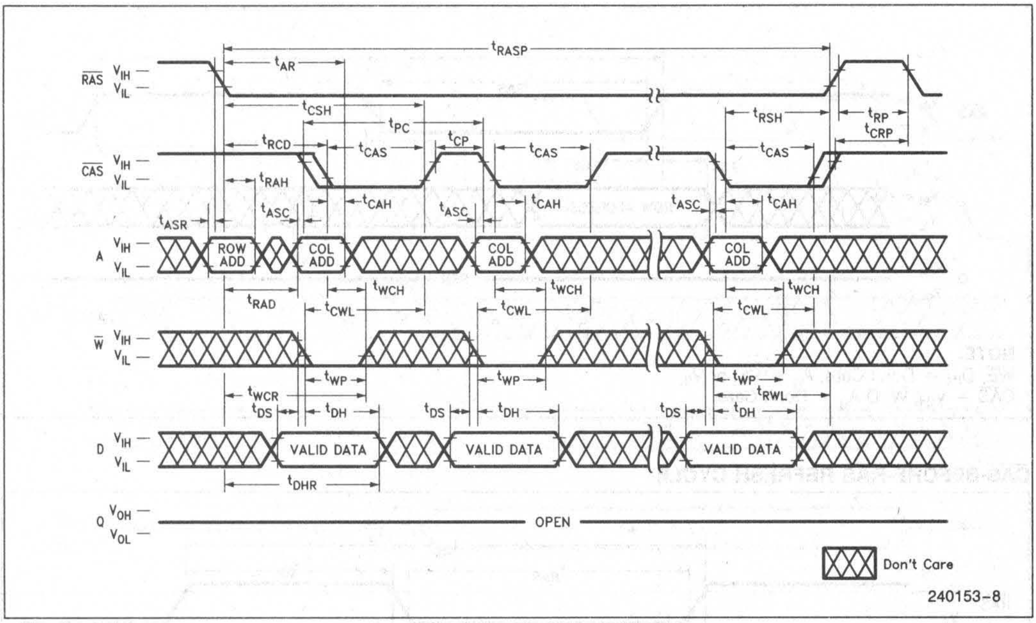
TIMING DIAGRAMS (Continued)

FAST PAGE MODE WRITE CYCLE



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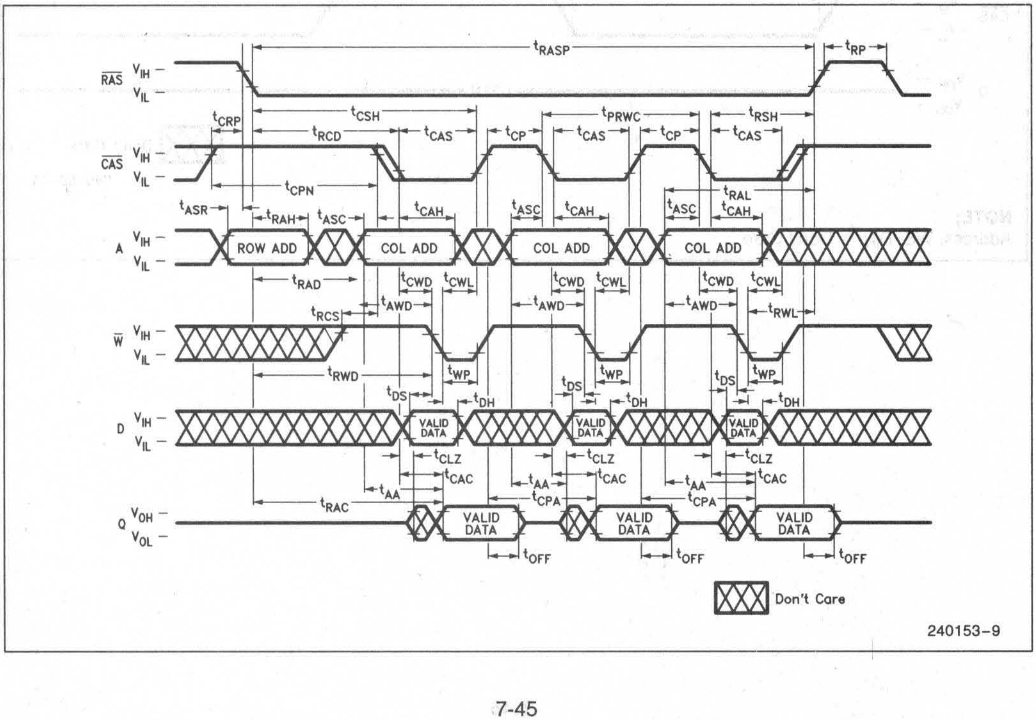
FAST PAGE MODE READ-WRITE CYCLE



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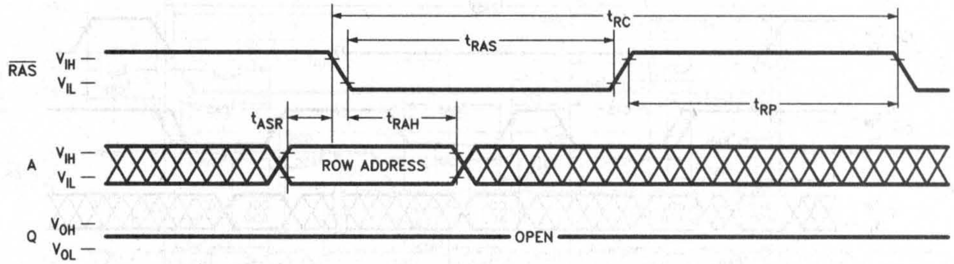
TIMING DIAGRAMS (Continued)

$\overline{RAS}$-ONLY REFRESH CYCLE



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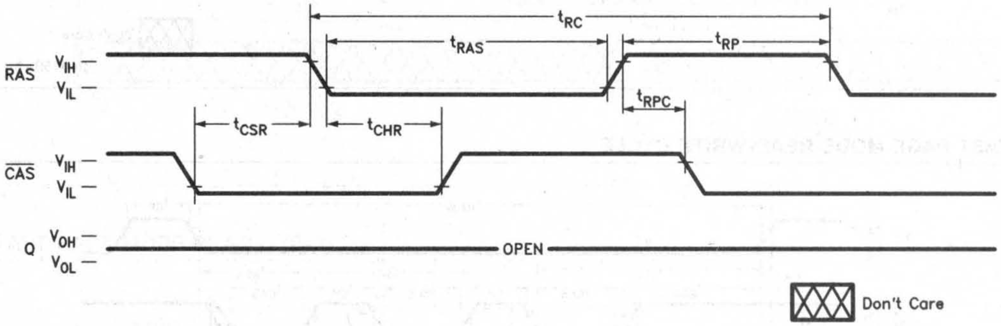
NOTE:
$\overline{WE}$, D_{IN} = Don't Care, $A_g = V_{IH}$ or V_{IL}
$\overline{CAS} = V_{IH}$, $\overline{W}$, D A_g = Don't Care

$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE



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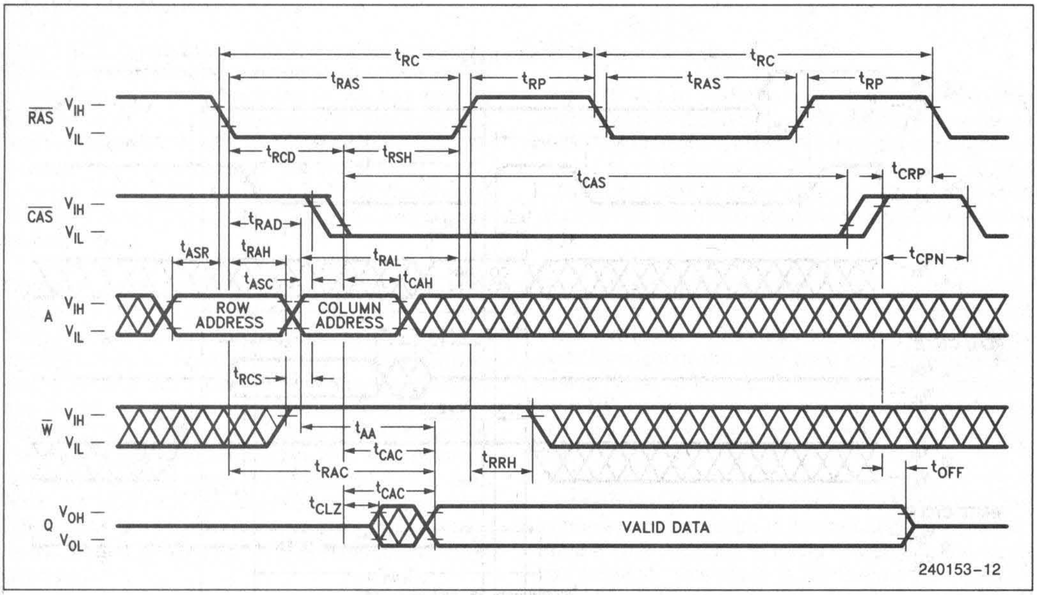
NOTE:
Address, $\overline{WE}$, D_{IN} = Don't Care

TIMING DIAGRAMS (Continued)

HIDDEN REFRESH CYCLE



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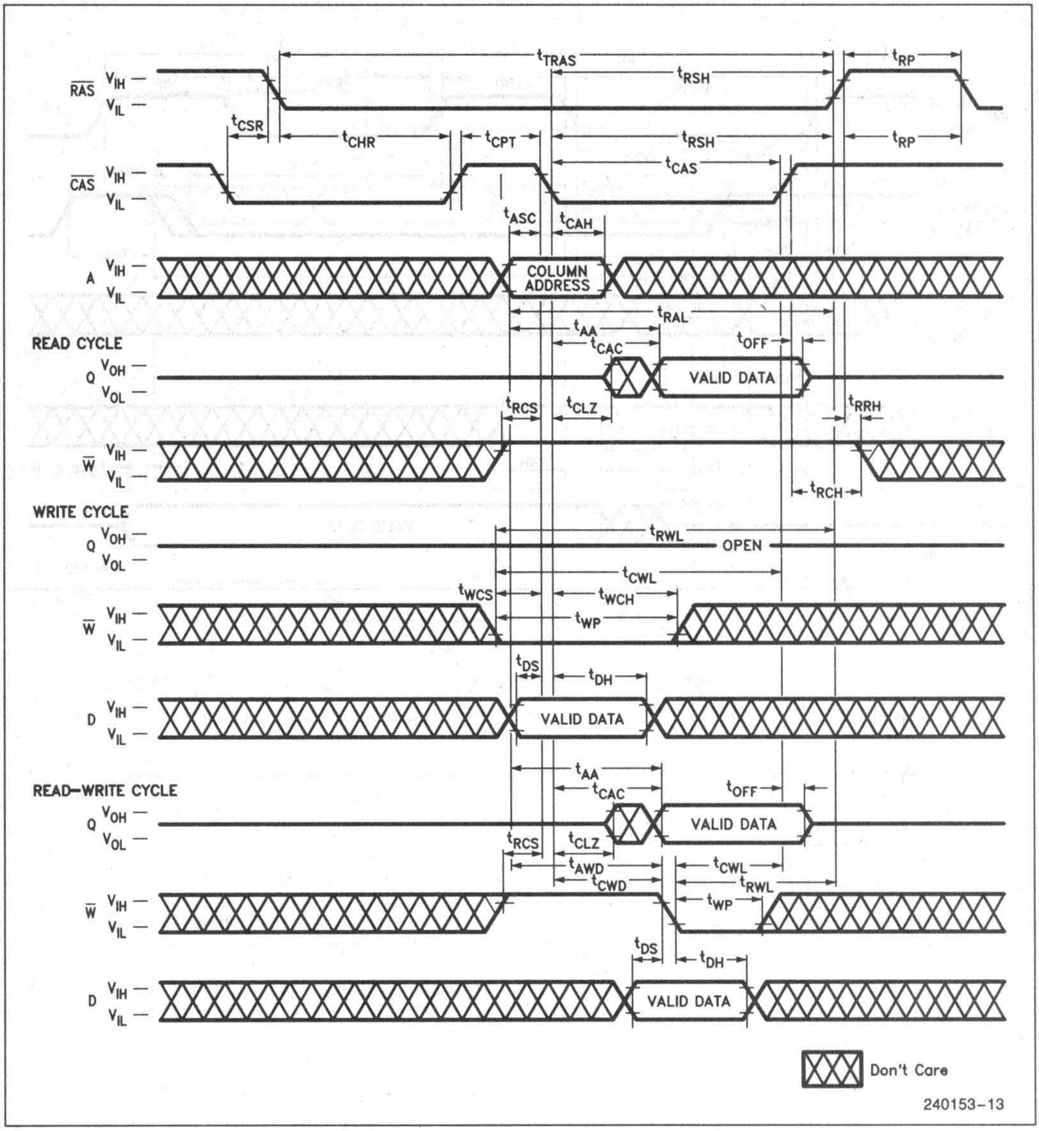
TIMING DIAGRAMS (Continued)

$\overline{\text{CAS}}$-BEFORE-$\overline{\text{RAS}}$ REFRESH COUNTER TEST CYCLE



21010 OPERATION

Device Operation

The 21010 contains 1,048,576 memory locations. Twenty address bits are required to address a particular memory location. Since the 21010 has only 10 address input pins, time multiplexed addressing is used to input 10 row and 10 column addresses. The multiplexing is controlled by the timing relationship between the row address strobe ($\overline{\text{RAS}}$), the column address strobe ($\overline{\text{CAS}}$) and the valid row and column address inputs.

Operation of the 21010 begins by strobing in a valid row address with $\overline{\text{RAS}}$ while $\overline{\text{CAS}}$ remains high. Then the address on the 10 address input pins is changed from a row address to a column address and is strobed in by $\overline{\text{CAS}}$. This is the beginning of any 21010 cycle in which a memory location is accessed. The specific type of cycle is determined by the state of the write enable pin and various timing relationships. The cycle is terminated when both $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ have returned to the high state. Another cycle can be initiated after $\overline{\text{RAS}}$ remains high long enough to satisfy the $\overline{\text{RAS}}$ precharge time (t_{RP}) requirement.

$\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ Timing

The minimum $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ pulse widths are specified by $t_{RAS(min)}$ and $t_{CAS(min)}$ respectively. These minimum pulse widths must be satisfied for proper device operation and data integrity. Once a cycle is initiated by bringing $\overline{\text{RAS}}$ low, it must not be aborted prior to satisfying the minimum $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ pulse widths. In addition, a new cycle must not begin until the minimum $\overline{\text{RAS}}$ precharge time, t_{RP}, has been satisfied. Once a cycle begins, internal clocks and other circuits within the 21010 begin a complex sequence of events. If the sequence is broken by violating minimum timing requirements, loss of data integrity can occur.

Read

A read cycle is achieved by maintaining the write enable input ($\overline{\text{W}}$) high during a $\overline{\text{RAS}}$/$\overline{\text{CAS}}$ cycle. The access time is normally specified with respect to the falling edge of $\overline{\text{RAS}}$. But the access time also depends on the falling edge of $\overline{\text{CAS}}$ and on the valid column address transition.

If $\overline{\text{CAS}}$ goes low before $t_{RCD(max)}$ and if the column address is valid before $t_{RAD(max)}$, then the access time to valid data is specified by $t_{RAC(min)}$. However, if $\overline{\text{CAS}}$ goes low after $t_{RCD(max)}$ or if the column address becomes valid after $t_{RAD(max)}$, the access time is specified by t_{CAC} or t_{AA}. In order to achieve the minimum access time, $t_{RAC(min)}$, it is necessary to meet both $t_{RCD(max)}$ and $t_{RAD(max)}$.

Write

The 21010 can perform early write, late write and read-modify-write cycles. The difference between these cycles is in the state of data-out and is determined by the timing relationship between $\overline{\text{W}}$ and $\overline{\text{CAS}}$. In any type of write cycle, Data-in must be valid at or before the falling edge of $\overline{\text{W}}$ or $\overline{\text{CAS}}$, whichever is later.

Early Write: An early write cycle is performed by bringing $\overline{\text{W}}$ low before $\overline{\text{CAS}}$. The data at the data input pin (D) is written into the addressed memory cell. Throughout the early write cycle the output remains in the Hi-Z state. This cycle is good for common I/O applications because the data-in and data-out pins may be tied together without bus contention.

Read-Modify-Write: In this cycle, valid data from the addressed cell appears at the output before and during the time that data is being written into the same cell location. This cycle is achieved by bringing $\overline{\text{W}}$ low after $\overline{\text{CAS}}$ and meeting the data sheet read-modify-write cycle timing requirements. This cycle requires using a separate I/O to avoid bus contention.

Late Write: If $\overline{\text{W}}$ is brought low after $\overline{\text{CAS}}$, a late write cycle will occur. The late write cycle is very similar to the read-modify-write cycle except that the timing parameters, t_{RWD}, t_{CWD}, and t_{AWD}, are not necessarily met. The state of data-out is indeterminate since the output can be either Hi-Z or contain data depending on the timing conditions. This cycle requires a separate I/O to avoid bus contention.

Data Output

The 21010 has a tri-state output buffer which is controlled by $\overline{\text{CAS}}$. Whenever $\overline{\text{CAS}}$ is high (V_{IH}) the output is in the high impedance (Hi-Z) state. In any cycle in which valid data appears at the output, the output goes into the low impedance state in a time specified by t_{CLZ} after the falling edge of $\overline{\text{CAS}}$. Invalid data may be present at the output during the time after t_{CLZ} and before the valid data appears at the output. The timing parameters t_{CAC}, t_{RAC}, and t_{AA} specify when the valid data will be present at the output. The valid data remains at the output until $\overline{\text{CAS}}$ returns high. This is true even if a new $\overline{\text{RAS}}$ cycle occurs (as in hidden refresh). Each of the 21010 operating cycles is listed below after the corresponding output state produced by the cycle.

Valid Output Data: Read, Read-Modify-Write, Hidden Refresh, Fast Page Mode Read, Fast Page Mode Read-Modify-Write.

High-Z Output State: Early Write, $\overline{\text{RAS}}$-only Refresh, Fast Page Mode Write, $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ Refresh, $\overline{\text{CAS}}$-only Cycle.

Indeterminate Output State: Delayed Write.

Refresh

The data in the 21010 is stored on a tiny capacitor within each memory cell. Due to leakage the data may leak off after a period of time. To maintain data integrity, it is necessary to refresh each of the rows every 8 ms. Either a burst refresh or distributed refresh may be used. There are several ways to accomplish this.

$\overline{\text{RAS}}$-only Refresh: This is the most common method for performing refresh. It is performed by strobing in a row address with $\overline{\text{RAS}}$ while $\overline{\text{CAS}}$ remains high. This cycle must be repeated for each of the 512 row addresses, (A0–A8). The state of address A9 is ignored during refresh.

$\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ Refresh: The 21010 has $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ on-chip refresh capability that eliminates the need for external refresh addresses. If $\overline{\text{CAS}}$ is held low for the specified setup time (t_{CSR}) before $\overline{\text{RAS}}$ goes low, the on-chip refresh circuitry is enabled. An internal refresh operation automatically occurs. The refresh address is supplied by the on-chip refresh address counter, which is then internally incremented in preparation for the next $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh cycle.

Hidden Refresh: A hidden refresh cycle may be performed while maintaining the latest valid data at the output by extending the $\overline{\text{CAS}}$ active time and cycling $\overline{\text{RAS}}$. The 21010 hidden refresh cycle is actually a $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh cycle within an extended read cycle. The refresh row address is provided by the on-chip refresh address counter.

Other Refresh Methods: It is also possible to refresh the 21010 by using read, write, or read-modify-write cycles. Whenever a row is accessed, all the cells in that row are automatically refreshed. There are certain applications in which it might be advantageous to perform refresh in this manner but in general $\overline{\text{RAS}}$-only or $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh is the preferred method.

$\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ Refresh Counter Test Cycle

A special timing sequence using the $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh counter test cycle provides a convenient method of verifying the functionality of the $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh activated circuitry. The cycle begins as a $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh operation. Then, if $\overline{\text{CAS}}$ is brought high and then low again while $\overline{\text{RAS}}$ is held low, the read and write operations are enabled. In this mode, the row address bits A0 through A8 are supplied by the on-chip refresh counter. The A9 bit is set high internally.

Fast Page Mode

The 21010 has Fast Page mode capability, which provides high speed read, write, or read-modify-write access to all memory cells within a selected row. These cycles may be mixed in any order. A fast page mode cycle begins with a normal cycle. Then, while $\overline{\text{RAS}}$ is kept low to maintain the row address, $\overline{\text{CAS}}$ is cycled to strobe in additional column addresses. This eliminates the time required to set up and strobe sequential row addresses for the same page.

Power-Up

If $\overline{\text{RAS}} = V_{SS}$ during power-up, the 21010 could begin an active cycle. This condition results in higher than necessary current demands from the power supply during power-up. It is recommended that $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ track with V_{CC} during power-up or be held at a valid V_{IH} in order to minimize the power-up current.

An initial pause of 200 μs is required after power-up, followed by 8 initialization cycles before proper device operation is assured. Eight initialization cycles are also required after any 8 ms period in which there are no $\overline{\text{RAS}}$ cycles. An initialization cycle is any cycle in which $\overline{\text{RAS}}$ is cycled.

Termination

The lines from the TTL driver circuits to the 21010 inputs act like unterminated transmission lines resulting in significant positive and negative overshoots at the inputs. To minimize overshoot it is advisable to terminate the input lines and to keep them as short as possible. Although either series or parallel termination may be used, series termination is generally recommended since it is simple and draws no additional power. It consists of a resistor in series with the input line placed close to the 21010 input pin. The optimum value depends on the board layout. It must be determined experimentally and is ususally in the range of 20Ω to 40Ω.

Board Layout

It is important to lay out the power and ground lines on memory boards in such a way that switching transient effects are minimized. The recommended methods are gridded power and ground lines or separate power and ground planes. The power and ground lines act like transmission lines to the high frequency transients generated by DRAMs. The impedance is minimized if all the power supply traces to all the DRAMs run both horizontally and vertically and are connected at each intersection, or better yet, if power and ground planes are used.

Address and control lines should be as short as possible to avoid skew. In boards with many DRAMs, these lines should fan out from a central point like a fork or comb, rather than being connected in a serpentine pattern. Also, the control logic should be centrally located on large memory boards to facilitate the shortest possible address and control lines to all the DRAMs.

Decoupling

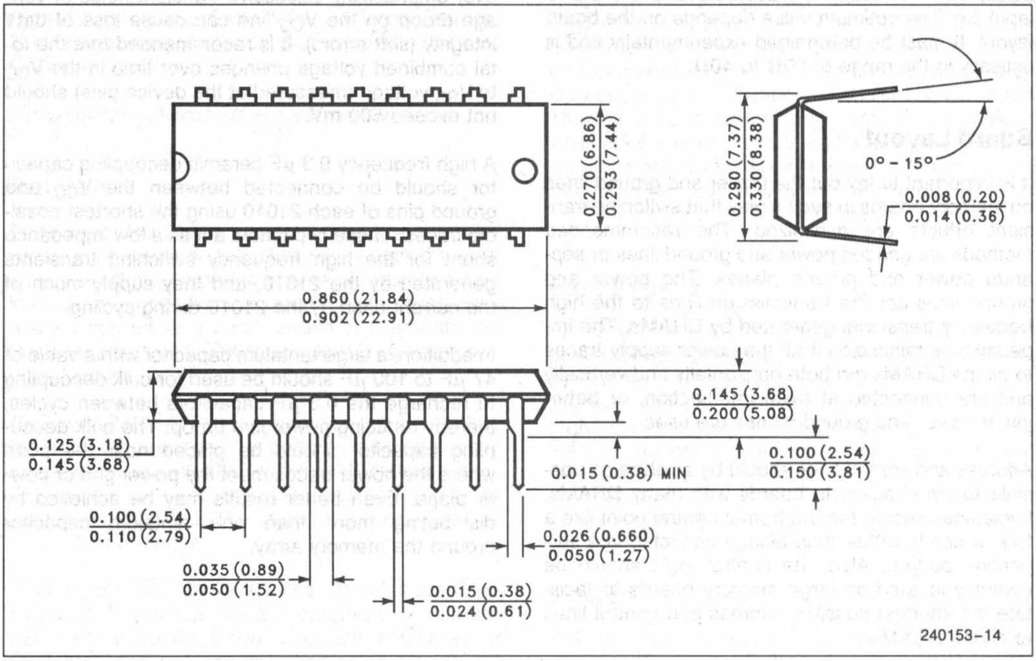
The importance of proper decoupling can not be over emphasized. Excessive transient noise or voltage droop on the V_{CC} line can cause loss of data integrity (soft errors). It is recommended that the total combined voltage changes over time in the V_{CC} to V_{SS} voltage (measured at the device pins) should not exceed 500 mV.

A high frequency 0.3 μF ceramic decoupling capacitor should be connected between the V_{CC} and ground pins of each 21010 using the shortest possible traces. These capacitors act as a low impedance shunt for the high frequency switching transients generated by the 21010, and they supply much of the current used by the 21010 during cycling.

In addition, a large tantalum capacitor with a value of 47 μF to 100 μF should be used for bulk decoupling to recharge the 0.3 μF capacitors between cycles, thereby reducing power line droop. The bulk decoupling capacitor should be placed near the point where the power traces meet the power grid or power plane. Even better results may be achieved by distributing more than one tantalum capacitor around the memory array.

PACKAGE DIMENSIONS

18-LEAD PLASTIC DUAL IN-LINE PACKAGE (P) inch (mm)



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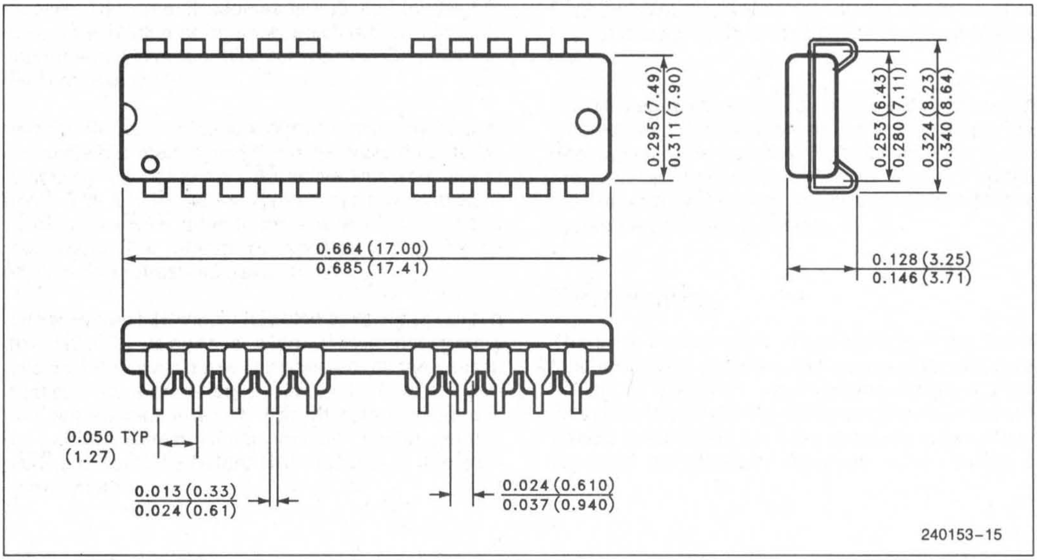
20-LEAD PLASTIC SMALL OUT-LINE J-LEAD (T) inch (mm)



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REVISION SUMMARY

1. Updated 21010-07 and 21010-08 AC Characteristics