TELEDYNE SEMICONDUCTOR

TSC701AM
Bus Compatible Four Digit LED Display Driver
• High Segment Drive Current
• Input Data Latches

General Description

The TSC701AM is a CMOS direct drive, four digit, seven segment LED display decoder and driver. The device is bus compatible making microprocessor controlled displays possible. Two chip select signals control data and digit select code latching prior to decoding and display. External data latches are unnecessary.

The TSC701AM drives common anode LED displays with 28 high current, open-drain N channel output transistors. Four seven segment LED displays may be driven. Drive current is guaranteed to be 11 mA minimum (18 mA TYP). This is twice the minimum drive current available from comparable devices and will provide high LED luminance. High luminous intensity is an important factor when a dark contrasting background is unavailable or the LED is viewed at a distance. The TSC701AM current capability makes it an ideal large character LED driver.

Four data bit inputs and four digit select signals permit interfacing to multiplexed BCD or binary output devices. The four bit data input is decoded into the seven segment alphanumeric code known as "Code B". A 0 to 9, —, E, H, L, P or "blank" reading may be displayed.

An added feature is the brightness control input that adjusts segment drive current. The control pin may also be used as a digital display enable. The TSC701AM is an improved pin compatible and functional equivalent to the ICM7212AM.

Features

- 28 Current Limited Outputs Drive Common-Anode LEDs at 18 mA Per Segment.
- Input and Digit Select Data Latches.
- Brightness Input Allows Potentiometer Control of LED Segment Current. Pin Also Serves as Digital Display Enable.
- Input and Digit Select Data Latches.
- Pin Compatible and Functionally Equivalent to ICM7212AM.
- Input Decoded to Seven Segment Code B Output (0 to 9, —, E, H, L, P, "Blank")

Ordering Information

Part No.	Package	Temp. Range	LED Segment Current	Output Code
TSC701AMIJL	40-Pin CerDIP	-25°C to +85°C	18 mA	Code B

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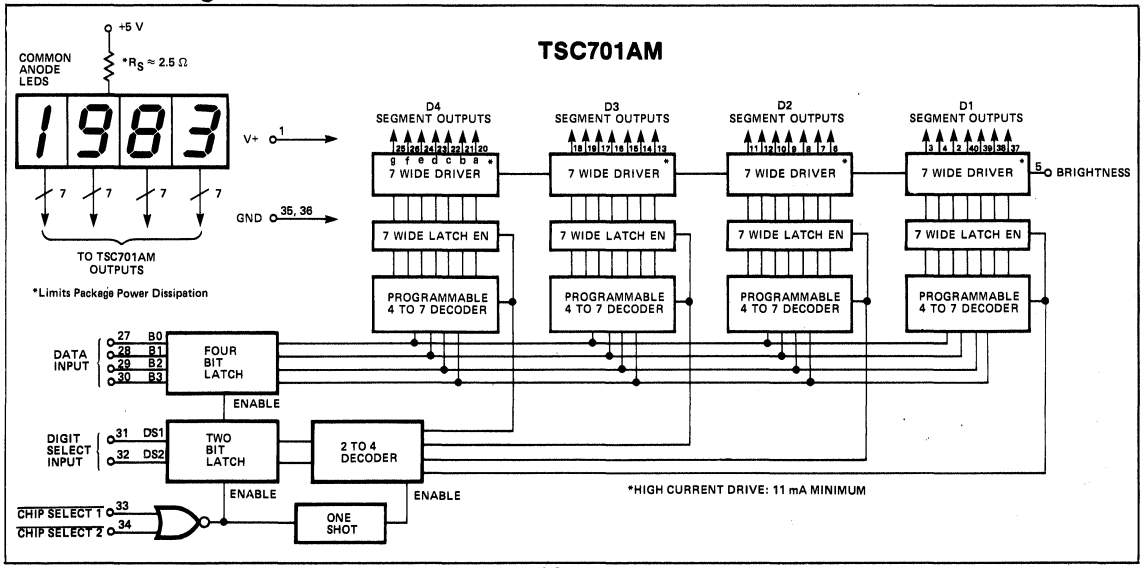
Functional Diagram



Absolute Maximum Ratings

Power Dissipation ..... 1.0 W
Supply Voltage ..... 6.5 V
Input Voltage (Any Terminal) V_S + 0.3 V to Ground -0.3 V
Operating Temperature
I Version ..... -25°C to +85°C

Maximum Chip Temperature ..... +150°C
Storage Temperature ..... -55°C to +150°C
Lead Temperature (10 Sec) ..... 300°C

Electrical Characteristics: Specifications measured with V_S = 5.0 V at T_A = 25°C.

TYPE	NO.	SYMBOL	PARAMETER	TEST CONDITIONS	TSC701AM MIN	TYP	MAX	UNIT
LED DRIVER	1	I_{SEG}	Segment ON Current	Test Circuit	11	18	20	mA
	2	I_{SLK}	Segment Leakage		—	±0.01	±1.0	µA
INPUT	3	V_{IH}	Logic "1" Input Voltage		3.0	—	—	V
	4	V_{IL}	Logic "0" Input Voltage		—	—	1.0	V
	5	I_{IN}	Input Current	Pins 27-34, 5	—	±0.01	±1.0	µA
	6	C_{IN}	Digital Input Capacitance	Pins 27-34	—	5	—	pF
	7	C_{BR}	Brightness Input Capacitance		—	200	—	pF
TIMING	8	t_{CSA}	Chip Select Active Pulse Width	Note 3	200	—	—	ns
	9	t_{DS}	Data Setup Time		100	—	—	ns
	10	t_{DH}	Data Hold Time		10	0	—	ns
	11	t_{ICS}	Inter-Chip Select Time		2	—	—	µs
POWER	12	V_S	Operating Supply Voltage Range		4	5	6	V
	13	I_S	Supply Current	Display OFF	—	—	50	µA
	14	I_{op}	Operating Current	Pin 5, at V_S^+ Display all "8's"	—	504	—	mA

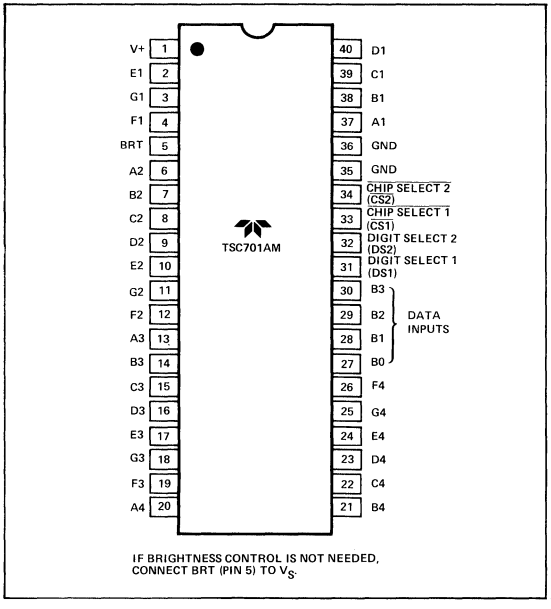
Notes:
1. Functional operation above the absolute maximum stress ratings is not implied.
2. Static Sensitive device. Unused devices must be stored in conductive material to protect devices from static discharge and static fields.
3. Other chip select ($\overline{CS}$) is either held at logic zero or both $\overline{CS1}$ and $\overline{CS2}$ driven together.

Input Definitions

In this table, V + and GROUND are considered to be normal operating input logic levels. For lowest power consumption, input signals should swing over the full supply.

INPUT	TERMINAL	CONDITION	FUNCTION	
B0	27	V + Logical One GND = Logical Zero	Ones (Least Significant)	Data Input Bits
B1	28	V+ = Logical One GND = Logical Zero	Twos	
B2	29	V+ = Logical One GND = Logical Zero	Fours	
B3	30	V+ = Logical One GND = Logical Zero	Eights (Most Significant)	
DS1	31	V+ = Logical One	Digit Select Inputs DS2, DS1 = 00 Selects D4 DS2, DS1 = 01 Selects D3 DS2, DS1 = 10 Selects D2 DS2, DS1 = 11 Selects D1	
DS2	32	GND = Logical Zero		
$\overline{CS1}$	33	V+ = Inactive	When both $\overline{CS1}$ and $\overline{CS2}$ are low the data and digit select input latches are open or enabled. On the rising of $\overline{CS1}$ or $\overline{CS2}$ data is latched, decoded and stored in the output drive latches.	
$\overline{CS2}$	34	GND = Active		

Pin Configuration



Timing Diagram

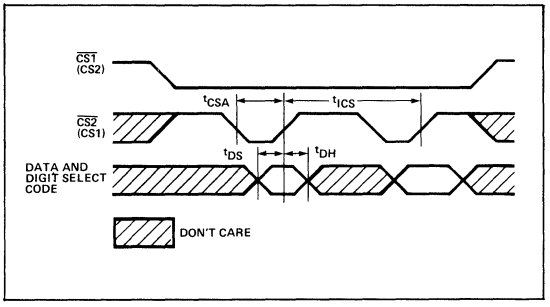


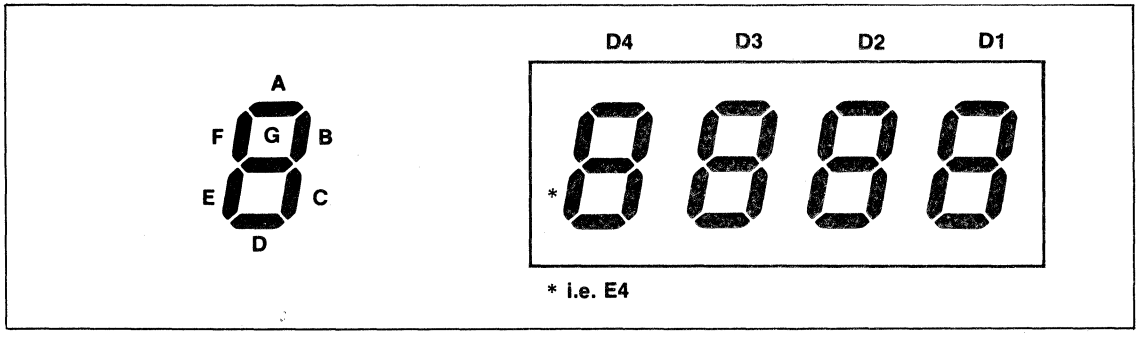
Figure 1: BUS Interface Timing Diagram

Output Definitions

Output pins are defined by the alphabetical segment assignment and numerical digital assignment.

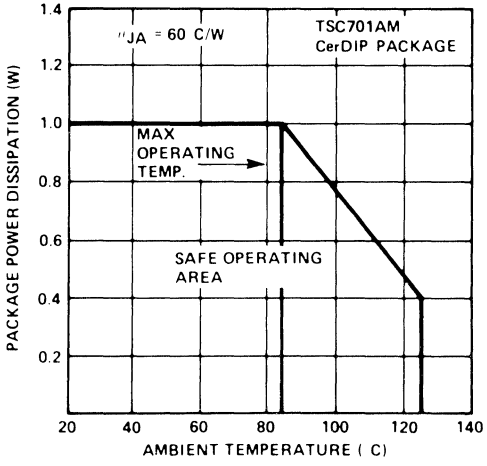
OUTPUT	TERMINAL	FUNCTION	OUTPUT	TERMINAL	FUNCTION
A1	37	A Segment Dr. Digit 1 (LSD)	A3	13	A Segment Dr. Digit 3
B1	38	B	B3	14	B
C1	39	C	C3	15	C
D1	40	D	D3	16	D
E1	2	E	E3	17	E
F1	4	F	F3	19	F
G1	3	G	G3	18	G
A2	6	A Segment Dr. Digit 2	A4	20	A Segment Dr. Digit 4 (MSD)
B2	7	B	B4	21	B
C2	8	C	C4	22	C
D2	9	D	D4	23	D
E2	10	E	E4	24	E
F2	12	F	F4	26	F
G2	11	G	G4	25	G

Digit Assignment

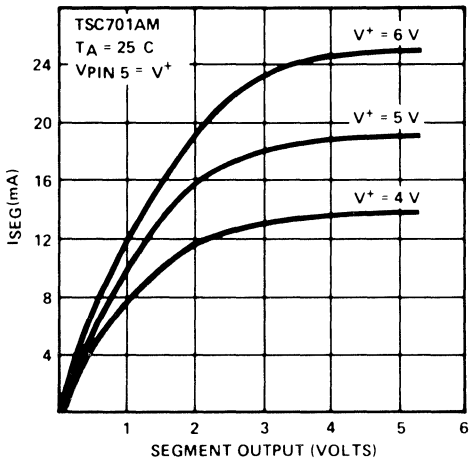


Electrical Operating Characteristics

Maximum Power Dissipation



LED Segment Current vs Output Voltage



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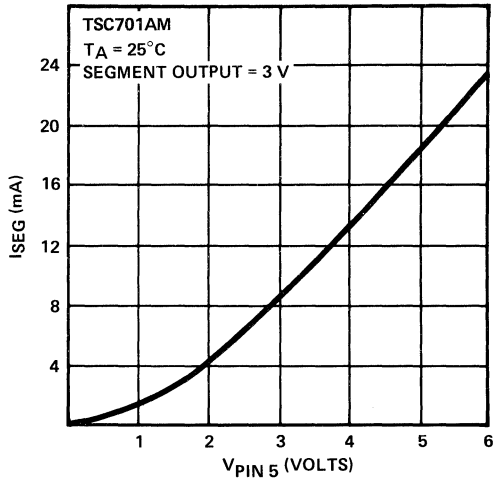
LED Segment Current vs Brightness Control Voltage



Input Configuration and Output Codes

The TSC701AM accepts a four bit, true binary (positive level = logic 1) input at pins 27 (LSB) through 30 (MSB). The output display format is 0 to 9, —, E, H, L, P and blank (see Table 1). The TSC701AM correctly decodes binary and BCD true codes to a seven segment output.

The TSC701AM is designed to interface with a data bus and display data under microprocessor control. Four data input bits (Pins 27-30) and two digit select input bits (Pins 31, 32) are written into input buffer latches. The rising edge of either chip select causes data to be latched, decoded and stored in the selected digit output data latch. The two bit digit code selects the appropriate output digit latch. The four bit display data word is decoded to the "Code B" seven segment output format.

For applications where bus compatibility is not required refer to the TSC7211A (LCD), TSC7212A (LED) and the TSC700A (LED) four digit decoder driver data sheets. These devices are designed to accept multiplexed BCD/Binary input data for display under the control of four separate digit select control signals.

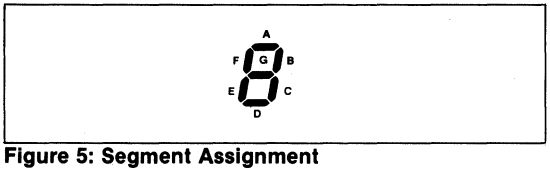


Figure 5: Segment Assignment

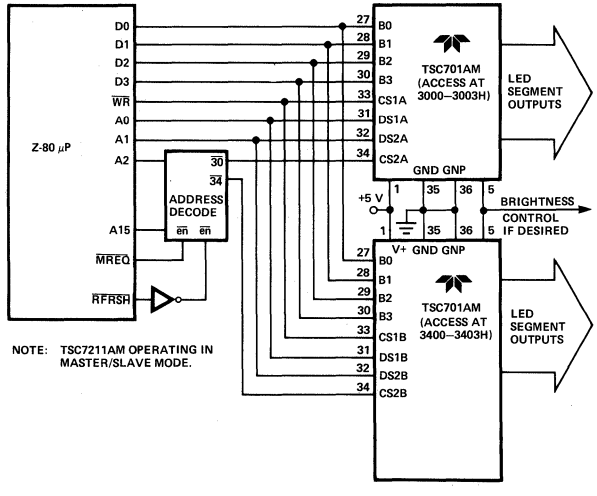
BINARY INPUT				CODE B TSC701AM
B3	B2	B1	B0	
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8
1	0	0	1	9
1	0	1	0	—
1	0	1	1	E
1	1	0	0	H
1	1	0	1	L
1	1	1	0	P
1	1	1	1	(Blank)

Table 1: Output Code

Applications Information

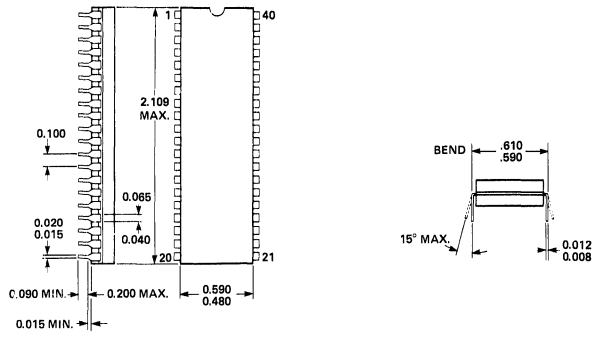
The TSC701AM has two ground pins. These pins should be connected together.

TSC701AM Interfaced to Z-80 Microprocessor



Package Information

40-Pin CerDIP
(Package #20)



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