KS54HCTLS/KS74HCTLS 640/643/645

Octal Bus Transceivers with 3-State Outputs

FEATURES

- **Function, pin-out, speed and drive compatibility with 54/74LS logic family**
- **Low power consumption characteristic of CMOS**
- **3-State outputs with high drive current (I_{OL} = 24 mA @ V_{OL} = 0.5V) for direct bus interface**
- **Inputs and outputs interface directly with TTL, NMOS and CMOS devices**
- **Wide operating voltage range: 4.5V to 5.5V**
- **Characterized for operation over industrial and military temperature ranges:**
  KS74HCTLS: −40°C to +85°C
  KS54HCTLS: −55°C to +125°C
- Package options include "small outline" packages (Available Tape & Reel), standard DIPs.

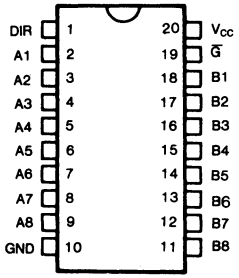
DESCRIPTION

These high-speed octal/bus transceivers are designed for asynchronous two-way communication between data buses. A direction control input (DIR) controls the flow direction of data. When DIR is high, data flows from the A inputs to the B outputs. When DIR is low, data flows from B to A. The '643 transfers inverted data from the A bus to the B bus and non-inverted data from the B bus to the A bus. The '640 transfers inverted data in both directions.

These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

PIN CONFIGURATION



FUNCTION TABLE

Control Inputs		Operation		
$\overline{G}$	DIR	'640	'643	'645
L	L	Inverted data transmitted from Bus B to Bus A	Data transmitted from Bus B to Bus A	Data transmitted from Bus B to Bus A
L	H	Inverted data transmitted from Bus A to Bus B	Inverted data transmitted from Bus A to Bus B	Data transmitted from Bus A to Bus B
H	X	Buses isolated (High-impedance state)	Buses isolated (High-impedance state)	Buses isolated (High-impedance state)

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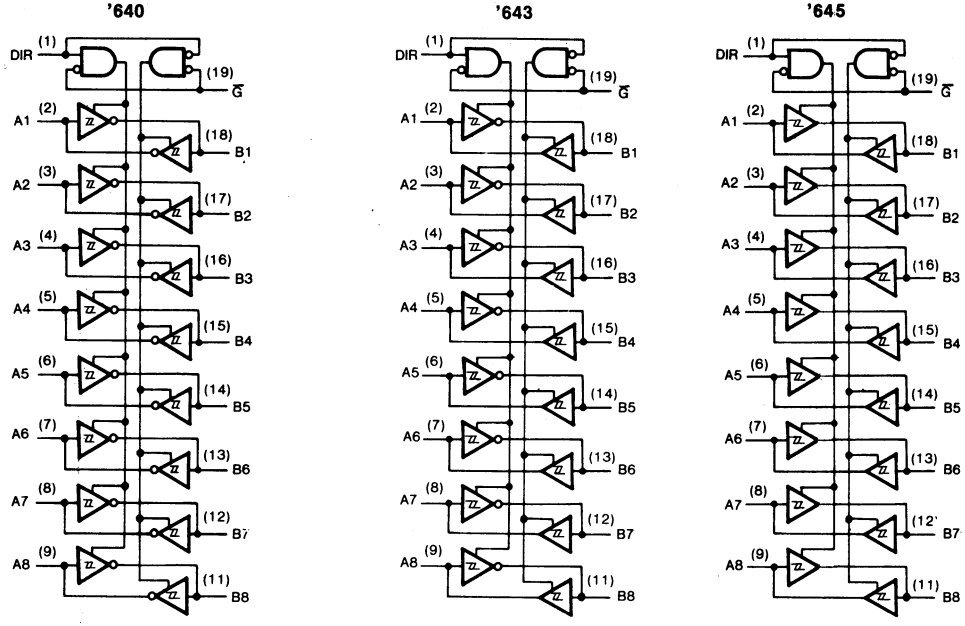
LOGIC DIAGRAMS



Absolute Maximum Ratings*

Supply Voltage Range V_{CC}, ... −0.5V to +7V
DC Input Diode Current, I_{IK}
($V_I < -0.5V$ or $V_I > V_{CC} + 0.5V$) . . . . . ±20 mA
DC Output Diode Current, I_{OK}
($V_O < -0.5V$ or $V_O > V_{CC} + 0.5V$) . . . . ±20 mA
Continuous Output Current Per Pin, I_O
($-0.5V < V_O < V_{CC} + 0.5V$) . . . . . ±70 mA
Continuous Current Through
V_{CC} or GND pins . . . . . ±250 mA
Storage Temperature Range, T_{stg} . . . −65°C to +150°C
Power Dissipation Per Package, P_d† . . . . . 500 mW

* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:
Plastic Package (N): −12mW/°C from 65°C to 85°C

Recommended Operating Conditions

Supply Voltage, V_{CC} . . . . . 4.5V to 5.5V
DC Input & Output Voltages*, V_{IN}, V_{OUT} . . 0V to V_{CC}
Operating Temperature
Range KS74HCTLS: −40°C to +85°C
KS54HCTLS: −55°C to +125°C
Input Rise & Fall Times, t_r, t_f . . . . . Max 500 ns

Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T_a=25°C	KS74HCTLS T_a=−40°C to +85°C	KS54HCTLS T_a=−55°C to +125°C	Unit
			Typ	Guaranteed Limits		
Minimum High-Level Input Voltage	V_{IH}			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	V_{IL}			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	V_{OH}	V_{IN}=V_{IH} or V_{IL} I_O=−20μA I_O=−6mA	V_{CC} 4.2	V_{CC} −0.1 3.98	V_{CC} −0.1 3.84	V_{CC} −0.1 3.7	V
Maximum Low-Level Output Voltage	V_{OL}	V_{IN}=V_{IH} or V_{IL} I_O=20μA I_O=12mA I_O=24mA	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	I_{IN}	V_{IN}=V_{CC} or GND		±0.1	±1.0	±1.0	μA
Maximum 3-State Leakage Current	I_{OZ}	Output Enable =V_{IH} V_{OUT}=V_{CC} or GND		±0.5	±5.0	±10.0	μA
Maximum Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND I_{OUT}=0μA		8.0	80.0	160.0	μA
Additional Worst Case Supply Current	ΔI_{CC}	per input pin V_I=2.4V other Inputs: at V_{CC} or GND I_{OUT}=0μA		2.7	2.9	3.0	mA

AC ELECTRICAL CHARACTERISTICS (Input t_r, t_f≤6 ns), HCTLS640, HCTLS643, HCTLS645

Characteristic	Symbol	Conditions†		T_a=25°C V_{CC}=5.0V	KS74HCTLS T_a=−40°C to +85°C V_{CC}=5.0V±10%	KS54HCTLS T_a=−55°C to +125°C V_{CC}=5.0V± 10%	Unit
				Typ	Guaranteed Limits		
Maximum Propagation Delay, A to B, or B to A	t_{PLH}	C_L=50pF C_L=150pF		9 12	12 15	16 21	19 25	ns
	t_{PHL}	C_L=50pF C_L=150pF		9 12	12 15	16 21	19 25	
Maximum Output Enable Time, $\overline{G}$ or DIR to A or B	t_{PZH}	R_L=1kΩ	C_L=50pF C_L=150pF	30 33	40 43	50 55	60 65	ns
	t_{PZL}		C_L=50pF C_L=150pF	30 33	40 43	50 55	60 65	
Maximum Output Disable Time, $\overline{G}$ or DIR to A or B	t_{PHZ}	R_L=1kΩ C_L=50pF		20	27	34	40	ns
	t_{PLZ}			20	27	34	40	
Maximum Input Capacitance	C_{IN}			5				pF
Maximum Output Capacitance	C_{OUT}	Output disabled		10				pF
Power Dissipation Capacitance* (per stage)	C_{PD}	$\overline{G}$=V_{CC} $\overline{G}$=GND		5 30				pF

* C_{PD} determines the no-load dynamic power dissipation: P_D=C_{PD} V_{CC}^2 f_{in}.
† For AC switching test circuits and timing waveforms see section 2.

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