

Document Title**1Mx8 bit Low Power and Low Voltage CMOS Static RAM****Revision History**

<u>Revision No.</u>	<u>History</u>	<u>Draft Date</u>	<u>Remark</u>
0.0	Initial draft	October 31, 2002	Preliminary
0.1	Revised - Deleted 44-TSOP2-400R package type.	December 11, 2002	Preliminary
1.0	Finalized - Changed Icc2 from 40mA to 30mA - Changed ISB1(industrial) from 30μA to 15μA - Changed ISB1(Automotive) from 40μA to 25μA	September 16, 2003	Final
2.0	Revised - Changed ISB1 of Automotive product from 25μA to 80μA - Changed Vcc in IDR Test Condition from 1.5V to 3.0V - Changed IDR of Industrial product from 6μA to 15μA - Changed IDR of Automotive product from 10μA to 80μA - Added Lead Free Products	March 27, 2005	Final

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CMOS SRAM

1Mx8 bit Low Power and Low Voltage full CMOS Static RAM

FEATURES

- Process Technology: Full CMOS
- Organization: 1M x8
- Power Supply Voltage: 2.7~3.6V
- Low Data Retention Voltage: 1.5V(Min)
- Three state outputs
- Package Type: 44-TSOP2-400F

GENERAL DESCRIPTION

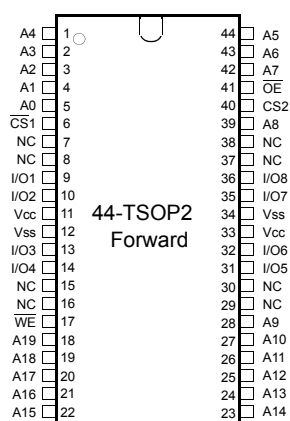
The K6X8008T2B families are fabricated by SAMSUNG's advanced full CMOS process technology. The families support various operating temperature range for user flexibility of system design. The families also support low data retention voltage for battery back-up operation with low data retention current.

PRODUCT FAMILY

Product Family	Operating Temperature	Vcc Range	Speed	Power Dissipation		PKG Type
				Standby (Isb1, Max)	Operating (Icc2, Max)	
K6X8008T2B-F	Industrial(-40~85°C)	2.7~3.6V	55 ¹⁾ /70ns	15μA	30mA	44-TSOP2-400F
K6X8008T2B-Q	Automotive(-40~125°C)		70ns	80μA		

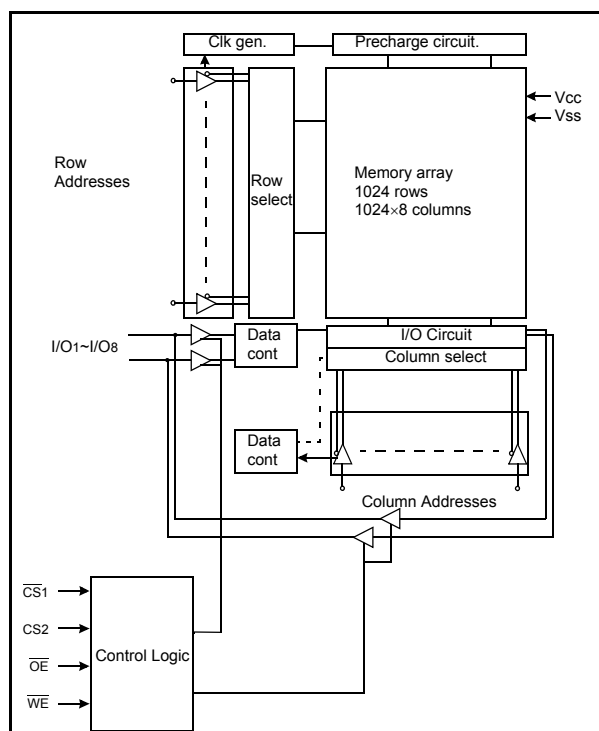
1. This parameter is measured with 50pF test load (Vcc=3.0~3.6V).

PIN DESCRIPTION



Name	Function	Name	Function
$\overline{\text{CS}}_1, \text{CS}_2$	Chip Select Inputs	Vcc	Power
$\overline{\text{OE}}$	Output Enable Input	Vss	Ground
$\overline{\text{WE}}$	Write Enable Input	A0~A19	Address Inputs
I/O ₁ ~I/O ₈	Data Inputs/Outputs	NC	No Connect

FUNCTIONAL BLOCK DIAGRAM



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PRODUCT LIST

Industrial Temperature Products(-40~85°C)		Automotive Temperature Products(-40~125°C)	
Part Name	Function	Part Name	Function
K6X8008T2B-TF55 ¹⁾	44-TSOP2-F, 55ns, LL	K6X8008T2B-TQ70	44-TSOP2-F, 70ns, L
K6X8008T2B-TF70	44-TSOP2-F, 70ns, LL	K6X8008T2B-UQ70	44-TSOP2-F, 70ns, L, LF
K6X8008T2B-UF55 ¹⁾	44-TSOP2-F, 55ns, LL, LF		
K6X8008T2B-UF70	44-TSOP2-F, 70ns, LL, LF		

1. Operating voltage range is 3.0~3.6V

2. LF : Lead Free Product

FUNCTIONAL DESCRIPTION

$\overline{CS_1}$	CS_2	$\overline{OE}$	$\overline{WE}$	I/O ₁₋₈	Mode	Power
H	X	X	X	High-Z	Deselected	Standby
X	L	X	X	High-Z	Deselected	Standby
L	H	H	H	High-Z	Output Disabled	Active
L	H	L	H	Dout	Read	Active
L	H	X	L	Din	Write	Active

Note: X means don't care. (Must be low or high state)

ABSOLUTE MAXIMUM RATINGS¹⁾

Item	Symbol	Ratings	Unit	Remark
Voltage on any pin relative to V _{SS}	V _{IN} , V _{OUT}	-0.2 to V _{CC} +0.3 (max. 3.9V)	V	-
Voltage on V _{CC} supply relative to V _{SS}	V _{CC}	-0.2 to 3.9	V	-
Power Dissipation	P _D	1.0	W	-
Storage temperature	T _{STG}	-65 to 150	°C	-
Operating Temperature	T _A	-40 to 85	°C	K6X8008T2B-F
		-40 to 125	°C	K6X8008T2B-Q

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Functional operation should be restricted to recommended operating condition. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS¹⁾

Item	Symbol	Product	Min	Typ	Max	Unit
Supply voltage	V _{CC}	K6X8008T2B Family	2.7	3.0/3.3	3.6	V
Ground	V _{SS}	All Family	0	0	0	V
Input high voltage	V _{IH}	K6X8008T2B Family	2.2	-	V _{CC} +0.3 ²⁾	V
Input low voltage	V _{IL}	K6X8008T2B Family	-0.3 ³⁾	-	0.6	V

Note:

1. Industrial Product: T_A=-40 to 85°C, otherwise specified.Automotive Product: T_A=-40 to 125°C, otherwise specified.2. Overshoot: V_{CC}+3.0V in case of pulse width ≤30ns.

3. Undershoot: -3.0V in case of pulse width ≤30ns.

4. Overshoot and undershoot are sampled, not 100% tested.

CAPACITANCE¹⁾ (f=1MHz, T_A=25°C)

Item	Symbol	Test Condition	Min	Max	Unit
Input capacitance	C _{IN}	V _{IN} =0V	-	8	pF
Input/Output capacitance	C _{IO}	V _{IO} =0V	-	10	pF

1. Capacitance is sampled, not 100% tested.

DC AND OPERATING CHARACTERISTICS

Item	Symbol	Test Conditions	Min	Typ	Max	Unit	
Input leakage current	I _{LI}	V _{IN} =V _{SS} to V _{CC}	-1	-	1	μA	
Output leakage current	I _{LO}	$\overline{CS}_1$ =V _{IH} , CS ₂ =V _{IL} or $\overline{OE}$ =V _{IH} or $\overline{WE}$ =V _{IL} , V _{IO} =V _{SS} to V _{CC}	-1	-	1	μA	
Average operating current	I _{CC1}	Cycle time=1μs, 100%duty, I _{IO} =0mA, $\overline{CS}_1$ ≤0.2V, CS ₂ ≥V _{CC} -0.2V, V _{IN} ≤0.2V or V _{IN} ≥V _{CC} -0.2V	-	-	3	mA	
	I _{CC2}	Cycle time=Min, I _{IO} =0mA, 100% duty, $\overline{CS}_1$ =V _{IL} , CS ₂ =V _{IH} , V _{IN} =V _{IL} or V _{IH}	-	-	30	mA	
Output low voltage	V _{OL}	I _{OL} = 2.1mA	-	-	0.4	V	
Output high voltage	V _{OH}	I _{OH} = -1.0mA	2.4	-	-	V	
Standby Current(TTL)	I _{SB}	$\overline{CS}_1$ =V _{IH} , CS ₂ =V _{IL} , Other inputs=V _{IH} or V _{IL}	-	-	0.4	mA	
Standby Current(CMOS)	I _{SB1}	Other input =0~V _{CC} , 1) $\overline{CS}_1$ ≥V _{CC} -0.2V, CS ₂ ≥V _{CC} -0.2V ($\overline{CS}_1$ controlled) or 2) 0V≤CS ₂ ≤0.2V(CS ₂ controlled)	K6X8008T2B-F	-	-	15	μA
		K6X8008T2B-Q	-	-	80		

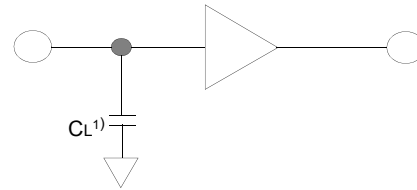
AC OPERATING CONDITIONS

TEST CONDITIONS (Test Load and Input/Output Reference)

Input pulse level: 0.4 to 2.2V

Input rising and falling time: 5ns

Input and output reference voltage: 1.5V

Output load(see right): $C_L=100\text{pF}+1\text{TTL}$ $C_L=50\text{pF}+1\text{TTL}$ 

1. Including scope and jig capacitance

AC CHARACTERISTICS ($V_{CC}=2.7\sim 3.6\text{V}$, Industrial product: $T_A=-40$ to 85°C , Automotive product: $T_A=-40$ to 125°C)

Parameter List		Symbol	Speed Bins				Units
			55ns ¹⁾		70ns		
			Min	Max	Min	Max	
Read	Read Cycle Time	t _{RC}	55	-	70	-	ns
	Address Access Time	t _{AA}	-	55	-	70	ns
	Chip Select to Output	t _{CO}	-	55	-	70	ns
	Output Enable to Valid Output	t _{OE}	-	25	-	35	ns
	Chip Select to Low-Z Output	t _{LZ}	10	-	10	-	ns
	Output Enable to Low-Z Output	t _{OLZ}	5	-	5	-	ns
	Chip Disable to High-Z Output	t _{HZ}	0	20	0	25	ns
	Output Disable to High-Z Output	t _{OHZ}	0	20	0	25	ns
	Output Hold from Address Change	t _{OH}	10	-	10	-	ns
Write	Write Cycle Time	t _{WC}	55	-	70	-	ns
	Chip Select to End of Write	t _{CW}	45	-	60	-	ns
	Address Set-up Time	t _{AS}	0	-	0	-	ns
	Address Valid to End of Write	t _{AW}	45	-	60	-	ns
	Write Pulse Width	t _{WP}	40	-	50	-	ns
	Write Recovery Time	t _{WR}	0	-	0	-	ns
	Write to Output High-Z	t _{WHZ}	0	20	0	20	ns
	Data to Write Time Overlap	t _{DW}	25	-	30	-	ns
	Data Hold from Write Time	t _{DH}	0	-	0	-	ns
	End Write to Output Low-Z	t _{OW}	5	-	5	-	ns

1. Voltage range is 3.0V~3.6V for industrial product.

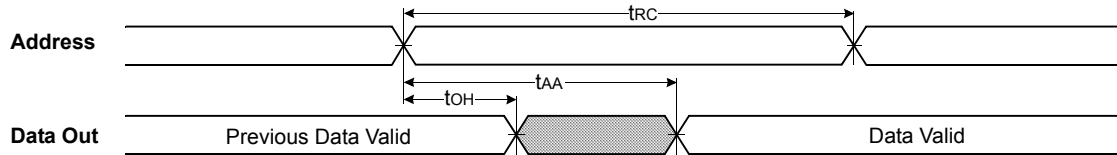
DATA RETENTION CHARACTERISTICS

Item	Symbol	Test Condition		Min	Typ	Max	Unit
V _{CC} for data retention	V _{DR}	$\overline{CS}_1 \geq V_{CC}-0.2\text{V}^{1)}$		1.5	-	3.6	V
Data retention current	I _{DR}	$V_{CC}=3.0\text{V}, \overline{CS}_1 \geq V_{CC}-0.2\text{V}^{1)}$	K6X8008T2B-F	-	-	15	μA
			K6X8008T2B-Q			80	
Data retention set-up time	t _{SDR}	See data retention waveform		0	-	-	ms
Recovery time	t _{RDR}			5	-	-	

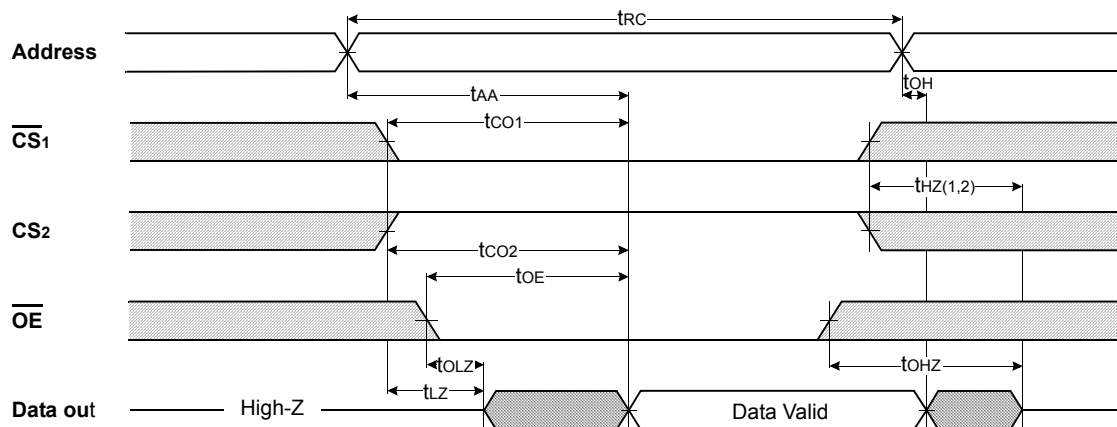
1. $\overline{CS}_1 \geq V_{CC}-0.2\text{V}, \overline{CS}_2 \geq V_{CC}-0.2\text{V}$ ($\overline{CS}_1$ controlled) or $\overline{CS}_2 \geq V_{CC}-0.2\text{V}$ ($\overline{CS}_2$ controlled).

TIMING DIAGRAMS

TIMING WAVEFORM OF READ CYCLE(1) (Address Controlled, $\overline{CS}_1 = \overline{OE} = V_{IL}$, $CS_2 = \overline{WE} = V_{IH}$)



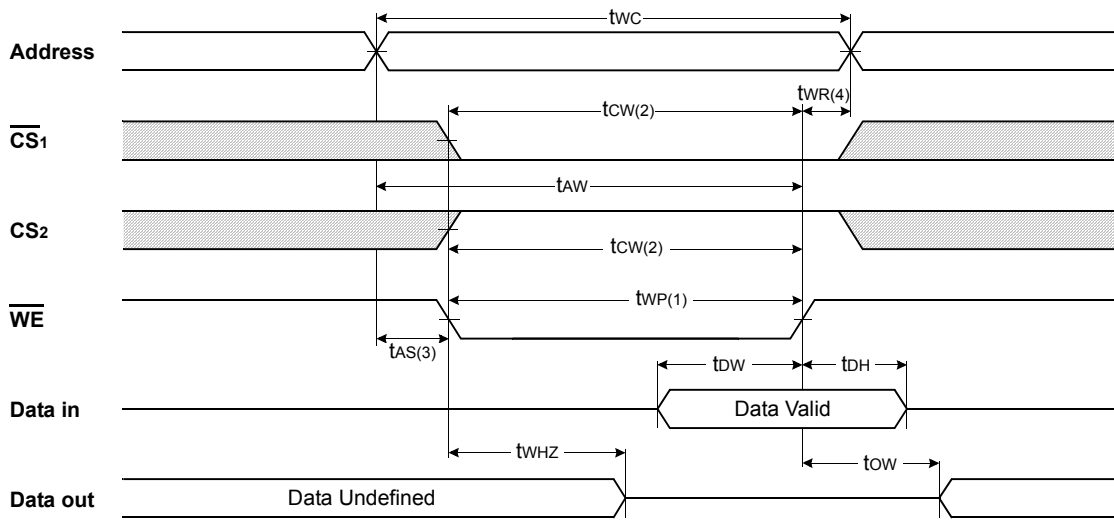
TIMING WAVEFORM OF READ CYCLE(2) ($\overline{WE} = V_{IH}$)



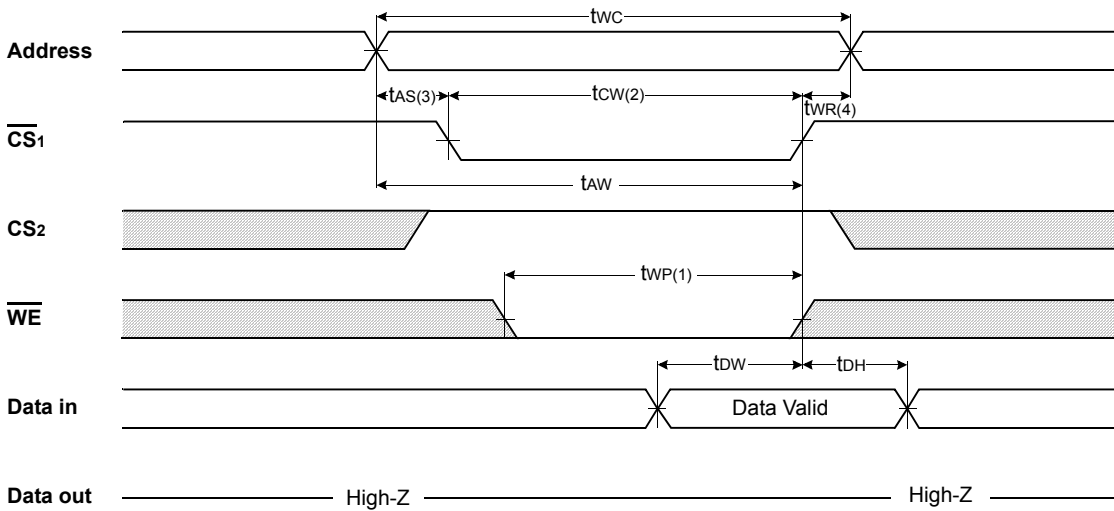
NOTES (READ CYCLE)

1. t_{HZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels.
2. At any given temperature and voltage condition, $t_{HZ}(\text{Max.})$ is less than $t_{LZ}(\text{Min.})$ both for a given device and from device to device interconnection.

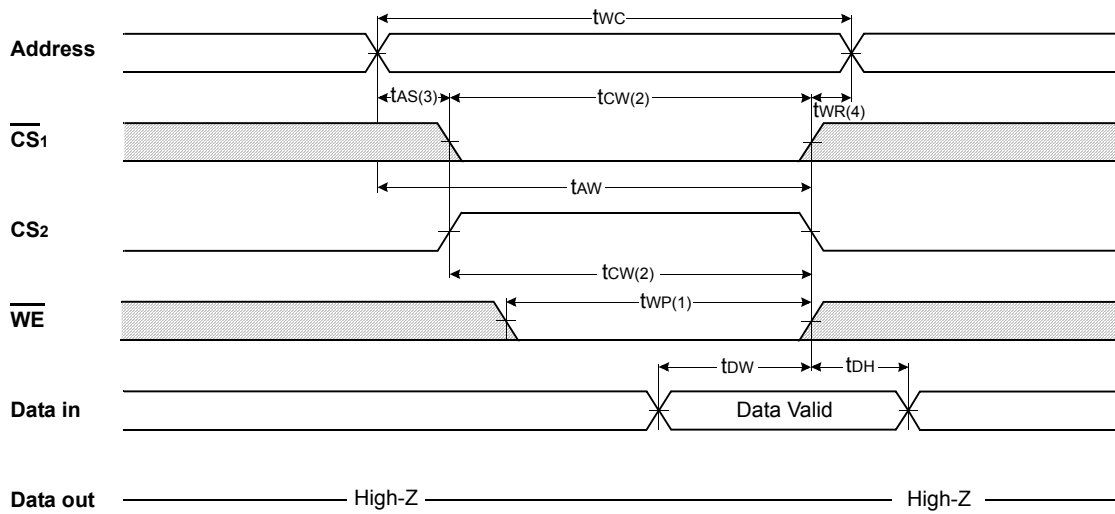
TIMING WAVEFORM OF WRITE CYCLE(1) ($\overline{WE}$ Controlled)



TIMING WAVEFORM OF WRITE CYCLE(2) ($\overline{CS_1}$ Controlled)



TIMING WAVEFORM OF WRITE CYCLE(3) (CS₂ Controlled)

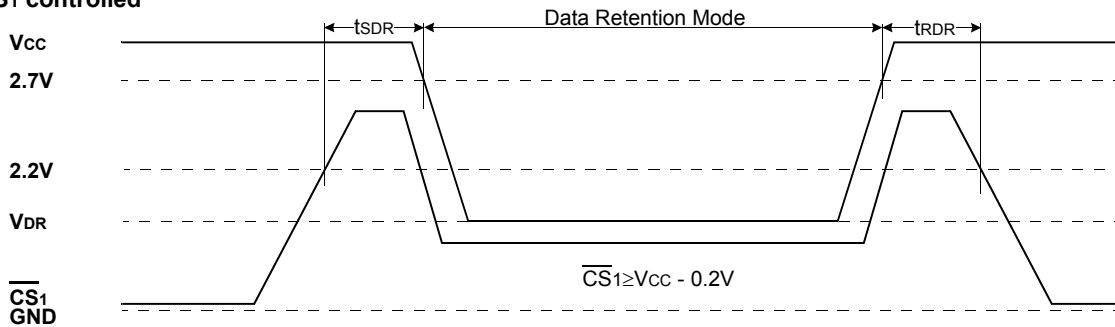


NOTES (WRITE CYCLE)

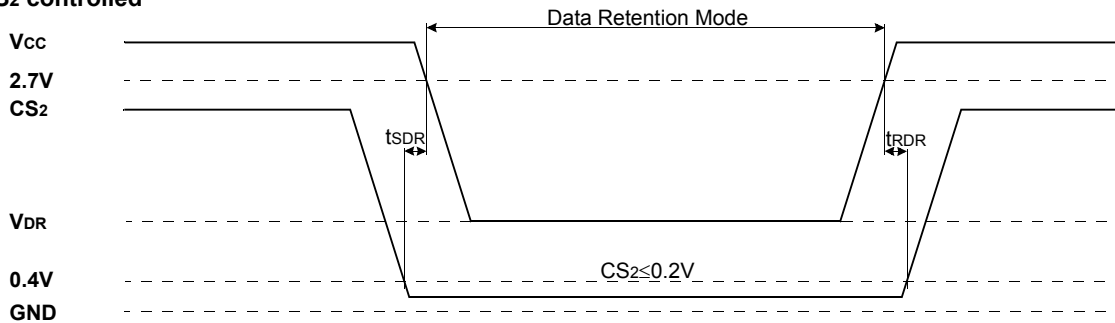
1. A write occurs during the overlap of a low $\overline{CS_1}$, a high CS₂ and a low $\overline{WE}$. A write begins at the latest transition among $\overline{CS_1}$ goes low, CS₂ going high and $\overline{WE}$ going low : A write end at the earliest transition among CS₁ going high, CS₂ going low and $\overline{WE}$ going high, tWP is measured from the beginning of write to the end of write.
2. tCW is measured from the CS₁ going low or CS₂ going high to the end of write.
3. tAS is measured from the address valid to the beginning of write.
4. tWR is measured from the end of write to the address change. tWR applied in case a write ends as $\overline{CS_1}$ or $\overline{WE}$ going high tWR2 applied in case a write ends as CS₂ going to low.

DATA RETENTION WAVE FORM

$\overline{CS_1}$ controlled



CS₂ controlled



CMOS SRAM

Unit: millimeters(inches)

THIN SMALL OUTLINE PACKAGE TYPE II (40UF)

The drawing illustrates the mechanical specifications of a Thin Small Outline Package Type II (40UF). It includes a top view, a side view, and a detail view of the lead profile.

Top View Dimensions:

- Overall width: 18.81 ± 0.10 mm (MAX. 0.741 in.)
- Width of the body: 18.41 ± 0.10 mm (MAX. 0.725 ± 0.004 in.)
- Lead pitch: 0.805 ± 0.032 mm (MAX. 0.0315 in.)
- Lead thickness: 0.35 ± 0.10 mm (MAX. 0.014 ± 0.004 in.)
- Lead width: 0.80 ± 0.0315 mm (MAX. 0.0315 in.)
- Lead spacing: 0.05 ± 0.002 mm (MIN. 0.002 in.)
- Lead length: 1.20 ± 0.047 mm (MAX. 0.047 in.)
- Lead thickness at the end: 1.00 ± 0.10 mm (MAX. 0.039 ± 0.004 in.)

Side View Dimensions:

- Overall height: 11.76 ± 0.20 mm (MAX. 0.463 ± 0.008 in.)
- Lead height: 10.16 ± 0.400 mm (MAX. 0.400 in.)
- Lead thickness: 0.25 ± 0.010 mm (MAX. 0.010 in.)
- Lead angle: $0 \sim 8^\circ$
- Lead width: $0.45 \sim 0.75$ mm (MAX. $0.018 \sim 0.030$ in.)
- Lead thickness at the end: 0.50 ± 0.020 mm (MAX. 0.020 in.)
- Lead angle at the end: 0.15 ± 0.10 mm (MAX. 0.006 ± 0.002 in.)

Detail View Dimensions:

- Lead thickness: 0.10 ± 0.004 mm (MAX. 0.004 in.)