

T-51-10-05



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TC826

A/D CONVERTER WITH BAR GRAPH DISPLAY OUTPUT

FEATURES

- Bipolar A/D Conversion
- 2.5% Resolution
- Direct LCD Display Drive
- "Thermometer" Bar or Dot Display
- 40 Data Segments Plus Zero
- Overrange Plus Polarity Indication
- Precision On-Chip Reference35 ppm/°C
- Differential Analog Input
- Low Input Leakage 10 pA
- Display Flashes on Overrange
- Display Hold Mode
- Auto-Zero Cycle Eliminates Zero Adjust Potentiometer
- 9V Battery Operation
- Low Power Consumption 1.1 mW
- 20 mV to 2.0 V Full-Scale Operation
- Non-Multiplexed LCD Drive for Maximum Viewing Angle

GENERAL DESCRIPTION

In many applications a graphical display is preferred over a digital display. Knowing a process or system operates, for example, within design limits is more valuable than a direct system variable readout. A bar or moving dot display supplies information precisely without requiring further interpretation by the viewer.

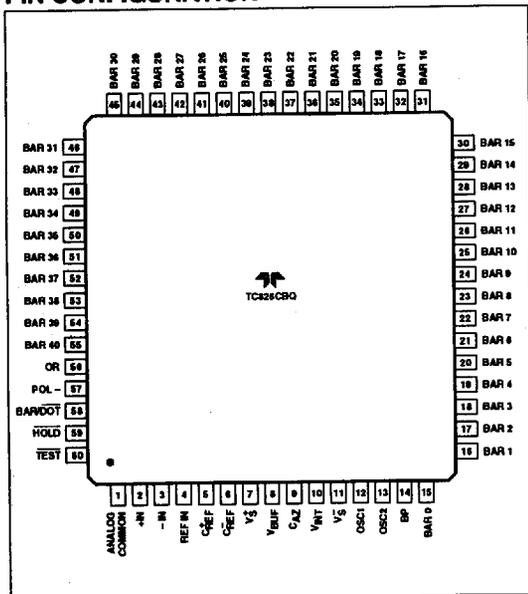
The TC826 is a complete analog-to-digital converter with direct liquid crystal (LCD) display drive. The 40 LCD data segments plus zero driver give a 2.5% resolution bar display. Full-scale differential input voltage range extends from 20 mV to 2V. The TC826 sensitivity is 500 μ V. A low drift 35 ppm/°C internal reference, LCD backplane oscillator and driver, input polarity LCD driver, and overrange LCD driver make designs simple and low cost. The CMOS design required only 125 μ A from a 9V battery. In +5V systems a TC7660 DC to DC converter can supply the -5V supply. The differential analog input leakage is a low 10 pA.

Two display formats are possible. The BAR mode display is like a "thermometer" scale. The LCD segment driver that equals the input plus all below it are on. The DOT mode activates only the segment equal to the input. In either mode the polarity signal is active for negative input signals. An overrange input signal causes the display to flash and activates the overrange annunciator. A hold mode can be selected that freezes the display and prevents updating.

The dual slope integrating conversion method with auto-zero phase maximizes noise immunity and eliminates zero-scale adjustment potentiometers. Zero-scale drift is a low 5 μ V/°C. Conversion rate is typically 5 per second and is adjustable by a single external resistor.

A compact, 0.5" square, flat package minimizes PC board area. The high pin count LSI package makes multiplexed LCD displays unnecessary. Low cost, direct drive LCD displays offer the widest viewing angle and are readily available. A standard display is available now for TC826 prototyping work.

PIN CONFIGURATION



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ORDERING INFORMATION

Part No.	Package	Temperature
TC826CBQ	60-Pin Plastic Quad Flat Package Formed Leads	0°C to 70°C

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V^+ to V^-)	15V
Analog Input Voltage (either input) ⁽¹⁾	V^+ to V^-
Package Power Dissipation	
Flat Package	500 mW
Operating Temperature	
'C' Devices	0°C to +70°C
Storage Temperature	-65°C to +150°C
Lead Temperature (Soldering, 60 sec)	300°C

Static-sensitive device. Unused devices must be stored in conductive material. Protect devices from static discharge and static fields. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to Absolute Maximum Rating Conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS:

unless otherwise stated $V_S = 9V$; $R_{OSC} = 430\text{ k}\Omega$; $T_A = 25^\circ\text{C}$; Full-Scale = 20 mV.

No.	Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
1	—	Zero Input	$V_{IN} = 0.0V$	-0	± 0	+0	Display
2	—	Zero Reading Drift	$V_{IN} = 0.0V$ $0^\circ\text{C} \leq T_A \leq 70^\circ\text{C}$	—	0.2	1	$\mu\text{V}/^\circ\text{C}$
3	NL	Linearity Error	Max Deviation From Best Straight Line	-1	0.5	+1	Count
4	—	Rollover Error	$-V_{IN} = +V_{IN}$	-1	0	+1	Count
5	EN	Noise	$V_{IN} = 0V$	—	60	—	μV_{P-P}
6	ILK	Input Leakage Current	$V_{IN} = 0V$	—	10	20	pA
7	CMRR	Common-Mode Rejection Ratio	$V_{CM} = \pm 1V$ $V_{IN} = 0V$	—	50	—	$\mu\text{V}/V$
8	—	Scale Factor Temperature Coefficient	$0 \leq T_A \leq 70^\circ\text{C}$ External Ref. Temperature Coefficient = 0 ppm/ $^\circ\text{C}$	—	1	—	ppm/ $^\circ\text{C}$
9	VCTC	Analog Common Temperature Coefficient	250 k Ω Between Common and V^+ $0^\circ\text{C} \leq T_A \leq 70^\circ\text{C}$	—	35	100	ppm/ $^\circ\text{C}$
10	—	Analog Common Voltage	250 k Ω Between Common and V_S^+	2.7	2.9	3.35	V
11	VSD	LCD Segment Drive Voltage		4	5	6	V_{P-P}
12	VBD	LCD Backplane Drive Voltage		4	5	6	V_{P-P}
13	—	Power Supply Current		—	125	175	μA

- NOTES: 1. Input voltages may exceed the supply voltages when the input current is limited to 100 μA .
2. Static sensitive device. Unused devices should be stored in conductive material to protect devices from static discharge and static fields.

3. Backplane drive is in phase with segment drive for 'off' segment and 180 $^\circ\text{C}$ out of phase for 'on' segment. Frequency is 10 times conversion rate.
4. Logic input pins 58, 59, and 60 should be connected through 1 M Ω series resistors to V_S^- for logic 0.

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PIN DESCRIPTION AND FUNCTION

Pin No.	Name	Description
1	Analog Common	Establishes the internal analog ground point. Analog common is set to 2.9V below the positive supply by an internal zener reference circuit. The voltage difference between V_S^+ and analog-common can be used to supply the TC826 voltage reference input at REF IN (Pin 4).
2	+IN	Positive analog signal input.
3	-IN	Negative analog signal input.
4	REF IN	Reference voltage positive input. Measured relative to analog-common. REF IN = Full-Scale/2.
5	CREF +	Reference capacitor connection.
6	CREF -	Reference capacitor connection.
7	V_S^+	Positive supply terminal.
8	VBUF	Buffer output. Integration resistor connection.
9	CAZ	Negative comparator input. Auto-zero capacitor connection.
10	VINT	Integrator output. Integration capacitor connection.
11	VS-	Negative supply terminal.
12	OSC1	Oscillator resistor (R_{OSC}) connection.
13	OSC2	Oscillator resistor (R_{OSC}) connection.
14	BP	LCD Backplane driver.
15	BAR 0	LCD Segment driver: Bar 0
16	1	1
17	2	2
18	3	3
19	4	4
20	5	5
21	6	6
22	7	7
23	8	8
24	9	9
25	10	10
26	11	11
27	12	12
28	13	13
29	14	14
30	15	15
31	16	16
32	17	17
33	18	18
34	19	19
35	20	20
36	21	21
37	22	22
38	23	23
39	24	24
40	25	25
41	26	26
42	27	27
43	28	28

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PIN DESCRIPTION AND FUNCTION (Cont.)

Pin No.	Name	Description
44	BAR 29	LCD Segment driver: Bar 29
45	30	30
46	31	31
47	32	32
48	33	33
49	34	34
50	35	35
51	36	36
52	37	37
53	38	38
54	39	39
55	40	40
56	OR	LCD segment driver that indicated input out-of-range condition.
57	POL-	LCD segment driver that indicates input signal is negative.
58	BAR / DOT	Input logic signal that selects bar or dot display format. Normally in bar mode. Connect to V_S^- through 1MΩ resistor for Dot format.
59	HOLD	Input logic signal that prevents display from changing. Pulled high internally to inactive state. Connect to V_S^- through 1MΩ series resistor for HOLD mode operation.
60	TEST	Input logic signal. Sets TC805 to BAR display mode. Bar 0 to 40, plus OR flash on and off. The POL-LCD driver is on. Pulled high internally to inactive state. Connect to V_S^- with 1 MΩ series resistor to activate.

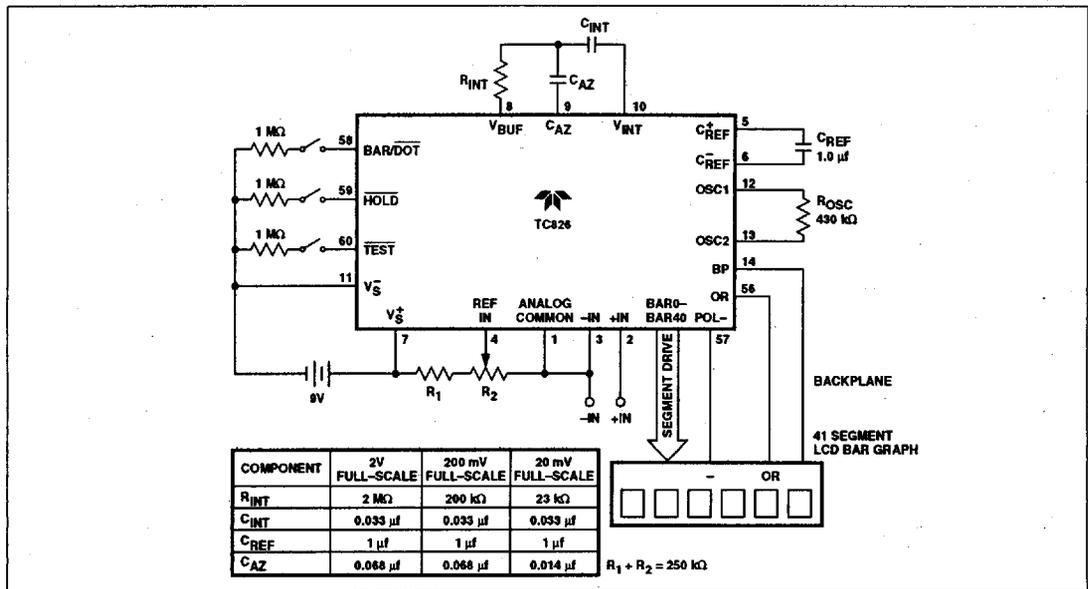


Figure 1 Typical TC826 Circuit Connection

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DUAL SLOPE CONVERSION PRINCIPLES

The TC826 is a dual slope, integrating analog-to-digital converter. The conventional dual slope converter measurement cycle has two distinct phases:

- Input Signal Integration
- Reference Voltage Integration (Deintegration)

The input signal being converted is integrated for a fixed time period (TSI). Time is measured by counting clock pulses. An opposite polarity constant reference voltage is then integrated until the integrator output voltage returns to zero. The reference integration time is directly proportional to the input signal (TRI). (Figure 2).

In a simple dual slope converter a complete conversion requires the integrator output to 'ramp-up' and 'ramp-down'.

A simple mathematical equation relates the input signal reference voltage and integration time:

$$\frac{1}{RC} \int_0^{T_{SI}} V_{IN}(t) dt = \frac{V_R T_{RI}}{RC}$$

Where:

V_R = Reference Voltage

V_{SI} = Signal Integration Time (Fixed)

T_{RI} = Reference Voltage Integration Time (Variable)

For a constant V_{IN} : $V_{IN} = V_R \frac{T_{RI}}{T_{SI}}$

The dual slope converter accuracy is unrelated to the integrating resistor and capacitor values as long as they are stable during a measurement cycle. An inherent benefit is noise immunity. Noise spikes are integrated or averaged to zero during the integration periods. Integrating ADCs are immune to the large conversion errors that plague successive approximation converters in high noise environments. Interfering signals with frequency components at multiples of the averaging period will be attenuated. (Figure 3.)

The TC826 converter improves the conventional dual slope conversion technique by incorporating an auto-zero phase. This phase eliminates zero-scale offset errors and drift. A potentiometer is not required to obtain a zero output for zero input.

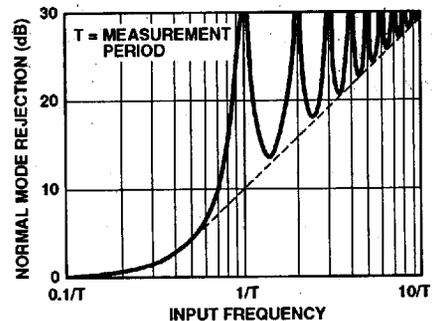


Figure 3 Normal-Mode Rejection of Dual Slope Converter

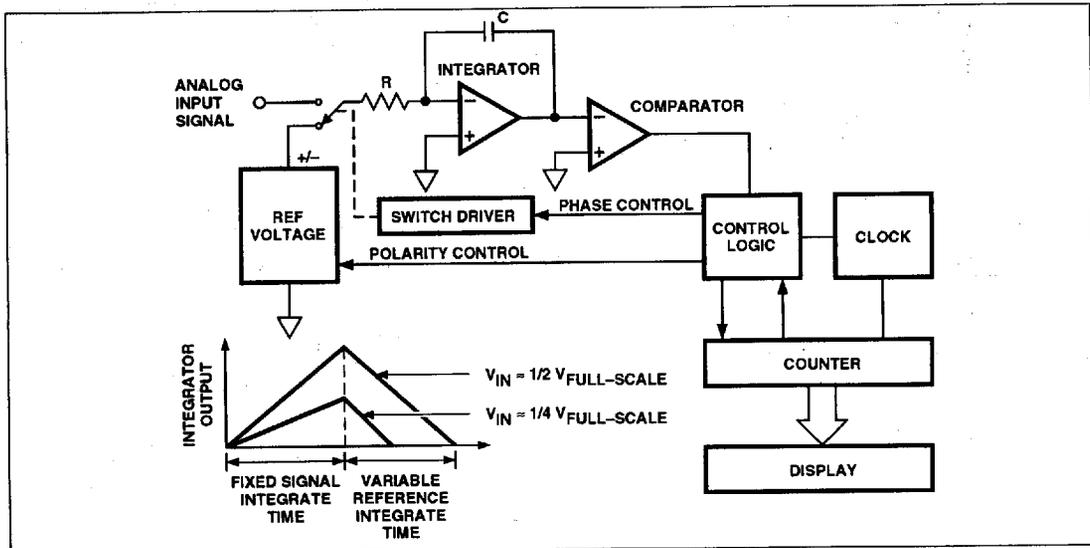


Figure 2 Basic Dual Slope Converter

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THEORY OF OPERATION

Analog Section

In addition to the basic signal integrate and deintegrate cycles discussed above, the TC826 incorporates an auto-zero cycle. This cycle removes buffer amplifier, integrator, and comparator offset voltage error terms from the conversion. A true digital zero reading results without external adjusting potentiometers. A complete conversion consists of three cycles: an auto-zero, signal integrate and reference cycle. (Figures 4 and 5.)

Auto-Zero Cycle

During the auto-zero cycle the differential input signal is disconnected from the circuit by opening internal analog gates. The internal nodes are shorted to analog common (internal analog ground) to establish a zero input condition. Additional analog gates close a feedback loop around the integrator and comparator. This loop permits comparator

offset voltage error compensation. The voltage level established on CAZ compensates for device offset voltages.

The auto-zero cycle length is 19 counts minimum. Unused time in the deintegrate cycle is added to the auto-zero cycle.

Signal Integration Cycle

The auto-zero loop is opened and the internal differential inputs connect to +IN and -IN. The differential input signal is integrated for a fixed time period. The TC826 signal integration period is 20 clock periods or counts. The externally set clock frequency is divided by 32 before clocking the internal counters. The integration time period is:

$$T_{SI} = \frac{32}{F_{OSC}} \times 20$$

Where:

F_{OSC} = External Clock Frequency

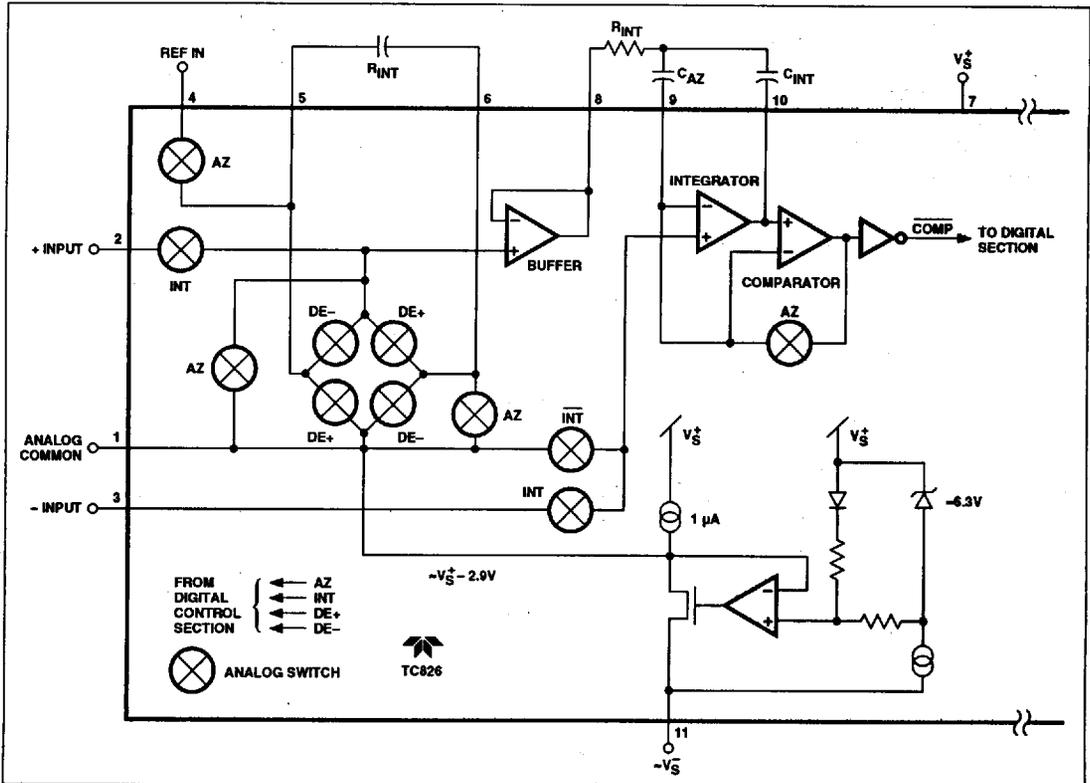


Figure 4 TC826 Analog Section

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The differential input voltage must be within the device common-mode range when the converter and measured system share the same power supply common (ground). If the converter and measured system do not share the same power supply common, $-IN$ should be tied to analog-common. This is the usual connection for battery operated systems. Polarity is determined at the end of signal integrate phase. The sign bit is a true polarity indication in that signals less than 1 LSB are correctly determined. This allows precision null detection limited only by device noise and system noise.

Reference Integrate Cycle

The final phase is reference integrate or deintegrate. $-IN$ is internally connected to analog common and $+IN$ is connected with the correct polarity to cause the integrator output to return to zero. The time required for the output to return to zero is proportional to the input signal and is between 0 and 40 counts. The digital reading displayed is:

$$20 = \frac{V_{IN}}{V_{REF}}$$

System Timing

The oscillator frequency is divided by 32 prior to clocking the internal counters. The three phase measurement

cycle takes a total of 80 clock pulses. The 80 count cycle is independent of input signal magnitude.

Each phase of the measurement cycle has the following length:

- Auto-Zero Phase: 19 to 59 Counts
For signals less than full-scale the auto-zero is assigned the unused reference integrate time period.
- Signal Integrate: 20 Counts
This time period is fixed. The integration period is:

$$T_{SI} = 20 \left[\frac{32}{F_{OSC}} \right]$$

Where F_{OSC} is the externally set clock frequency.

- Reference Integrate: 0 to 41 Counts

Reference Voltage Selection

A full-scale reading requires the input signal be twice the reference voltage. The reference potential is measured between REF IN (Pin 4) and Analog-Common (Pin 1).

Required Full-Scale Voltage	V_{REF}
20 mV	10 mV
2V	1V

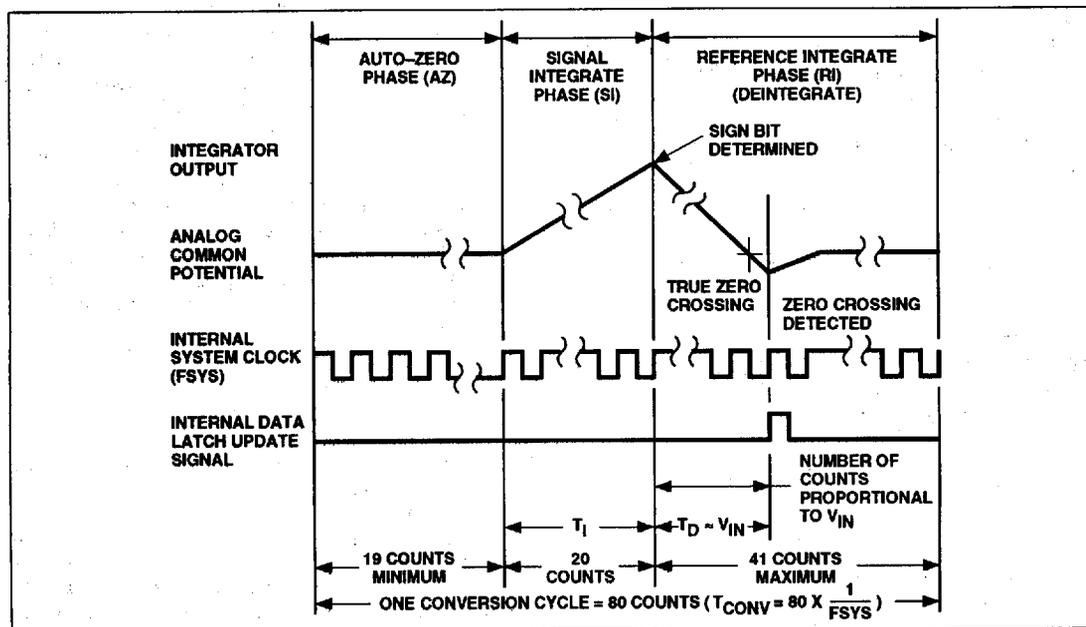


Figure 5 TC826 Conversion Has Three Phases

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The internal voltage reference potential available at analog-common will normally be used to supply the converters reference. This potential is stable whenever the supply potential is greater than approximately 7V. In applications where an externally generated reference voltage is desired refer to Figure 6.

The reference voltage is adjusted with a near full-scale input signal. Adjust for proper LCD display readout.

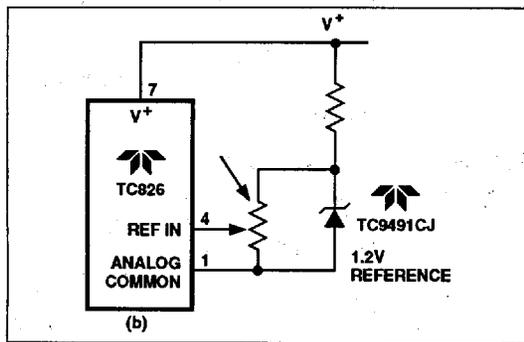


Figure 6 External Reference

Components Value Selection

Integrating Resistor (R_{INT})

The desired full-scale input voltage and output current capability of the input buffer and integrator amplifier set the integration resistor value. The internal class A output stage amplifiers will supply a 1 μ A drive current with minimal linearity error. R_{INT} is easily calculated for a 1 μ A full-scale current:

$$R_{INT} = \frac{\text{Full-Scale Input Voltage (V)}}{1 \times 10^{-6}} = \frac{V_{FS}}{1 \times 10^{-6}}$$

Where V_{FS} = Full-Scale Analog Input

Integrating Capacitor (C_{INT})

The integrating capacitor should be selected to maximize integrator output swing. The integrator output will swing to within 0.4V of V_{S+} or V_{S-} without saturating.

The integrating capacitor is easily calculated:

$$C_{INT} = \frac{V_{FS}}{R_{INT}} \left(\frac{640}{F_{OSC} \times V_{INT}} \right)$$

Where: V_{INT} = Integrator Swing
 F_{OSC} = Oscillator Frequency

The integrating capacitor should be selected for low dielectric absorption to prevent roll-over errors. Polypropylene capacitors are suggested.

Auto-Zero Capacitor (C_{AZ})

C_{AZ} should be 2-3 times larger than the integration capacitor. A polypropylene capacitor is suggested. Typical values from 0.14 μ F to 0.068 μ F are satisfactory.

Reference Capacitor (C_{REF})

A 1 μ F capacitor is suggested. Low leakage capacitors such as polypropylene are recommended.

Several capacitor/resistor combinations for common full-scale input conditions are given in Table 1.

Table 1 Suggested Component Values

Component	2V	200 mV	20 mV
	Full-Scale $V_{REF} \approx 1V$	Full-Scale $V_{REF} \approx 100 \text{ mV}$	Full-Scale $V_{REF} \approx 10 \text{ mV}$
R_{INT}	2 M Ω	200 k Ω	20 k Ω
C_{INT}	0.033 μ F	0.033 μ F	0.033 μ F
C_{REF}	1 μ F	1 μ F	1 μ F
C_{AZ}	0.068 μ F	0.068 μ F	0.14 μ F
R_{OSC}	430 k Ω	430 k Ω	430 k Ω

NOTES: Approximately 5 conversions/second.

Differential Signal Inputs

The TC826 is designed with true differential inputs and accepts input signals within the input stage common-mode voltage range (V_{CM}). The typical range is $V^+ -1$ to $V^- +1V$. Common-mode voltages are removed from the system when the TC826 operates from a battery or floating power source (isolated from measured system) and $-IN$ is connected to analog-common (V_{COM}).

In systems where common-mode rejection ratio minimizes error. Common-mode voltages do, however, affect the integrator output level. Integrator output saturation must be prevented. A worse case condition exists if a large positive V_{CM} exists in conjunction with a full-scale negative differential signal. The negative signal drives the integrator output positive along with V_{CM} . For such applications, the integrator output swing can be reduced below the recommended 2V full-scale swing. The integrator output will swing within 0.3V of V_{S+} or V_{S-} without increased linearity error.

Digital Section

The TC826 contains all the segment drivers necessary to drive a liquid crystal display (LCD). An LCD backplane driver is included. The backplane frequency is the external clock frequency divided by 256. A 430 k Ω OSC gets the backplane frequency to approximately 55 Hz with a 5V nominal amplitude. When a segment driver is in phase with the backplane signal the segment is 'OFF'. An out-of-phase segment drive signal causes the segment to be 'ON' or

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visible. This AC drive configuration results in negligible DC voltage across each LCD segment. This insures long LCD display life. The polarity segment drive, -POL, is 'ON' for negative analog inputs. If +IN and -IN are reversed this indicator would reverse. The TC826 transfer function is shown in Figure 7.

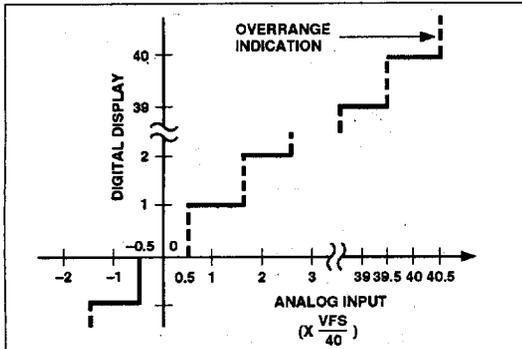


Figure 7 TC826 Transfer Function

BAR / DOT Input (Pin 58)

The BAR / DOT input allows the user to select the display format. The TC826 powers up in the BAR mode. Select the DOT display format by connecting BAR / DOT to the negative supply (Pin 11) through a 1 MΩ resistor.

HOLD Input (Pin 59)

The TC826 data output latches are not updated at the end of each conversion if HOLD is tied to the negative supply (Pin 11) through a 1 MΩ series resistor. The LCD display continuously displays the previous conversion results.

The HOLD pin is normally pulled high by an internal pull-up.

TEST Input (Pin 59)

The TC826 enters a test mode with the TEST input connected to the negative supply (Pin 11). The connection must be made through a 1 MΩ resistor. The TEST input is normally internally pulled high. A low input sets the output data latch to all ones. The BAR display mode is set. The 41 LCD output segments (zero plus 40 data segments) and overrange annunciator flash on and off at 1/4 the conversion rate. The polarity annunciator (POL-) segment will be on but not flashing.

Overrange Display Operation (OR, Pin 56)

An out-of-range input signal will be indicated on the LCD display by the OR annunciator driver (Pin 56) becoming active.

In the BAR display format the 41 bar segments and the overrange annunciator, OR, will flash ON and OFF. The flash rate is one fourth the conversion rate (FOSC/2560).

In the DOT display mode, OR flashes and all other data segment drivers are off.

Polarity Indication (POL—Pin 57)

The TC826 converts and displays data for positive and negative input signals. The POL—LCD segment driver (Pin 57) is active for negative signals.

Oscillator Operation

The TC826 external oscillator frequency, FOSC, is set by resistor RO SC connected between pins 12 and 13. The oscillator frequency vs. resistance curve is shown in Figure 8.

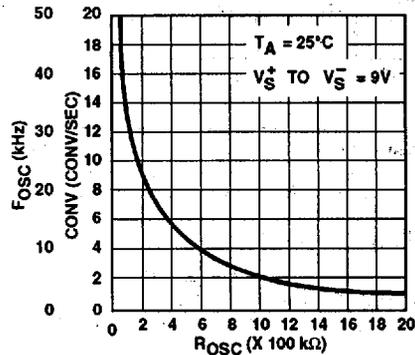


Figure 8 Oscillator Frequency vs. RO SC

FOSC is divided by 32 to provide an internal system clock, FYSY. Each conversion requires 80 internal clock cycles. The internal system clock is divided by 8 to provide the LCD backplane drive frequency. The display flash rate during an input out-of-range signal is set by dividing FYSY by 320. (See Figure 9.)

The internal oscillator may be bypassed by driving OSC1 (Pin 12) with an external signal generator. OSC2 (Pin 13) should be left unconnected.

The oscillator should swing from V_{S+} to V_{S-} in single supply operation (Figure 10A). In dual supply operation the signal should swing from power supply ground to V_{S+} .

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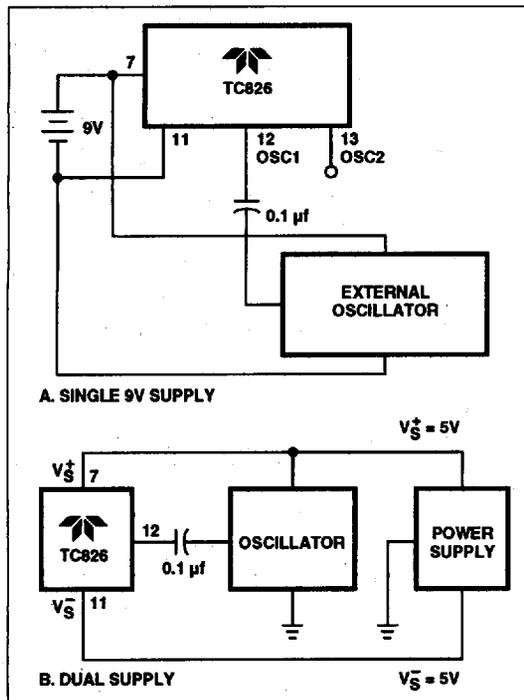


Figure 10 External Oscillator Connection

LCD Display Format

The input signal can be displayed in two formats (Figure 11). The BAR / DOT input (Pin 58) selects the format. The TC826 measurement cycle operates indifferently for either mode.

A. BAR MODE

1. INPUT = 0

BAR 4	<input type="checkbox"/>	OFF
BAR 3	<input type="checkbox"/>	OFF
BAR 2	<input type="checkbox"/>	OFF
BAR 1	<input type="checkbox"/>	OFF
BAR 0	<input checked="" type="checkbox"/>	ON

2. INPUT = 5% OF FULL-SCALE

<input type="checkbox"/>	OFF
<input type="checkbox"/>	OFF
<input checked="" type="checkbox"/>	ON
<input checked="" type="checkbox"/>	ON
<input checked="" type="checkbox"/>	ON

B. DOT MODE

1. INPUT = 0

BAR 4	<input type="checkbox"/>	OFF
BAR 3	<input type="checkbox"/>	OFF
BAR 2	<input type="checkbox"/>	OFF
BAR 1	<input type="checkbox"/>	OFF
BAR 0	<input checked="" type="checkbox"/>	ON

2. INPUT = 5% OF FULL-SCALE

<input type="checkbox"/>	OFF
<input type="checkbox"/>	OFF
<input checked="" type="checkbox"/>	ON
<input type="checkbox"/>	OFF
<input type="checkbox"/>	OFF

Figure 11 Display Option Formats

BAR Format

The TC826 power-ups in the BAR mode. BAR / DOT is pulled high internally. This display format is similar to a thermometer display. All bars/LCD segments, including zero, below the bar/LCD segment equaling the input signal level are on. A half-scale input signal, for example, would be displayed with BAR 0 to BAR 20 on.

DOT Format

By connecting BAR / DOT to V_S^- through a 1 MΩ resistor the DOT mode is selected. Only the BAR LCD segment equaling the input signal is on. The zero segment is on for zero input.

This mode is useful for moving cursor or 'needle' applications.

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LCD DISPLAYS

Most end products will use a custom LCD display for final production. Custom LCD displays are low cost and available from all manufacturers. The TC826 interfaces to non-multiplexed LCD displays. A backplane driver is included on chip.

To speed initial evaluation and prototype work a standard TC826 LCD display is available from Varitronix.

Varitronix Ltd.
9/F Linen House, 61-63, King Yip Street
Kwun Tjong, Hong Kong
Telex: 36643 VTRAX HX

USA Office:
VL Electronics Inc.
3161 Los Feliz Blvd., Suite 303
Los Angeles, CA 90039
Tel: 213/661-8883
Telex: 821554

- Part No.: VBG412-1 (Pin Connectors)
- Part No.: VBG412-2 (Elastomer Connectors)

Other standard LCD displays suitable for development work are available in both linear and circular formats. One manufacturer is:

UCE Inc.
24 Fitch Street
Norwalk, CT 06855
Tel: 203/838-7509

- Part No. 5040: 50 segment circular display with 3 digit numeric scale.
- Part No. 5020: 50 segment linear display.

LCD BACKPLANE DRIVER (PIN 14)

Additional drive electronics is not required to interface the TC826 to an LCD display. The TC826 has an on-chip backplane generator and driver. The backplane frequency is:

$$FBP = FOSC/256$$

Figure 12 gives typical backplane driver rise/fall time v. backplane capacitance.

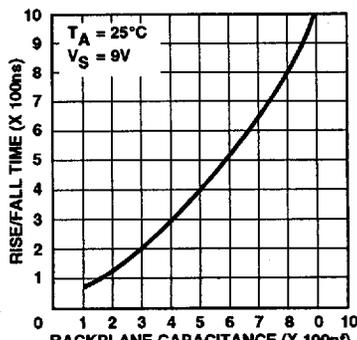


Figure 12 Backplane Driver Rise/Fall Time vs. Capacitance

FLAT PACKAGE SOCKET

Sockets suitable for prototype work are available. A USA source is:

Nepenthe Distribution
2471 East Bayshore, Suite 520
Palo Alto, CA 94303
Tel: 415/856-9332
Telex: 910/373-2060

'BQ' Socket Part No.: IC51-064-042 BQ