◀▼ TELEDYNE
SEMICONDUCTOR

TSC826
A/D Converter With
Bar Graph Display Output
- ● **2.5% Resolution**
- ● **Direct LCD Drive**
- ● **Bar/Dot Display Format**

General Description

In many applications a graphical display is preferred over a digital display. Knowing a process or system operates, for example, within design limits is more valuable than a direct system variable readout. A bar or moving dot display supplies information precisely without requiring further interpretation by the viewer.

The TSC826 is a complete analog-to-digital converter with direct liquid crystal (LCD) display drive. The 40 LCD data segments plus zero driver give a 2.5% resolution bar display. Full-scale differential input voltage range extends from 20 mV to 2 V. The TSC826 sensitivity is 500 μV. A low drift 35 ppm/°C internal reference, LCD backplane oscillator and driver, input polarity LCD driver, and overrange LCD driver make designs simple and low cost. The CMOS design requires only 125 μA from a 9 V battery. In +5 V systems a TSC7660 DC to DC converter can supply the –5 V supply. The differential analog input leakage is a low 10 pA.

Two display formats are possible. The BAR mode display is like a "thermometer" scale. The LCD segment driver that equals the input plus all below it are on. The DOT mode activates only the segment equal to the input. In either mode the polarity signal is active for negative input signals. An overrange input signal causes the display to flash and activates the overrange annunciator. A hold mode can be selected that freezes the display and prevents updating.

The dual slope integrating conversion method with auto-zero phase maximizes noise immunity and eliminates zero-scale adjustment potentiometers. Zero-scale drift is a low 5 μV/°C. Conversion rate is typically 5 per second and is adjustable by a single external resistor.

A compact, 0.5" square, flat package minimizes PC board area. The high pin count LSI package makes multiplexed LCD displays unnecessary. Low cost, direct drive LCD displays offer the widest viewing angle and are readily available. A standard display is available now for TSC826 prototyping work.

Features

- ● Bipolar A/D Conversion
- ● 2.5% Resolution
- ● Direct LCD Display Drive
- ● "Thermometer" Bar or Dot Display
- ● 40 Data Segments Plus Zero
- ● Overrange Plus Polarity Indication
- ● Precision On-Chip Reference .... 35 ppm/°C
- ● Differential Analog Input
- ● Low Input Leakage .... 10 pA
- ● Display Flashes on Overrange
- ● Display Hold Mode
- ● Auto-Zero Cycle Eliminates Zero Adjust Potentiometer
- ● 9 V Battery Operation
- ● Low Power Consumption .... 1.1 mW
- ● 20 mV to 2.0 V Full-Scale Operation
- ● Non-Multiplexed LCD Drive for Maximum Viewing Angle

Ordering Information

Part No.	Package	Temperature Range
TSC826CBQ	60-Pin Plastic Quad Flat Package Formed Leads	0°C to 70°C
TSC826CSQ	60-Pin Plastic Quad Flat Package Straight Leads	0°C to 70°C
TSC826Y	CHIP	0°C to 70°C

Pin Configuration
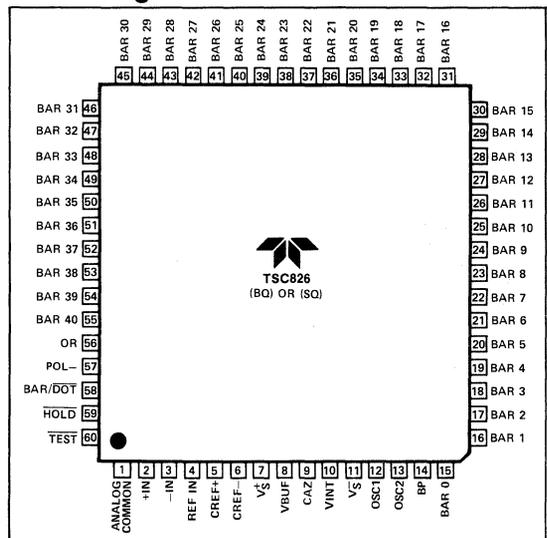
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Absolute Maximum Ratings

Supply Voltage (V^+ to V^-) .... 15 V

Analog Input Voltage (either input)[1] .... V^+ to V^-

Package Power Dissipation

    Flat Package (B, S) .... 500 mW

Operating Temperature

    ("C" Devices) .... 0°C to +70°C

Storage Temperature .... −65°C to +160°C

Lead Temperature (Soldering, 60 sec) .... 300°C

Electrical Characteristics: V_S = 9 V, ROSC = 430 kΩ, TA = 25°C, Full-Scale = 20 mV unless otherwise stated.

NO.	SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TSC826 TYP	MAX	UNIT
1	—	Zero Input Reading	V_{IN} = 0.0 V	−0	±0	+0	Display
2	—	Zero Reading Drift	V_{IN} = 0.0 V 0°C ≤ T_A ≤ 70°C	—	0.2	1	μV/°C
3	NL	Linearity Error	Max Deviation From Best Straight Line	−1	0.5	+1	Count
4	—	Rollover Error	$-V_{IN}$ = $+V_{IN}$	−1	0	+1	Count
5	EN	Noise	V_{IN} = 0 V	—	60	—	μV$_{P-P}$
6	ILK	Input Leakage Current	V_{IN} = 0 V	—	10	20	pA
7	CMRR	Common-Mode Rejection Ratio	VCM = ±1 V V_{IN} = 0 V	—	50	—	μV/V
8	—	Scale Factor Temperature Coefficient	0 ≤ T_A ≤ 70°C External Ref. Temperature Coefficient = 0 ppm/°C	—	1	—	ppm/°C
9	VCTC	Analog Common Temperature Coefficient	250 kΩ Between Common and V^+ 0°C ≤ T_A ≤ 70°C	—	35	100	ppm/°C
10		Analog Common Voltage	250 kΩ Between Common and V_S^+	2.7	2.9	3.35	V
11	VSD	LCD Segment Drive Voltage		4	5	6	V$_{P-P}$
12	VBD	LCD Backplane Drive Voltage		4	5	6	V$_{P-P}$
13	I	Power Supply Current		—	125	175	μA

Notes:

1. Input voltages may exceed the supply voltages when the input current is limited to 100 μA.
2. Static sensitive device. Unused devices should be stored in conductive material to protect devices from static discharge and static fields.
3. Backplane drive is in phase with segment drive for "off" segment and 180°C out of phase for "on" segment. Frequency is 10 times conversion rate.
4. Logic input pins 58, 59, 60 should be connected through 1 MΩ series resistors to V_S^- for logic 0.

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Pin Description and Function

PIN NO.	NAME	DESCRIPTION
1	Analog Common	Establishes the internal analog ground point. Analog common is set to 2.9 V below the positive supply by an internal zener reference circuit. The voltage difference between V_S^+ and analog-common can be used to supply the TSC826 voltage reference input at REF IN (Pin 4).
2	+IN	Positive analog signal input.
3	−In	Negative analog signal input.
4	REF IN	Reference voltage positive input. Measured relative to analog-common. REF IN ≈ Full-Scale/2.
5	C_{REF} +	Reference capacitor connection.
6	C_{REF} −	Reference capacitor connection.
7	V_S^+	Positive supply terminal.
8	VBUF	Buffer output. Integration resistor connection.
9	CAZ	Negative comparator input. Auto-zero capacitor connection.
10	VINT	Integrator output. Integration capacitor connection.
11	V_S^-	Negative supply terminal.
12	OSC1	Oscillator resistor (R_{OSC}) connection.
13	OSC2	Oscillator resistor (R_{OSC}) connection.
14	BP	LCD Backplane driver.
15	BAR 0	LCD Segment driver: Bar 0
16	1	1
17	2	2
18	3	3
19	4	4
20	5	5
21	6	6
22	7	7
23	8	8
24	9	9
25	10	10
26	11	11
27	12	12
28	13	13
29	14	14
30	15	15
31	16	16
32	17	17
33	18	18
34	19	19
35	20	20
36	21	21
37	22	22
38	23	23

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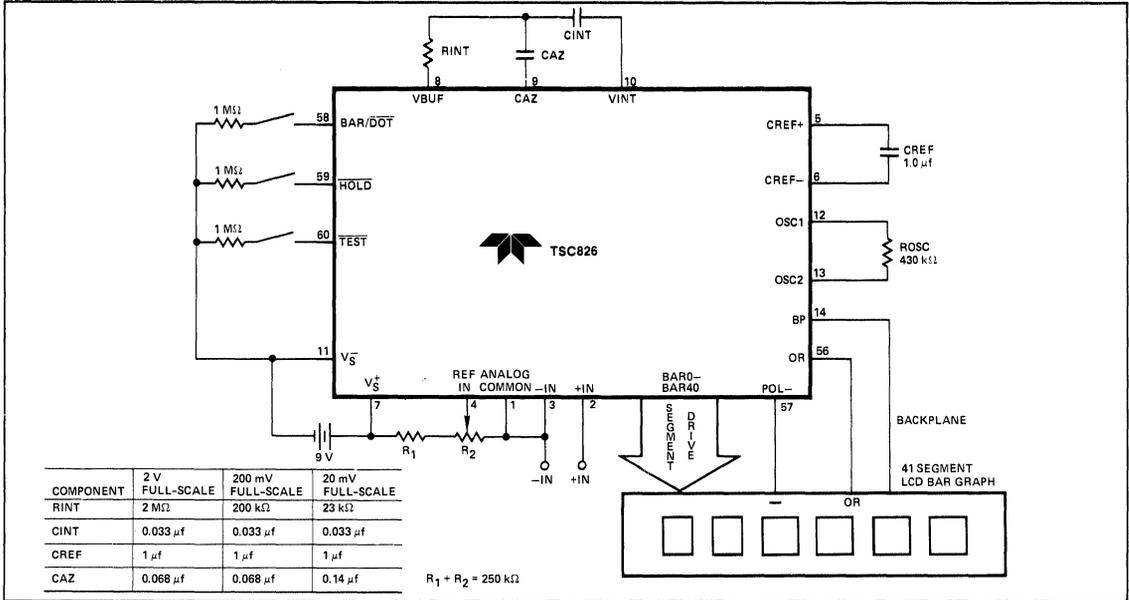## Pin Description and Function (Cont.)

PIN NO.	NAME	DESCRIPTION
39	BAR 24	BAR Segment driver: Bar 24
40	25	25
41	26	26
42	27	27
43	28	28
44	29	29
45	30	30
46	31	31
47	32	32
48	33	33
49	34	34
50	35	35
51	36	36
52	37	37
53	38	38
54	39	39
55	40	40
56	OR	LCD segment driver that indicates input out-of-range condition.
57	POL-	LCD segment driver that indicates input signal is negative.
58	BAR/$\overline{\text{DOT}}$	Input logic signal that selects bar or dot display format. Normally in bar mode. Connect to $\overline{V_S}$ through 1MΩ resistor for Dot format.
59	$\overline{\text{HOLD}}$	Input logic signal that prevents display from changing. Pulled high internally to inactive state. Connect to V_S through 1MΩ series resistor for HOLD mode operation.
60	$\overline{\text{TEST}}$	Input logic signal. Sets TSC805 to BAR display mode. Bar 0 to 40, plus OR flash on and off. The POL-LCD driver is on. Pulled high internally to inactive state. Connect to V_S with 1 MΩ series resistor to activate.

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Typical TSC826 Circuit Connection (Figure 1)

COMPONENT	2 V FULL-SCALE	200 mV FULL-SCALE	20 mV FULL-SCALE
RINT	2 MΩ	200 kΩ	23 kΩ
CINT	0.033 μf	0.033 μf	0.033 μf
CREF	1 μf	1 μf	1 μf
CAZ	0.068 μf	0.068 μf	0.14 μf

$R_1 + R_2 = 250 \text{ k}\Omega$

Dual Slope Conversion Principles

The TSC826 is a dual slope, integrating analog-to-digital converter. The conventional dual slope converter measurement cycle has two distinct phases:

- Input Signal Integration
- Reference Voltage Integration (Deintegration)

The input signal being converted is integrated for a fixed time period (T_{SI}). Time is measured by counting clock pulses. An opposite polarity constant reference voltage is then integrated until the integrator output voltage returns to zero. The reference integration time is directly proportional to the input signal (T_{RI}). (Figure 2).

In a simple dual slope converter a complete conversion requires the integrator output to "ramp-up" and "ramp-down."

A simple mathematical equation relates the input signal reference voltage and integration time:

$$\frac{1}{RC} \int_0^{T_{SI}} V_{IN}(t)dt = \frac{V_R \, T_{RI}}{RC}$$

where:

V_R = Reference Voltage
V_{SI} = Signal Integration Time (Fixed)
T_{RI} = Reference Voltage Integration Time (Variable)

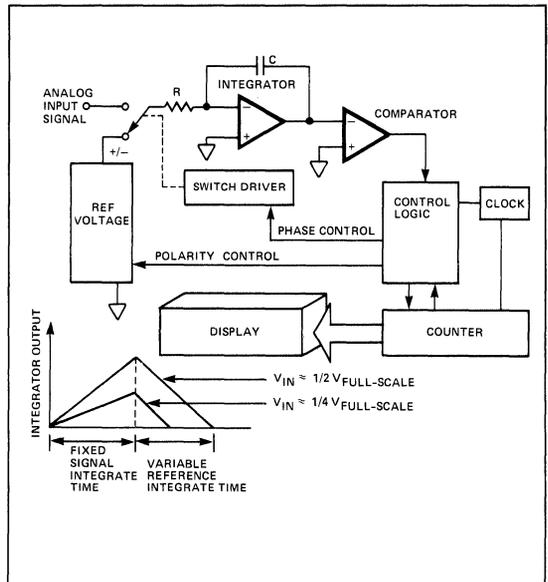For a constant V_{IN}: $V_{IN} = V_R \dfrac{T_{RI}}{T_{SI}}$

Figure 2: Basic Dual Slope Converter

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The dual slope converter accuracy is unrelated to the integrating resistor and capacitor values as long as they are stable during a measurement cycle. An inherent benefit is noise immunity. Noise spikes are integrated or averaged to zero during the integration periods. Integrating ADCs are immune to the large conversion errors that plague successive approximation converters in high noise environments. Interfereing signals with frequency components at multiples of the averaging period will be attenuated. (Figure 3).

The TSC826 converter improves the conventional dual slope conversion technique by incorporating an auto-zero phase. This phase eliminates zero-scale offset errors and drift. A potentiometer is not required to obtain a zero output for zero input.
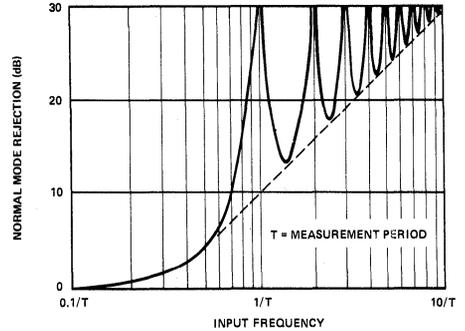

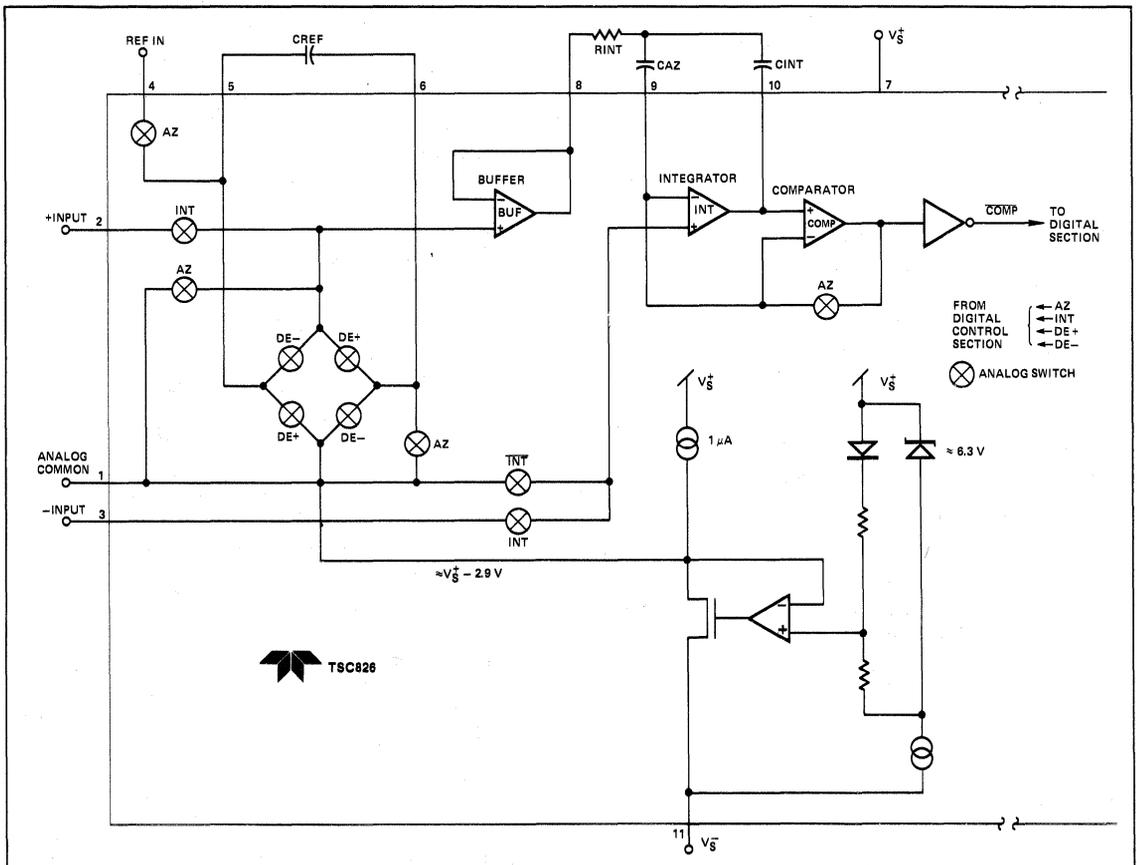**Figure 3: Normal-Mode Rejection of Dual Slope Converter**

Figure 4: TSC826 Analog Section

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Theory of Operation
Analog Section

In addition to the basic signal integrate and deintegrate cycles discussed above the TSC826 incorporates an auto-zero cycle. This cycle removes buffer amplifier, integrator, and comparator offset voltage error terms from the conversion. A true digital zero reading results without external adjusting potentiometers. A complete conversion consists of three cycles: an auto-zero, signal integrate and reference integrate cycle. See Figure 4 and 5.

Auto-Zero Cycle

During the auto-zero cycle the differential input signal is disconnected from the circuit by opening internal analog gates. The internal nodes are shorted to analog common (internal analog ground) to establish a zero input condition. Additional analog gates close a feedback loop around the integrator and comparator. This loop permits comparator offset voltage error compensation. The voltage level established on CAZ compensates for device offset voltages.

The auto-zero cycle length is 19 counts minimum. Unused time in the deintegrate cycle is added to the auto-zero cycle.

Signal Integration Cycle

The auto-zero loop is opened and the internal differential inputs connect to +IN and –IN. The differential input signal is integrated for a fixed time period. The TSC826 signal integra-

tion period is 20 clock periods or counts. The externally set clock frequency is devided by 32 before clocking the internal counters. The integration time period is:

$$T_{SI} = \frac{32}{F_{OSC}} \times 20$$

Where:

F_{OSC} = External Clock Frequency

The differential input voltage must be within the device common-mode range when the converter and measured system share the same power supply common (ground). If the converter and measured system do not share the same power supply common, –IN should be tied to analog-common. This is the usual connection for battery operated systems. Polarity is determined at the end of signal integrate signal phase. The sign bit is a true polarity indication in that signals less than 1 LSB are correctly determined. This allows precision null detection limited only by device noise and system noise.

Reference Integrate Cycle

The final phase is reference integrate or deintegrate. –IN is internally connected to analog common and +IN is connected with the correct polarity to cause the integrator output to return to zero. The time required for the output to return to zero is proportional to the input signal and is between 0 and 40 counts. The digital reading displayed is:
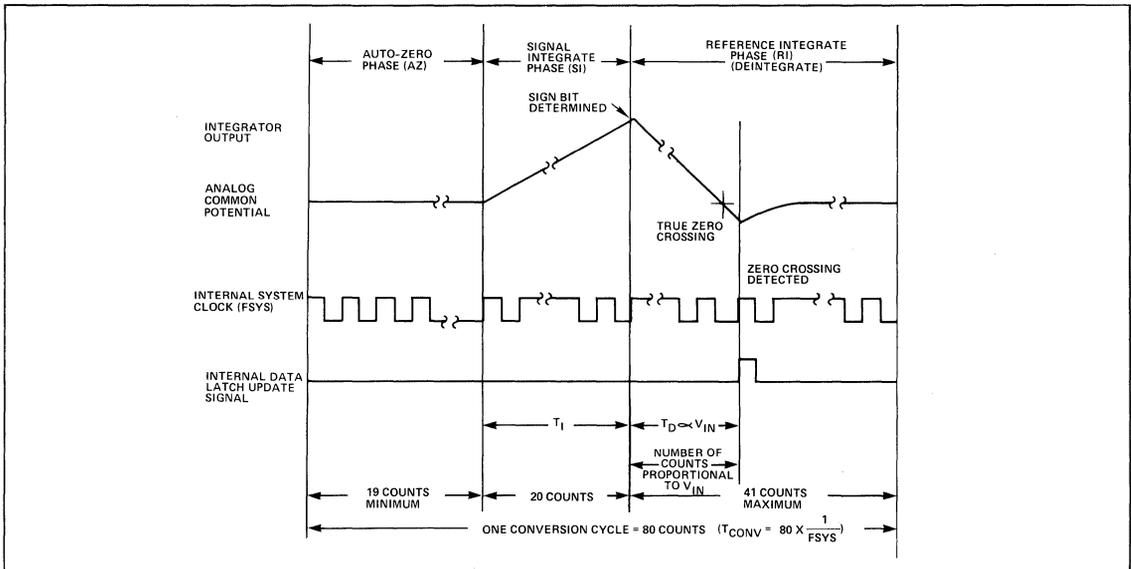
$$20 \frac{V_{IN}}{V_{REF}}$$

Figure 5: TSC826 Conversion Has Three Phases

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System Timing

The oscillator frequency is divided by 32 prior to clocking the internal counters. The three phase measurement cycle takes a total of 80 clock pulses. The 80 count cycle is independent of input signal magnitude.

Each phase of the measurement cycle has the following length:

● Auto-Zero Phase: 19 to 59 Counts
  For signals less than full-scale the auto-zero phase is assigned the unused reference integrate time period.

● Signal Integrate: 20 Counts
  This time period is fixed. The integration period is:

$$T_{SI} = 20 \left[\frac{32}{F_{OSC}} \right]$$

Where F_{OSC} is the externally set clock frequency.

● Reference Integrate: 0 to 41 Counts

Reference Voltage Selection

A full-scale reading requires the input signal be twice the reference voltage. The reference potential is measured between REF IN (Pin 4) and Analog-Common (Pin 1).

Required Full-Scale Voltage	V_{REF}
20 mV	10 mV
2 V	1 V

The internal voltage reference potential available at analog-common will normally be used to supply the converters reference. This potential is stable whenever the supply potential is greater than approximately 7 V. In applications where an externally generated reference voltage is desired refer to Figure 6.

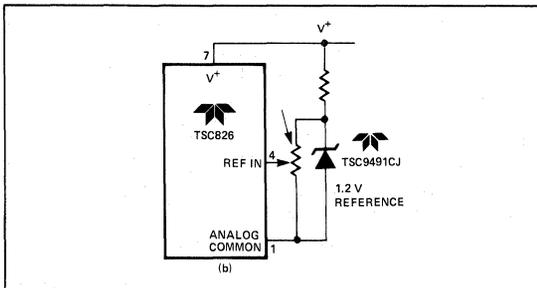The reference voltage is adjusted with a near full-scale input signal. Adjust for proper LCD display readout.

Figure 6: External Reference

Component Value Selection
Integrating Resistor (RINT)

The desired full-scale input voltage and output current capability of the input buffer and integrator amplifier set the integration resistor value. The internal class A output stage amplifiers will supply a 1 μA drive current with minimal linearity error. RINT is easily calculated for a 1 μA full-scale current:

$$R_{INT} = \frac{\text{Full-Scale Input Voltage (V)}}{1 \times 10^{-6}} = \frac{VFS}{1 \times 10^{-6}}$$

Where: VFS = Full-Scale Analog Input

Integrating Capacitor (CINT)

The integrating capacitor should be selected to maximize integrator output swing. The integrator output will swing to within 0.4 V of V_S^+ or V_S^- without saturating.

The integrating capacitor is easily calculated:

$$CINT = \frac{VFS}{RINT} \left(\frac{640}{FOSC \times VINT} \right)$$

Where: VINT = Integrator Swing
       FOSC = Oscillator Frequency

The integrating capacitor should be selected for low dielectric absorption to prevent roll-over errors. Polypropylene capacitors are suggested.

Auto-Zero Capacitor (CAZ)

CAZ should be 2-3 times larger than the integration capacitor. A polypropylene capacitor is suggested. Typical values from 0.14 μf to 0.068 μf are satisfactory.

Reference Capacitor (CREF)

A 1.0 μf capacitor is suggested. Low leakage capacitors such as polypropylene are recommended.

Several capacitor/resistor combinations for common full-scale input conditions are given in Table 1.

Table 1: Suggested Component Values

Component	2 V Full-Scale $V_{REF} \approx$ 1 V	200 mV Full-Scale $V_{REF} \approx$ 100 mV	20 mV Full-Scale $V_{REF} \approx$ 10 mV
RINT	2 MΩ	200 kΩ	20 kΩ
CINT	0.033 μf	0.033 μf	0.033 μf
CREF	1 μf	1 μf	1 μf
CAZ	0.068 μf	0.068 μf	0.14 μf
ROSC	430 kΩ	430 kΩ	430 kΩ

1. Approximately 5 conversions/sec.

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Differential Signal Inputs (+IN (Pin 2), -IN (Pin 3))

The TSC826 is designed with true differential inputs and accepts input signals within the input stage common-mode voltage range (V_{CM}). The typical range is $V^+ -1.0$ to $V^- + 1$ V. Common-mode voltages are removed from the system when the TSC826 operates from a battery or floating power source (Isolated form measured system) and -IN is connected to analog-common (V_{COM}).

In systems where common-mode voltages exist the TSC826 72 dB common-mode rejection ratio minimizes error. Common-mode voltages do, however, affect the integrator output level. Integrator output saturation must be prevented. A worse case condition exists if a large positive V_{CM} exists in conjunction with a full-scale negative differential signal. The negative signal drives the integrator output positive along with V_{CM}. For such applications, the integrator output swing can be reduced below the recommended 2.0 V full-scale swing. The integrator output will swing within 0.3 V of V_S^+ or V_S^- without increased linearity error.

Digital Section

The TSC826 contains all the segment drivers necessary to drive a liquid crystal display (LCD). An LCD backplane driver is included. The backplane frequency is the external clock frequency divided by 256. A 430 kΩ OSC gets the backplane frequency to approximately 55 Hz with a 5 V nominal amplitude. When a segment driver is in phase with the backplane signal the segment is "OFF." An out-of-phase segment drive signal causes the segment to be "ON" or visible. This AC drive configuration results in negligible DC voltage across each LCD segment. This insures long LCD display life. The polarity segment driver, -POL, is "ON" for negative analog inputs. If +IN and -IN are reversed this indicator would reverse. The TSC826 transfer function is shown in Figure 7.
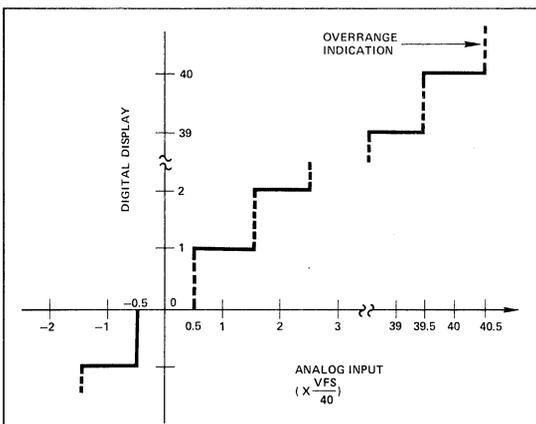

Figure 7: TSC826 Transfer Function

BAR/$\overline{\text{DOT}}$ Input (Pin 58)

The BAR/$\overline{\text{DOT}}$ input allows the user to select the display format. The TSC826 powers up in the BAR mode. Select the DOT display format by connecting BAR/$\overline{\text{DOT}}$ to the negative supply (Pin 11) through a 1 MΩ resistor.

$\overline{\text{HOLD}}$ Input (Pin 59)

The TSC826 data output latches are not updated at the end of each conversion if $\overline{\text{HOLD}}$ is tied to the negative supply (Pin 11) through a 1 MΩ series resistor. The LCD display continuously displays the previous conversion result.

The $\overline{\text{HOLD}}$ pin is normally pulled high by an internal pull-up.

$\overline{\text{TEST}}$ Input (Pin 60)

The TSC826 enters a test mode with the $\overline{\text{TEST}}$ input connected to the negative supply (Pin 11). The connection must be made through a 1 MΩ resistor. The $\overline{\text{TEST}}$ input is normally internally pulled high. A low input sets the output data latch to all ones. The BAR display mode is set. The 41 LCD output segments (zero plus 40 data segments) and overrange annunciator flash on and off at 1/4 the conversion rate. The polarity annunciator (POL-) segment will be on but not flashing.

Overrange Display Operation (OR, Pin 56)

An out-of-range input signal will be indicated on the LCD display by the OR annunciator driver (Pin 56) becoming active.

In the BAR display formate the 41 bar segments and the overrange annunciator, OR, will flash ON and OFF. The flash rate is one fourth the conversion rate (FOSC/2560).

In the DOT display mode, OR flashes and all other data segment drivers are off.

Polarity Indication (POL-, Pin 57)

The TSC826 converts and displays data for positive and negative input signals. The POL- LCD segment driver (Pin 57) is active for negative signals.
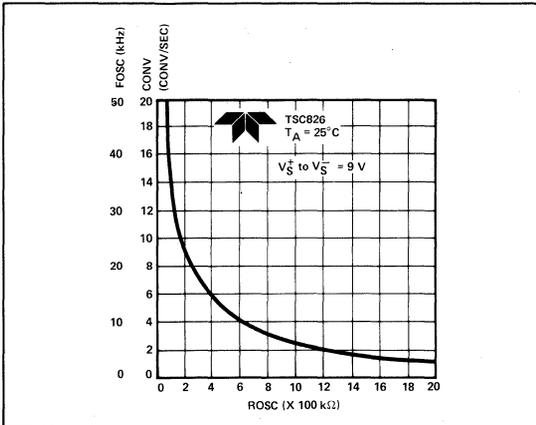
Oscillator Operation

The TSC826 external oscillator frequency, FOSC, is set by resistor ROSC connected between pins 12 and 13. The oscillator frequency vs resistance curve is shown in Figure 8.

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**Figure 8: Oscillator Frequency vs. ROSC**

FOSC is divided by 32 to provide an internal system clock, FSYS. Each conversion requires 80 internal clock cycles. The internal system clock is divided by 8 to provide the LCD backplane drive frequency. The display flash rate during an input out-of-range signal is set by dividing FSYS by 320. (See Figure 9)
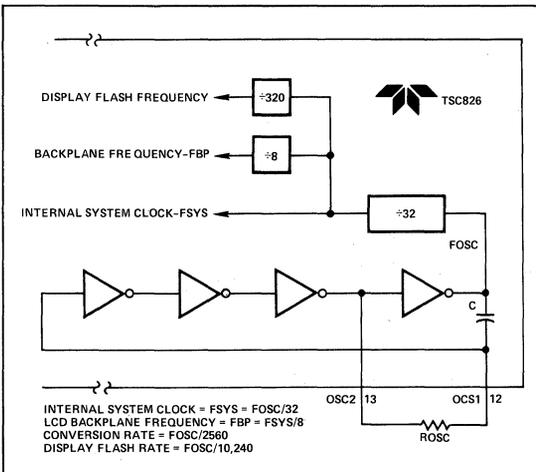
Figure 9: Internal Oscillator Operation

The internal oscillator may be bypassed by driving OSCI (Pin 12) with an external signal generator. OSC2 (Pin 13) should be left unconnected.

The oscillator should swing from V_S^+ to V_S^- in single supply operation (Figure 10A). In dual supply operation the signal should swing from power supply ground to V_S^+.
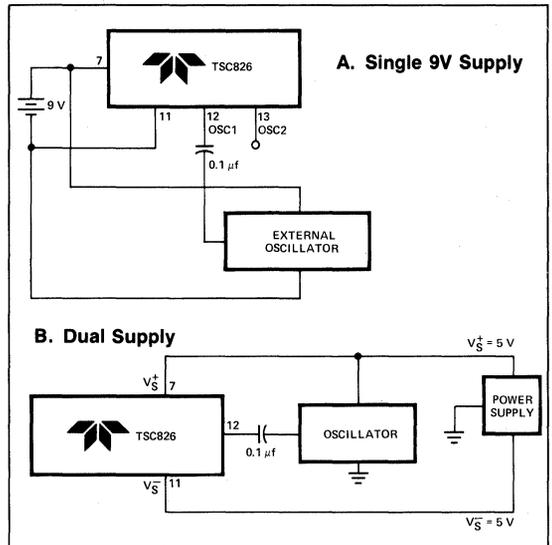
Figure 10: External Oscillator Connection

LCD Display Format

The input signal can be displayed in two formats (Figure 11). The BAR/$\overline{DOT}$ input (Pin 58) selects the format. The TSC826 measurement cycle operates identically for either mode.

BAR Format

The TSC826 power-ups in the BAR mode. BAR/$\overline{DOT}$ is pulled high internally. This display format is similar to a thermometer display. All bars/LCD segments, including zero, below the bar/LCD segment equalingd the input signal level are on. A half-scale input signal, for example, would be displayed with BAR 0 to BAR 20 on.

DOT Format

By connecting BAR/$\overline{DOT}$ to V_S^- through a 1 MΩ resistor the DOT mode is selected. Only the BAR LCD segment equalling the input signal is on. The zero segment is on for zero input.

This mode is useful for moving cursor or "needle" applications.

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A. BAR MODE

1. INPUT = 0   **2. INPUT = 5% of FULL-SCALE**

BAR 4	[___] OFF	[___]	OFF
BAR 3	[___] OFF	[___]	OFF
BAR 2	[___] OFF	[////]	ON
BAR 1	[___] OFF	[////]	ON
BAR 0	[////] ON	[////]	ON

B. DOT MODE

1. INPUT = 0   **2. INPUT = 5% of FULL-SCALE**

BAR 4	[___] OFF	[___]	OFF
BAR 3	[___] OFF	[___]	OFF
BAR 2	[___] OFF	[////]	ON
BAR 1	[___] OFF	[___]	OFF
BAR 0	[////] ON	[___]	OFF

Figure 11: Display Option Formats

LCD Displays

Most end products will use a custom LCD display for final production. Custom LCD displays are low cost and available from all manufacturers. The TSC826 interfaces to non-multiplexed LCD displays. A backplane driver is included on chip.

To speed initial evaluation and prototype work a standard TSC826 LCD display is available from Varitronix.

Varitronix Ltd.
9/F Linen House, 61-63, King Yip Street
Kwun Tjong, Hong Kong
Tel: 3-410286
TELEX: 36643 VTRAX HX

USA Office:
VL Electronics Inc.
2775 Glendower Avenue
Los Angeles, CA 900027
Tel: (213) 661-8883
TELEX: 821554

- Part No.: VBG412-1 (Pin Connectors)
- Part No.: VBG412-2 (Elastomer Connectors)

Other standard LCD displays suitable for development work are available in both linear and circular formats. One manufacturer is:

UCE Inc.
24 Fitch Street
Norwalk, Conn. 06855
(203) 838-7509

- Part No. 5040:   50 segment circular display with 3 digit numeric scale.

- Part No. 5020:   50 segment linear display.

LCD Backplane Driver (Pin 14)

Additional drive electronics is not required to interface the TSC826 to an LCD display. The TSC826 has an on-chip backplane generator and driver. The backplane frequency is:

$$FBP = FOSC/256$$

Figure 12 gives typical backplane driver rise/fall time vs backplane capacitance.
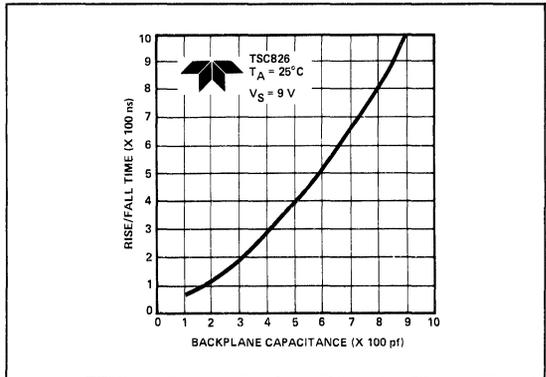

Figure 12: Backplane Driver Rise/Fall Time vs Capacitance

Flat Package Socket

Sockets suitable for prototype work are available. A USA source is:

Nepenthe Distribution
2471 East Bayshore
Suite 520
Palo Alto, California 94303
(415) 856-9332
TWX: 910-373-2060

(a) "BQ" Socket Part No.: IC51-064-042 BQ
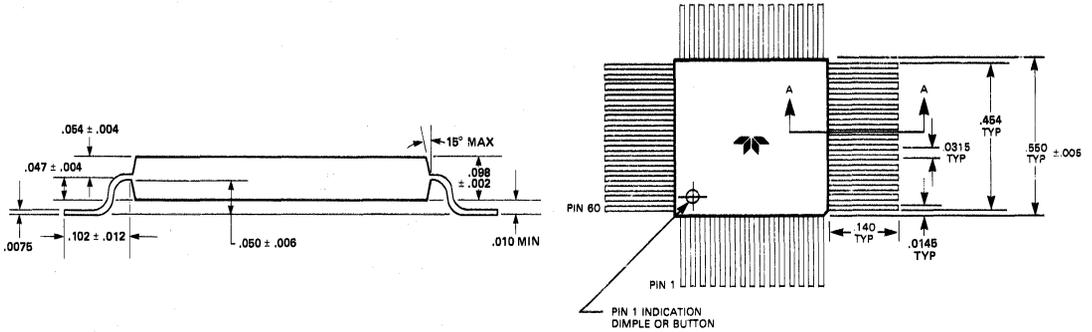
(b) "SQ" Socket Part No.: IC51-064-042 SQ

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◀▼ TELEDYNE SEMICONDUCTOR

A/D Converter With
Bar Graph Display Output
• 2.5% Resolution
• Direct LCD Drive
• Bar/Dot Display Format

TSC826

Package Outline

60-Pin Plastic Flat Package

.054 ± .004

.047 ± .004

15° MAX

.098 ± .002

.0075 .102 ± .012 .050 ± .006 .010 MIN

PIN 60

PIN 1

PIN 1 INDICATION
DIMPLE OR BUTTON

A

A

.454 TYP

.0315 TYP

.550 TYP ± .005

.140 TYP

.0145 TYP

"BQ" Package — Formed Leads

(Package #21)

"SQ" Package — Unformed Leads

(Package #22)