Monolithic CMOS D/A Converters

8600 Series

8640, 8641

12-Bit Multiplying

Features

- 12 bit linearity (0.01% achieved without laser trimming)
- 2 ppm/°C max gain error tempco
- Full Four Quadrant Multiplication
- Low Power CMOS, <30mW
- TTL/CMOS Compatible Inputs
- Low feedthrough error
- Compensated feedback resistor
- Low cost
- 883B processing available
- Direct replacement for AD7521 and AD7541

Applications

- CRT Graphics Generator
- Synchro-to-digital converters
- Digitally controlled attenuators
- Programmable amplifiers
- Digitally controlled power supplies
- A/D Conversion
- Function Generators
- Digital Filters

Ordering Information

Temperature Range / Nonlinearity	0°C to +70°C	−25°C to +85°C	−55°C to +125°C
0.024%	8640CJ	8640CN	8640BN
0.012%	8641CJ	8641CN	8641BN

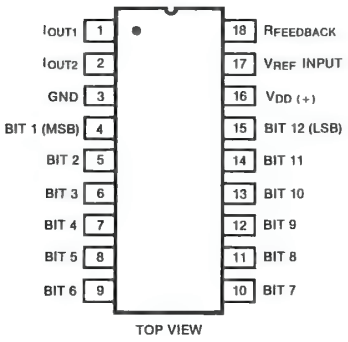
General Description

The 8640 and 8641 are 12-bit monolithic CMOS digital-to-analog converters featuring double layer metal interconnections for improved high speed operation and lower cost. The use of precision thin-film deposition resistors provides 12-bit linearity without laser trimming, thus eliminating any long-term instabilities laser trimming might introduce. The use of compensating FET switches in the feedback resistor and at the end of the ladder chain reduces gain error temperature coefficient to a maximum of 2 pm/°C.

The 8640, 8641, 12-bit multiplying D/A converters consist of a highly stable thin film R-2R ladder and twelve CMOS current switches on a monolithic chip. Most applications require the addition of only an output operational amplifier and a voltage or current reference.

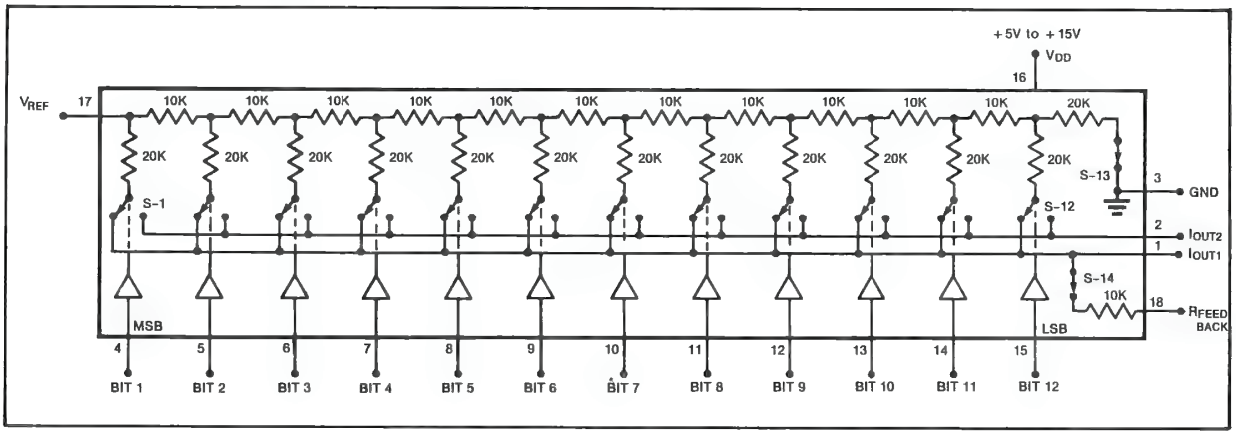
The 8640 and 8641 are pin for pin replacements for Analog Devices AD7541. They meet or exceed the performance of the AD7541, with improved supply rejection, lower variation of linearity and gain error with V_{DD}, and improved temperature stability.

Connection Diagram



TOP VIEW

Schematic Diagram



Absolute Maximum Ratings

($T_A = 25°$ unless otherwise noted)

Storage Temperature		−65°C to +150°C
Operating Temperature	CJ	0°C to −70°C
	CN	−25°C to +85°C
	BN	−55°C to −125°C
V_{DD} (to GND)		+17V
V_{REF} (to GND)		±25V
Digital Input Voltage Range		V_{DD} to GND
Output Voltage (Pin 1, Pin 2)		−100mV to V_{DD}
Package Dissipation Derate above +75°C by		450mW 6mW
Lead Temperature (Soldering, 10 seconds)		300°C

CAUTION

1. Do not apply voltages higher than V_{DD} or less than GND potential on any terminal except V_{REF}.
2. The digital control inputs are zener protected; however, permanent damage may occur on unconnected units under high energy electrostatic field. Terminate all unused inputs. Store in conductive foam at all times. Use proper anti-static handling procedures.

Electrical Characteristics

NOTE: Unless otherwise specified, V_{DD} = +15V, V_{REF} = +10V. See page 7 for definitions and test circuits.

PARAMETER	$T_A = 25°C$ MIN	TYP	MAX	T_A = Full Temp Range MIN	TYP	MAX	UNITS	CONDITIONS
STATIC ACCURACY								
Resolution	12			12			bits	
Nonlinearity 8640			±1			±1	LSB	$V_{OUT1} = V_{OUT2} = 0V$
8641			± ½			± ½	LSB	$V_{OUT1} = V_{OUT2} = 0V$
Nonlinearity Tempco			2			2	ppm/°C	
Gain Error[2]			±0.3				%FSR[1]	
Gain Error Tempco			2			2	ppm/°C	
Power Supply Sensitivity			0.003			0.005	%per%	V_{DD} = 15V ± 0.5V
Output Leakage Current			±50			±200	nA	V_{REF} = ±10V
DYNAMIC PERFORMANCE								
Output Current Settling Time			500			500	nS	to 2 LSB (.05%)
			1			1	μS	to ½ LSB (.01%)
Feedthrough Error			1			1	mVpp	V_{REF} = 20Vpp @ 10 kHz
REFERENCE INPUT								
Input Resistance	5	10	20	5		20	kΩ	
DIGITAL INPUTS								
V_{INH}			2.4			2.4	V	
V_{INL}	0.8			0.8			V	
Input Leakage Current			±1			±1	μA	V_{IN} = 0 or 15V
Input Capacitance			8			8	pF	
ANALOG OUTPUT CAPACITANCE								
C_{OUT1}			200			200	pF	Digital Inputs = V_{INH}
C_{OUT2}			60			60	pF	Digital Inputs = V_{INH}
C_{OUT1}			60			60	pF	Digital Inputs = V_{INL}
C_{OUT2}			200			200	pF	Digital Inputs = V_{INL}
POWER REQUIREMENTS								
V_{DD}Range	5		16	5		16	V	Accuracy is not guaranteed over this range
I_{DD}			2			2	mA	Digital Inputs = V_{INH} or V_{INL}

NOTES: 1. FSR is Full Scale Range
2. Using internal feedback resistor.

Typical Performance Characteristics

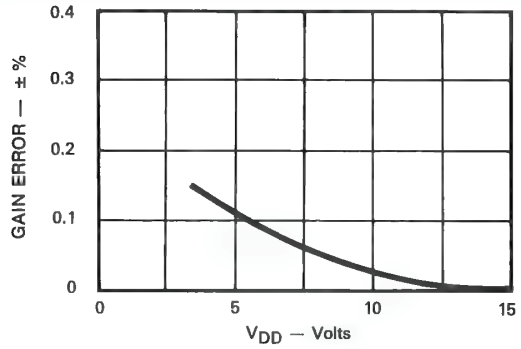


Figure 1. Gain Error vs. Supply Voltage

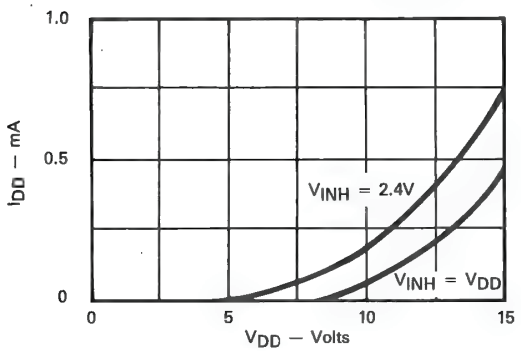


Figure 2. Supply Current vs. Supply Voltage

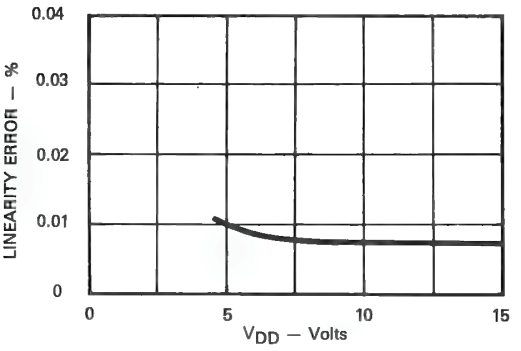


Figure 3. Linearity Error vs. Supply Voltage

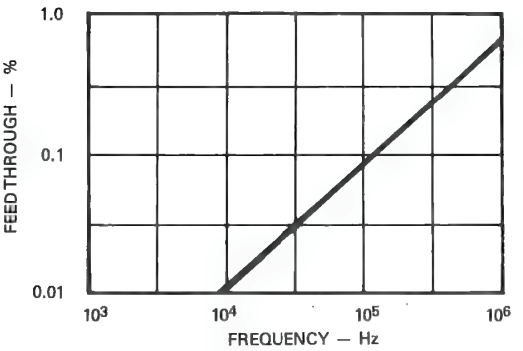


Figure 4. Feedthrough Error vs. Frequency

Application Hints

Linearity depends on the voltage at I_{OUT1} and I_{OUT2} (pin 1 and pin 2) being exactly equal to GND (pin 3) and to the output amplifier's non-inverting (+) input. Careful PC board layout and adjustment and selection of the amplifier's offset voltage and bias current are necessary.

The input structures of some high speed operational amplifiers can attempt to draw substantial current during switch-on. Schottky diodes should be used in these circumstances to prevent exceeding the absolute maximum rating for V_{OUT1} and V_{OUT2}.

The power supply should be carefully checked for noise, which would affect performance, and overshoot which could damage the device.

Unused digital inputs must always be grounded or tied to V_{DD} to ensure correct operation. Particular care should be taken when digital inputs are routed to another PC card. It is recommended that inputs open-circuited when PC cards are disconnected be taken to V_{DD} or GND via high value (1MΩ) resistors to prevent the buildup of static charge.

Circuit Description

The 8640, 8641, 12-bit multiplying D/A converters consist of a highly stable thin film R-2R ladder and twelve CMOS current switches on a monolithic chip. Most applications require the addition of only an output operational amplifier and a voltage or current reference.

The simplified D/A circuit is shown in Figure 5. An inverted R-2R ladder structure is used—that is, the binarily weighted currents are switched between the I_{OUT1} and the I_{OUT2} bus lines thus maintaining a constant current in each ladder leg independent of the switch state.

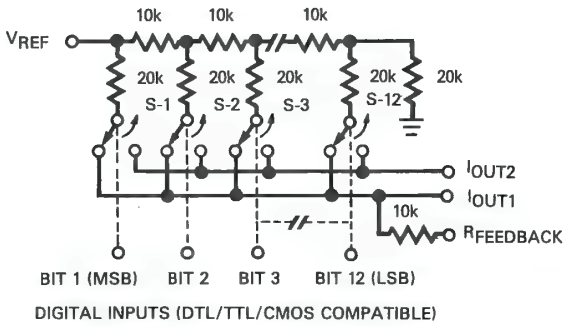


Figure 5. D/A Functional Diagram (Inputs "HIGH")

One of the CMOS current switches is shown in Figure 6. The geometries of devices 1, 2 and 3 are optimized to make the digital control inputs DTL/TTL/CMOS compatible over the full military temperature range. The input stage drives two inverters (devices 4, 5, 6 and 7) which in turn drive the two output N-channels. The "ON" resistances of the switches are binarily scaled so the voltage drop across each switch is the same. For example, switch 1 of Figure 5 was designed for an

"ON" resistance of 10 ohms, switch 2 of 20 ohms and so on. For a 10V reference input, the current through switch 1 is 0.5mA, the current through switch 2 is 0.25mA, and so on, thus maintaining a constant 5mV drop across each switch. It is essential that each switch voltage drop be equal if the binarily weighted current division property of the ladder is to be maintained.

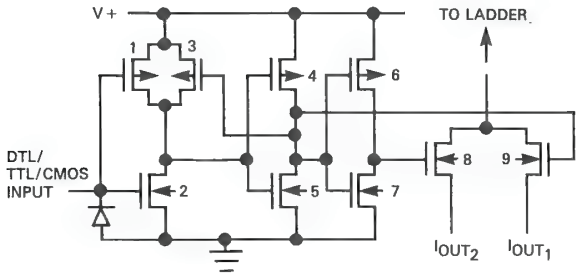


Figure 6. CMOS Switch

Equivalent Circuit Analysis

The equivalent circuits for all digital inputs high and all digital inputs low are shown in Figures 7 and 8. In Figure 7 with all digital inputs low, the reference current is switched to I_{OUT2}. The current source $I_{LEAKAGE}$ is composed of surface and junction leakages to the substrate while the 1/4096 current source represents a constant 1-bit current drain through the termination resistor on the R-2R ladder. The "ON" capacitance of the output N-channel switch is 200pF, as shown on the I_{OUT2} terminal. Analysis of the circuit for all digital inputs high, as shown in Figure 8, is similar to Figure 7; however, the "ON" switches are now on terminal I_{OUT1}, hence the 200pF at that terminal.

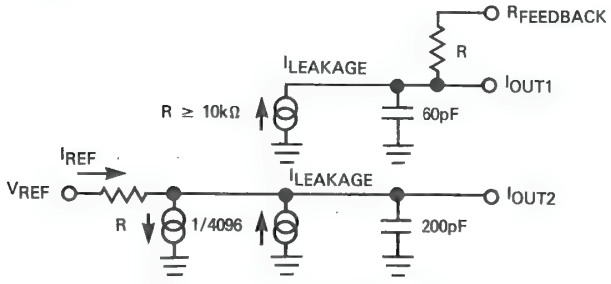


Figure 7. DIA Equivalent Circuit — All Digital Inputs Low

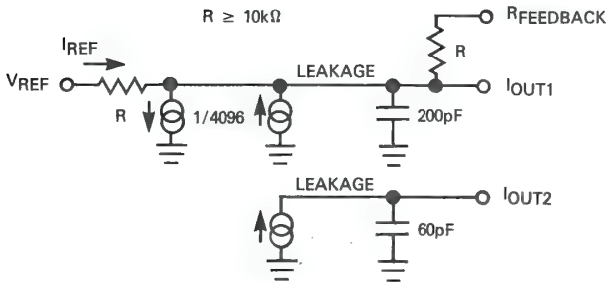


Figure 8. DIA Equivalent Circuit — All Digital Inputs High

Dynamic Performance

Output Impedance

The preceding circuit analysis shows that the output capacitance is dependent upon the digital code, as is the output resistance. Looking back into I_{OUT1} the resistance varies between 10kΩ ($R_{FEEDBACK}$ alone) and 5kΩ (R_F in parallel with the 10kΩ network resistance.)

This variation affects both static accuracy and dynamic performance. The effect on static accuracy is further considered on pages 5 and 6. The dynamic performance of the D/A will depend upon the gain and phase stability of the output amplifier, together with the optimum choice of PC board layout and decoupling components.

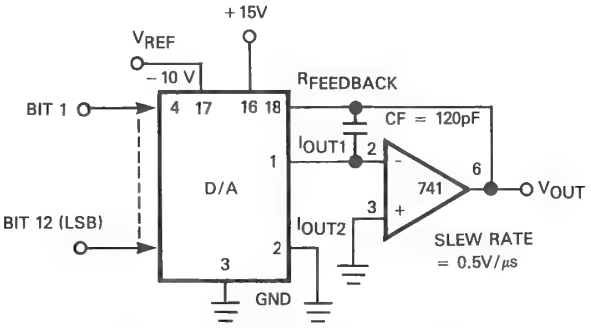


Figure 9. DAC Circuit Using 741 Op Amp

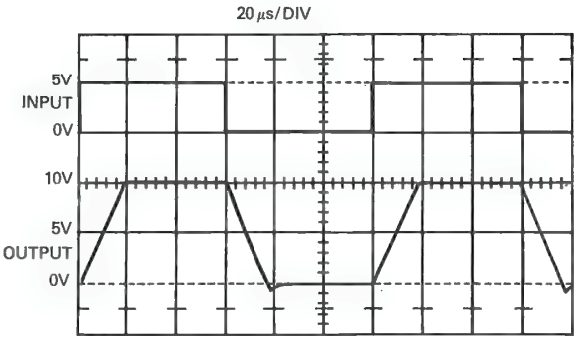


Figure 10. Output Waveform with 741 Op Amp

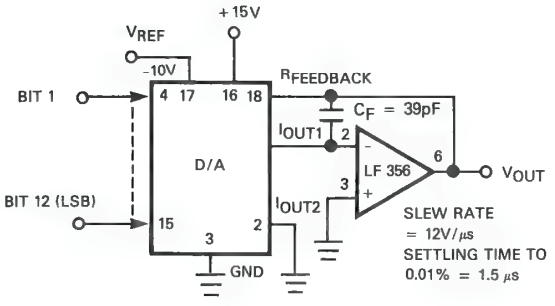


Figure 11. DAC Circuit Using LF356 Op Amp

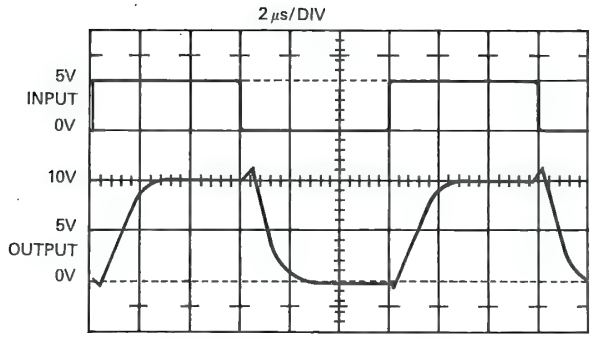


Figure 12. Output Waveform with LF 356 Op Amp

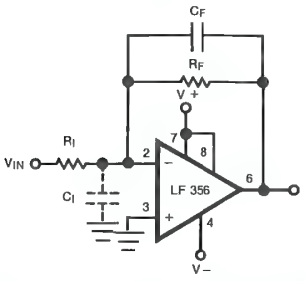


Figure 12A. Optimizing Settling Time

The capacitance seen at the inverting input of the op amp interacts with the feedback elements and creates an undesirable high frequency pole. In order to optimize the settling time and step response of the entire D/A system, a compensation capacitor, C_F, needs to be added such that $R_IC_I \cong R_FC_F$. C_I is equal to the sum of the op amp input capacitance plus the D/A output capacitance and the layout capacitance. The final value of C_F is best determined by actual lab testing.

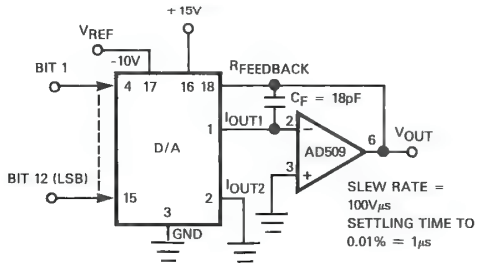


Figure 13. DAC Circuit Using AD509

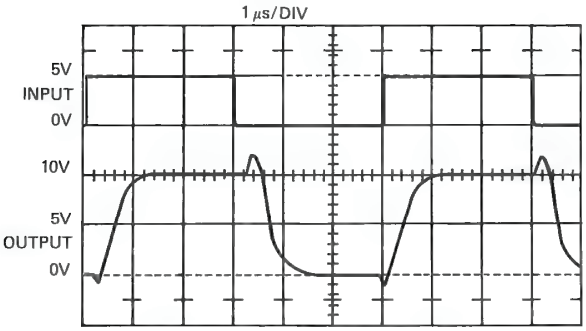


Figure 14. Output Waveform with AD509 Op Amp

The circuits and waveforms shown in Figures 9 to 14 are representative of the three principal types of output amplifiers: a general purpose low drift (741), a fast settling, high speed, low cost op amp (LF 356), and a fast settling unit (AD509).

Points to remember when applying high speed amplifiers include:

1. Protection diodes as shown in Figures 15 and 16.
2. Phase compensation for the DAC's output capacitance (C_F).
3. Power supply decoupling and correct grounding.

Applications

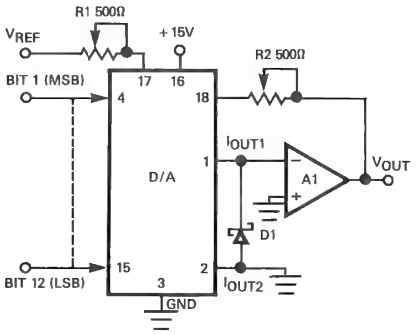


Figure 15. Unipolar Binary Operation

Unipolar Binary Operation

The connections required for unipolar digital binary operation are shown above. V_{REF} may be positive or negative so 2-quadrant multiplication may be performed. Schottky diode D1 (HP5082-2811, IN5817, MBR120P or equivalent) protects I_{OUT1} from negative excursions which could damage the device. This precaution is only necessary with certain high speed amplifiers.

Bipolar (4-Quadrant) Binary Operation

The digital input is offset binary coded and multiplies V_{REF} according to Table 2. Resistors R1 and R2 should be equal within 0.1% at all temperatures, but need not track the resistors within the DAC. D1 and D2 perform the same function as in Figure 15. Network R3, R4 and R5 sum ½LSB of current into I_{OUT2} to ensure correct coding at zero.

R1 or R2 can be adjusted to produce the outputs shown in Table 1. However, it is recommended that when the application permits it R1 and R2 be omitted. The typical gain error in this condition is 0.3% of full scale. The offset voltage of amplifier A1 should be adjusted to less than 0.5mV over the temperature range.

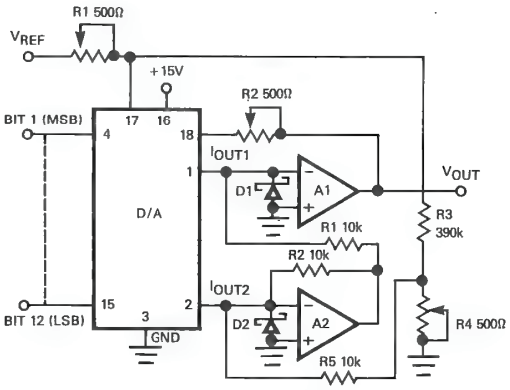


Figure 16. Bipolar (4-Quadrant) Binary Operation

Digital Input	Nominal Analog Output
1 1 1 1 1 1 1 1 1 1 1 1	$-0.99975\ V_{REF}$
1 0 0 0 0 0 0 0 0 0 0 0	$-0.50000\ V_{REF}$
0 1 0 0 0 0 0 0 0 0 0 0	$-0.25000\ V_{REF}$
0 0 0 0 0 0 0 0 0 0 0 0	0

Table 1. Code Table for Unipolar Operation (Figure 15)

Digital Input	Nominal Analog Output
1 1 1 1 1 1 1 1 1 1 1 1	$-0.99951\ V_{REF}$
1 0 0 0 0 0 0 0 0 0 0 1	$-0.00049\ V_{REF}$
1 0 0 0 0 0 0 0 0 0 0 0	0
0 1 0 0 0 0 0 0 0 0 0 0	$+0.50000\ V_{REF}$
0 0 0 0 0 0 0 0 0 0 0 0	$+1.00000\ V_{REF}$

Table 2. Code Table for Bipolar Operation (Figure 16)

Amplifiers A1 and A2 should be adjusted to an input offset of less than 0.1mV and should be better than 0.5mV over the temperature range. With V_{REF} set to approximately 10V, R4 should be adjusted so that with code 100000000000 V_{OUT} = 0V ±0.2mV. R1 or R2 should be adjusted so that with code 000000000000 $V_{OUT} = V_{REF}$.

As with the unipolar circuit R1 and R2 can be omitted, with a resulting typical gain error of 0.3% of full scale. R4 may be replaced by a 100Ω fixed resistor. In this case, the typical zero error is 0.015% of F.S.R.

Output Amplifier Considerations

It has already been pointed out that the DAC output resistance varies with the digital code. The effect this has on static accuracy will now be considered.

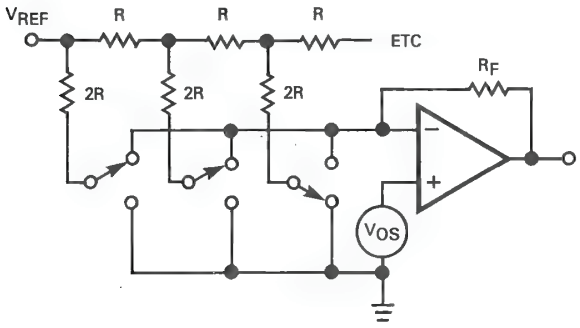


Figure 17. Output Amplifier

$$\text{The error voltage} = V_{OS}\left(1 + \frac{R_F}{R_O}\right)$$

R_O is a function of the digital code.
$R_O \cong 10k\Omega$ for any more than 4-bits Logic 1.
$R_O \cong 30k\Omega$ for any single bit Logic 1.

The gain for offset, therefore, changes as follows:

$$\text{At code 001111111111 } V_{ERROR1} = V_{OS}\left(1 + \frac{10k}{10k}\right) = 2\,V_{OS}$$

$$\text{At code 010000000000 } V_{ERROR2} = V_{OS}\left(1 + \frac{10k}{30k}\right) = \frac{4}{3}\,V_{OS}$$

The error difference is therefore $\frac{2}{3}\,V_{OS}$.

Since, for a 12-bit resolution DAC, one LSB has a weight (for V_{REF} = 10V) of 2.5mV, it is clearly important that V_{OS} be nulled, either using the amplifier's nulling facility or an external network.

It is important to realize that an offset can be caused by including the usual bias current compensation resistor in the amplifier's non-inverting input terminal. This should not be used. Instead the amplifier should have a bias current which is low over the temperature range of interest, and should certainly not exceed 75nA.

Analog/Digital Division

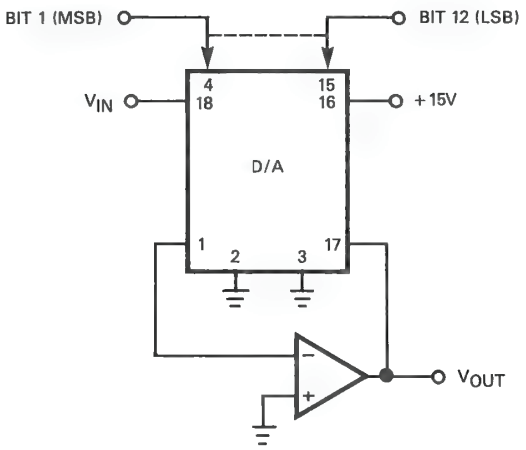


Figure 18. Analog/Digital Divider

With the D/A connected in its normal multiplying configuration shown in Figure 15, the transfer function is

$$V_O = -V_{IN}\left(\frac{A_1}{2^1} + \frac{A_2}{2^2} + \frac{A_3}{2^3} + \ldots . \frac{A_{12}}{A^{12}}\right)$$

where the coefficients A_X assume a value of 1 for an ON bit and 0 for an OFF bit.

By connecting the DAC in the feedback of an operational amplifier, as shown in Figure 18, the transfer function becomes

$$V_O = \left(\frac{-V_{IN}}{\frac{A_1}{2^1} + \frac{A_2}{2^2} + \frac{A_3}{2^3} + \ldots . \frac{A_{12}}{2^{12}}}\right)$$

This is division of an analog variable (V_{IN}) by a digital word. With all bits off, the amplifier output goes to the supply rails since division by zero is not defined. With the LSB (Bit 12) ON, the gain is 4096. With all bits ON, the gain is 1 (±1LSB).

Test Circuits

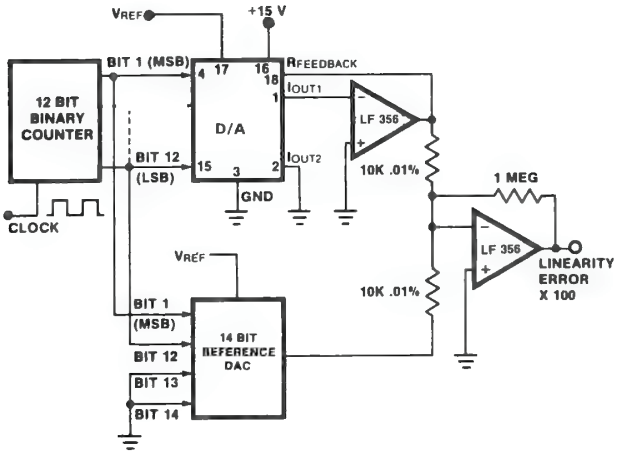


Figure 19. Nonlinearity

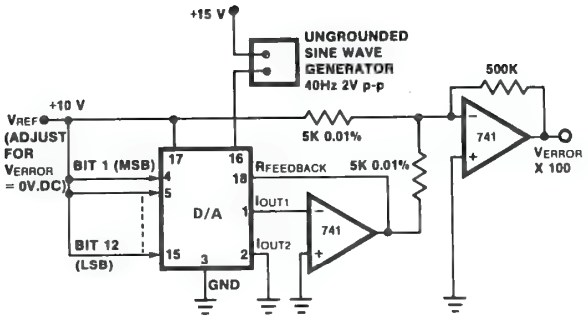


Figure 22. Power Supply Rejection

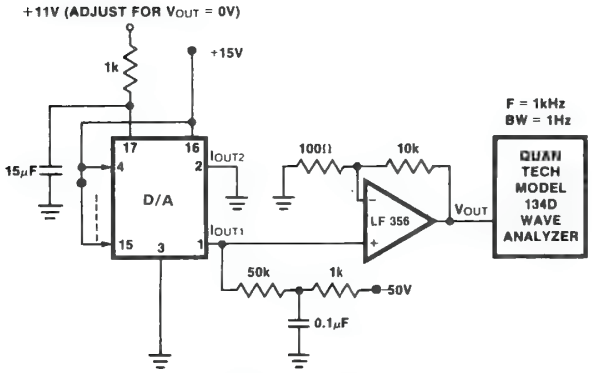


Figure 20. Noise

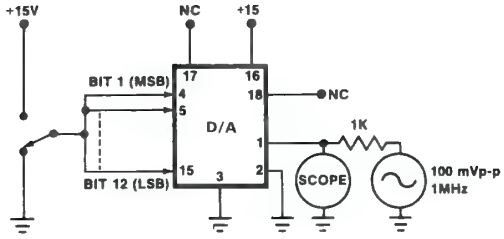


Figure 23. Output Capacitance

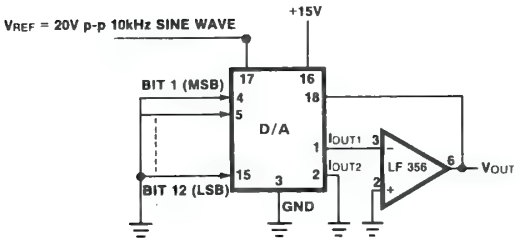


Figure 21. Feedthrough Error

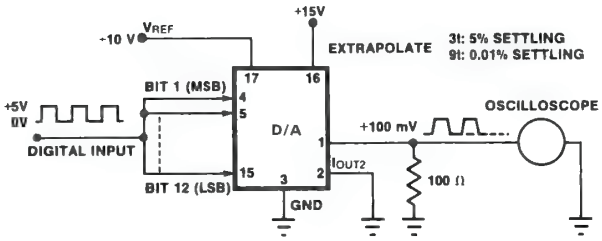


Figure 24. Output Current Settling Time

Specification Definitions

Nonlinearity: Error caused by deviation of the DAC transfer function from a best straight line fit. Normally expressed as a percentage of full scale. For a multiplying DAC, this should hold true over the entire V_{REF} range.

Resolution: Value of the LSB. For example, a unipolar converter with n bits has a resolution of (2^{-n}) (V_{REF}). A bipolar converter of n bits has a resolution of $[2^{-(n-1)}]$ $[V_{REF}]$. Resolution in no way implies linearity.

Settling Time: Time required for the output of the DAC to settle to within ½ LSB for a given digital input change, i.e., 0 to Full Scale.

Gain: Ratio of output voltage, from an external op amp, to the V_{REF} input voltage when the DAC's internal feedback resistor is used.

Feedthrough Error: Error caused by capacitive coupling from V_{REF} to the output with all switches OFF.

Output Capacitance: Capacity from I_{OUT1} and I_{OUT2} to ground.

Output Leakage Current: Current which appears on I_{OUT1} terminal with all digital inputs LOW or on I_{OUT2} terminal when all inputs are HIGH.

Digital/Synchro Converter

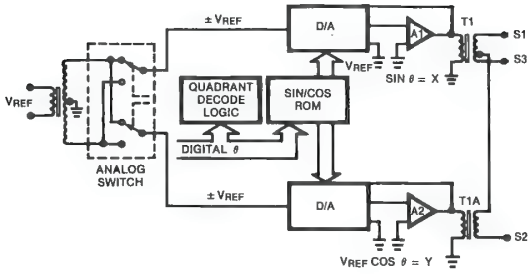


Figure 25. 14-Bit Digital to Synchro Converter

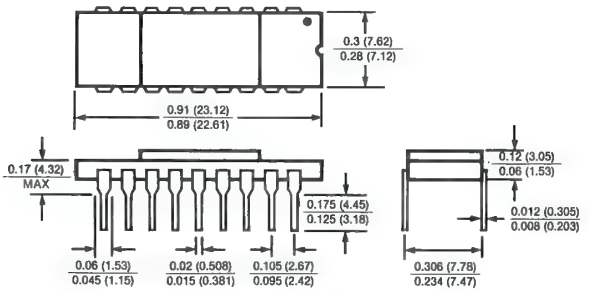
The low cost and high accuracy available from the Teledyne Semiconductor 8640, 8641 together with their bipolar multiplying capability, are exploited fully in the circuit of Figure 25. V_{REF} is normally 400Hz but by replacing the transformers with dc-coupled circuits coordinate transformation may be performed.

The SIN/COS ROM is readily available at low cost and the Analog switch enables greater resolution to be obtained.

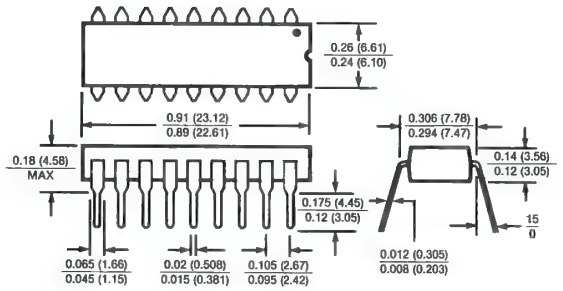
Resolver-to-synchro transformation is performed by the Scott connected pair T1 and T1A. The power available to the load connected to S1, S2 and S3 is determined by the amplifiers A1 and A2. A particular advantage of the circuit shown in Figure 19 is that it is invariant with respect to θ, and may be used to directly drive equipment such as CRT displays.

Physical Dimensions

Dimensions shown in inches and (mm).



N Package
18-Pin Ceramic DIP



J Package
18-Pin Plastic DIP

NOTE: Pin 1 indicated by adjacent dot, indent or end notch.