

GD54/74LS174

HEX D-TYPE FLIP-FLOPS, COMMON CLEAR

Feature

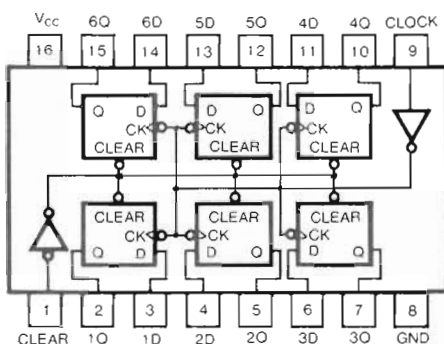
- Contains Six Flip-Flops with Single-Rail Outputs
- Buffered Clock and Direct Clear Inputs
- Individual Data Input to Each Flip-Flop
- Application Include: Buffer/Storage Registers
Shift Registers
Pattern Generators

Description

These monolithic, positive-edge triggered flip-flops utilize TTL circuitry to implement D-type flip-flop logic.

Information at the D inputs meeting the setup time requirements is transferred to the outputs on the positive going edge of the clock pulse. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going pulse. When the clock input is at either the high or low level, the D input signal has no effect at the output.

Pin Configuration



Suffix-Blank: Plastic Dual In Line Package
Suffix-J : Ceramic Dual In Line Package

Function Table (Each F/F)

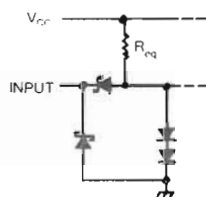
INPUTS			OUTPUTS
CLEAR	CLOCK	D	Q
L	X	X	L
H	↑*	H	H
H	↑*	L	L
H	L	X	Q ₀

*↑=transition from low to high level.

*Q₀=the level of Q before the indicated steady-state input conditions were established

Schematics of Inputs and Outputs

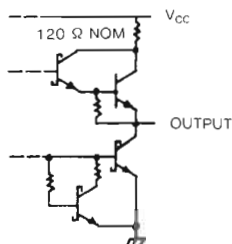
EQUIVALENT OF EACH INPUT



Clock $R_{inq} = 17 \text{ k}\Omega \text{ NOM}$

Clear D $R_{inq} = 20 \text{ k}\Omega \text{ NOM}$

TYPICAL OF ALL OUTPUTS



Absolute Maximum Ratings

- Supply voltage, Vcc 7V
- Input voltage 7V
- Operating free-air temperature range 54LS -55°C to 125°C
74LS 0°C to 70°C
- Storage temperature range -65°C to 150°C

Recommended Operating Conditions

SYMBOL	PARAMETER		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	54	4.5	5	5.5	V
		74	4.75	5	5.25	
I_{OH}	High-level output current	54, 74			-400	μA
I_{OL}	Low-level output current	54			4	mA
		74			8	
f_{clock}	Clock frequency		0		30	MHz
t_w	Width of clock or clear pulse		20			ns
t_{su}	Set up time	Data input	20			ns
		Clear inactive-state	25			
t_h	Data hold time		5			ns
T_A	Operating free-air temperature	54	-55		125	$^{\circ}C$
		74	0		70	

Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP (Note 1)	MAX	UNIT
V_{IH}	High-level input voltage		2			V
V_{IL}	Low-level input voltage	54			0.7	V
		74			0.8	
V_{IK}	Input clamp voltage	$V_{CC} = \text{Min}, I_I = -18 \text{ mA}$			-1.5	V
V_{OH}	High-level output voltage	$V_{CC} = \text{Min}, V_{IL} = \text{Max}$	54	2.5	3.4	V
		$I_{OH} = \text{Max}, V_{IH} = \text{Min}$	74	2.7	3.4	
V_{OL}	Low-level output voltage	$V_{CC} = \text{Min}, V_{IL} = \text{Max}$	54, 74	0.25	0.4	V
		$V_{IH} = \text{Min}, I_{OL} = 8 \text{ mA}$	74	0.35	0.5	
I_I	Input current at maximum input voltage	$V_{CC} = \text{Max}, V_I = 7 \text{ V}$			0.1	mA
I_{IH}	High-level input current	$V_{CC} = \text{Max}, V_I = 2.7 \text{ V}$			20	μA
I_{IL}	Low-level input current	$V_{CC} = \text{Max}, V_I = 0.4 \text{ V}$			-0.4	mA
I_{OS}	Short-circuit output current	$V_{CC} = \text{Max}$ (Note 2)	-20		-100	mA
I_{CC}	Supply current	$V_{CC} = 5.25 \text{ V}$, (Note 3)		16	26	mA

Note 1: All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^{\circ}C$.

Note 2: Not more than one output should be shorted at a time, and duration should not exceed one second.

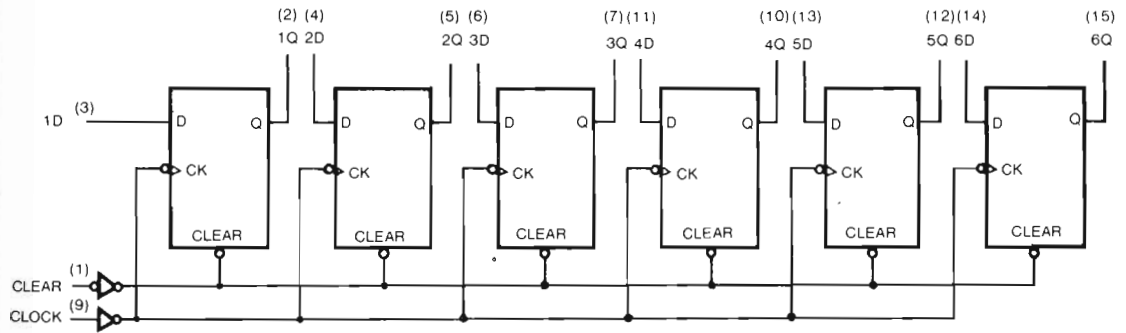
Note 3: With all outputs open, 4.5V applied to the serial input, all other inputs except the CLOCK grounded, I_{CC} is measured after a momentary ground, then 4.5V, is applied to the CLOCK

Switching Characteristics, $V_{CC} = 5 \text{ V}$, $T_A = 25^{\circ}C$

SYMBOL	PARAMETER	TEST CONDITION#	MIN	TYP	MAX	UNIT
f_{max}	Maximum clock frequency	$C_L = 15 \text{ pF}, R_L = 2 \text{ k}\Omega$	30	40		MHz
t_{PHL}	Propagation delay time, high-to-low-level output from clear			23	35	ns
t_{PLH}	Propagation delay time, low-to-high-level output from clock			20	30	ns
t_{PHL}	Propagation delay time, high-to-low-level output from clock			21	30	ns

#For load circuit and voltage waveforms, see page 3-11.

Function Block Diagram



Application Example

(6-BIT SHIFT REGISTER)

