



Integrated Device Technology, Inc.

FAST CMOS 20-BIT TRANSPARENT LATCHES

IDT54/74FCT16841AT/BT/CT/ET
IDT54/74FCT162841AT/BT/CT/ET

FEATURES:

- **Common features:**
 - 0.5 MICRON CMOS Technology
 - **High-speed, low-power CMOS replacement for ABT functions**
 - **Typical $t_{sk(o)}$ (Output Skew) < 250ps**
 - **Low input and output leakage $\leq 1\mu A$ (max.)**
 - ESD > 2000V per MIL-STD-883, Method 3015; > 200V using machine model (C = 200pF, R = 0)
 - Packages include 25 mil pitch SSOP, 19.6 mil pitch TSSOP, 15.7 mil pitch TVSOP and 25 mil pitch Cerpack
 - Extended commercial range of -40°C to +85°C
 - $V_{CC} = 5V \pm 10\%$
- **Features for FCT16841AT/BT/CT/ET:**
 - High drive outputs (-32mA I_{OH} , 64mA I_{OL})
 - Power off disable outputs permit "live insertion"
 - Typical VOLP (Output Ground Bounce) < 1.0V at $V_{CC} = 5V$, $T_A = 25^\circ C$
- **Features for FCT162841AT/BT/CT/ET:**
 - Balanced Output Drivers: $\pm 24mA$ (commercial), $\pm 16mA$ (military)
 - Reduced system switching noise
 - Typical VOLP (Output Ground Bounce) < 0.6V at $V_{CC} = 5V$, $T_A = 25^\circ C$

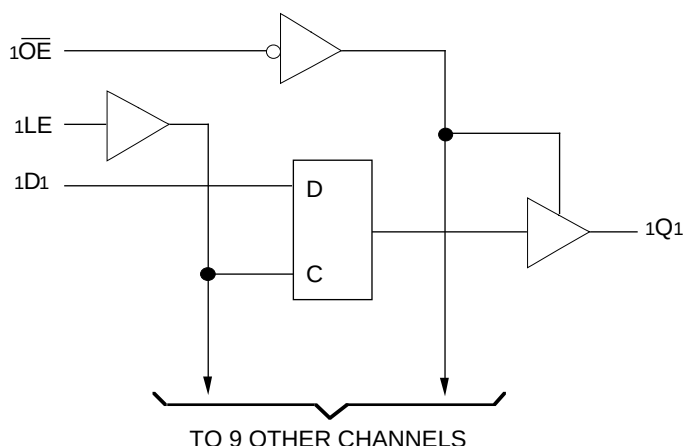
DESCRIPTION:

The FCT16841AT/BT/CT/ET and FCT162841AT/BT/CT/ET 20-bit transparent D-type latches are built using advanced dual metal CMOS technology. These high-speed, low-power latches are ideal for temporary storage of data. They can be used for implementing memory address latches, I/O ports, and bus drivers. The Output Enable and Latch Enable controls are organized to operate each device as two 10-bit latches or one 20-bit latch. Flow-through organization of signal pins simplifies layout. All inputs are designed with hysteresis for improved noise margin.

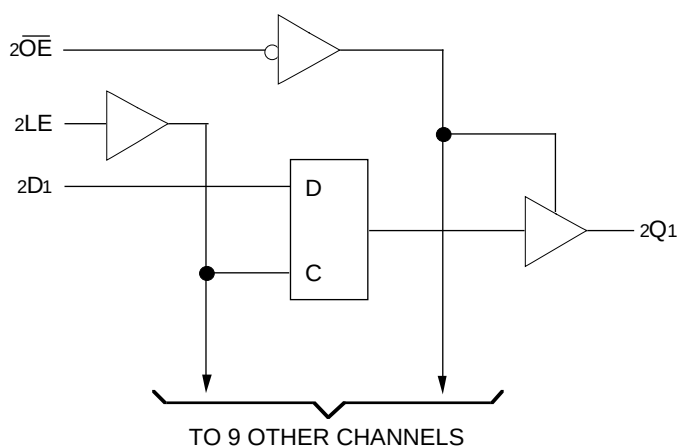
The FCT16841AT/BT/CT/ET are ideally suited for driving high-capacitance loads and low-impedance backplanes. The output buffers are designed with power off disable capability to allow "live insertion" of boards when used as backplane drivers.

The FCT162841AT/BT/CT/ET have balanced output drive with current limiting resistors. This offers low ground bounce, minimal undershoot, and controlled output fall times—reducing the need for external series terminating resistors. The FCT162841AT/BT/CT/ET are plug-in replacements for the FCT16841AT/BT/CT/ET and ABT16841 for on-board interface applications.

FUNCTIONAL BLOCK DIAGRAM



2556 drw 01



2556 drw 02

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MILITARY AND COMMERCIAL TEMPERATURE RANGES

JULY 1996

The image displays two pinout diagrams for the 2556 dual inverter, showing the top view of the package.

Left Diagram: SSOP/TSSOP/TVSOP TOP VIEW

This diagram shows the pinout for the SSOP/TSSOP/TVSOP package. The pins are numbered 1 through 28 on the left side and 56 through 29 on the right side. The central label is E56-1.

Right Diagram: CERPACK TOP VIEW

This diagram shows the pinout for the CERPACK package. The pins are numbered 1 through 28 on the left side and 56 through 29 on the right side. The central label is E56-1.

PIN DESCRIPTION

Pin Names	Description
xDx	Data Inputs
xLE	Latch Enable Input (Active HIGH)
x $\overline{\text{OE}}$	Output Enable Input (Active LOW)
xQx	3-State Outputs

2556 tbl 01

FUNCTION TABLE⁽¹⁾

Inputs			Outputs
xDx	xLE	x $\overline{\text{OE}}$	xQx
H	H	L	H
L	H	L	L
X	L	L	Q ⁽²⁾
X	X	H	Z

2556 tbl 02

NOTES:

1. H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
Z = High Impedance
2. Output level before xLE HIGH-to-LOW Transition.

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Symbol	Description	Max.	Unit
V _{TERM} ⁽²⁾	Terminal Voltage with Respect to GND	−0.5 to +7.0	V
V _{TERM} ⁽³⁾	Terminal Voltage with Respect to GND	−0.5 to V _{CC} +0.5	V
T _{STG}	Storage Temperature	−65 to +150	°C
I _{OUT}	DC Output Current	−60 to +120	mA

2556 lmk 03

NOTES:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. All device terminals except FCT162XXXT Output and I/O terminals.
3. Output and I/O terminals for FCT162XXXT.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter ⁽¹⁾	Conditions	Typ.	Max.	Unit
C _{IN}	Input Capacitance	V _{IN} = 0V	3.5	6.0	pF
C _{OUT}	Output Capacitance	V _{OUT} = 0V	3.5	8.0	pF

2556 lmk 04

NOTE:

1. This parameter is measured at characterization but not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

Commercial: $T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$, $V_{CC} = 5.0\text{V} \pm 10\%$; Military: $T_A = -55^{\circ}\text{C}$ to $+125^{\circ}\text{C}$, $V_{CC} = 5.0\text{V} \pm 10\%$

Symbol	Parameter	Test Conditions ⁽¹⁾		Min.	Typ. ⁽²⁾	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Input HIGH Current (Input pins) ⁽⁵⁾	$V_{CC} = \text{Max.}$	$V_I = V_{CC}$	—	—	± 1	μA
	Input HIGH Current (I/O pins) ⁽⁵⁾			—	—	± 1	
I_{IL}	Input LOW Current (Input pins) ⁽⁵⁾		$V_I = \text{GND}$	—	—	± 1	
	Input LOW Current (I/O pins) ⁽⁵⁾			—	—	± 1	
I_{OZH}	High Impedance Output Current (3-State Output pins) ⁽⁵⁾	$V_{CC} = \text{Max.}$	$V_O = 2.7\text{V}$	—	—	± 1	μA
I_{OZL}			$V_O = 0.5\text{V}$	—	—	± 1	
V_{IK}	Clamp Diode Voltage	$V_{CC} = \text{Min.}$, $I_{IN} = -18\text{mA}$		—	-0.7	-1.2	V
I_{OS}	Short Circuit Current	$V_{CC} = \text{Max.}$, $V_O = \text{GND}$ ⁽³⁾		-80	-140	-225	mA
V_H	Input Hysteresis	—		—	100	—	mV
I_{CCL} I_{CCH} I_{CCZ}	Quiescent Power Supply Current	$V_{CC} = \text{Max.}$, $V_{IN} = \text{GND}$ or V_{CC}		—	5	500	μA

2556 Ink 05

OUTPUT DRIVE CHARACTERISTICS FOR FCT16841T

Symbol	Parameter	Test Conditions ⁽¹⁾		Min.	Typ. ⁽²⁾	Max.	Unit
I_O	Output Drive Current	$V_{CC} = \text{Max.}$, $V_O = 2.5\text{V}$ ⁽³⁾		-50	—	-180	mA
V_{OH}	Output HIGH Voltage	$V_{CC} = \text{Min.}$ $V_{IN} = V_{IH}$ or V_{IL}	$I_{OH} = -3\text{mA}$	2.5	3.5	—	V
			$I_{OH} = -12\text{mA MIL.}$ $I_{OH} = -15\text{mA COM'L.}$	2.4	3.5	—	V
			$I_{OH} = -24\text{mA MIL.}$ $I_{OH} = -32\text{mA COM'L.}$ ⁽⁴⁾	2.0	3.0	—	V
V_{OL}	Output LOW Voltage	$V_{CC} = \text{Min.}$ $V_{IN} = V_{IH}$ or V_{IL}	$I_{OL} = 48\text{mA MIL.}$ $I_{OL} = 64\text{mA COM'L.}$	—	0.2	0.55	V
I_{OFF}	Input/Output Power Off Leakage ⁽⁵⁾	$V_{CC} = 0\text{V}$, V_{IN} or $V_O \leq 4.5\text{V}$		—	—	± 1	μA

2556 Ink 06

OUTPUT DRIVE CHARACTERISTICS FOR FCT162841T

Symbol	Parameter	Test Conditions ⁽¹⁾		Min.	Typ. ⁽²⁾	Max.	Unit
I_{ODL}	Output LOW Current	$V_{CC} = 5\text{V}$, $V_{IN} = V_{IH}$ or V_{IL} , $V_{OUT} = 1.5\text{V}$ ⁽³⁾		60	115	200	mA
I_{ODH}	Output HIGH Current	$V_{CC} = 5\text{V}$, $V_{IN} = V_{IH}$ or V_{IL} , $V_{OUT} = 1.5\text{V}$ ⁽³⁾		-60	-115	-200	mA
V_{OH}	Output HIGH Voltage	$V_{CC} = \text{Min.}$ $V_{IN} = V_{IH}$ or V_{IL}	$I_{OH} = -16\text{mA MIL.}$ $I_{OH} = -24\text{mA COM'L.}$	2.4	3.3	—	V
V_{OL}	Output LOW Voltage	$V_{CC} = \text{Min.}$ $V_{IN} = V_{IH}$ or V_{IL}	$I_{OL} = 16\text{mA MIL.}$ $I_{OL} = 24\text{mA COM'L.}$	—	0.3	0.55	V

2556 Ink 07

NOTES:

- For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at $V_{CC} = 5.0\text{V}$, $+25^{\circ}\text{C}$ ambient.
- Not more than one output should be tested at one time. Duration of the test should not exceed one second.
- Duration of the condition can not exceed one second.
- The test limit for this parameter is $\pm 5\mu\text{A}$ at $T_A = -55^{\circ}\text{C}$.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions ⁽¹⁾		Min.	Typ. ⁽²⁾	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	$V_{CC} = \text{Max.}$ $V_{IN} = 3.4V^{(3)}$		—	0.5	1.5	mA
I_{CCD}	Dynamic Power Supply Current ⁽⁴⁾	$V_{CC} = \text{Max.}$ Outputs Open $\overline{xOE} = \text{GND}$ One Input Toggling 50% Duty Cycle	$V_{IN} = V_{CC}$ $V_{IN} = \text{GND}$	—	60	100	μA / MHz
I_C	Total Power Supply Current ⁽⁶⁾	$V_{CC} = \text{Max.}$ Outputs Open $f_i = 10\text{MHz}$ 50% Duty Cycle $\overline{xOE} = \text{GND}$ $xLE = V_{CC}$ One Bit Toggling	$V_{IN} = V_{CC}$ $V_{IN} = \text{GND}$	—	0.6	1.5	mA
			$V_{IN} = 3.4V$ $V_{IN} = \text{GND}$	—	0.9	2.3	
		$V_{CC} = \text{Max.}$ Outputs Open $f_i = 2.5\text{MHz}$ 50% Duty Cycle $\overline{xOE} = \text{GND}$ $xLE = V_{CC}$ Twenty Bits Toggling	$V_{IN} = V_{CC}$ $V_{IN} = \text{GND}$	—	3.0	5.5 ⁽⁵⁾	
			$V_{IN} = 3.4V$ $V_{IN} = \text{GND}$	—	8.0	20.5 ⁽⁵⁾	

NOTES:

2556 tbl 08

- For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at $V_{CC} = 5.0V$, $+25^\circ\text{C}$ ambient.
- Per TTL driven input ($V_{IN} = 3.4V$). All other inputs at V_{CC} or GND.
- This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
- Values for these conditions are examples of the I_C formula. These limits are guaranteed but not tested.
- $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
 $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP} N_{CP} / 2 + f_i N_i)$
 $I_{CC} = \text{Quiescent Current (} I_{CCL}, I_{CCH} \text{ and } I_{CCZ} \text{)}$
 $\Delta I_{CC} = \text{Power Supply Current for a TTL High Input (} V_{IN} = 3.4V \text{)}$
 $D_H = \text{Duty Cycle for TTL Inputs High}$
 $N_T = \text{Number of TTL Inputs at } D_H$
 $I_{CCD} = \text{Dynamic Current Caused by an Input Transition Pair (HLH or LHL)}$
 $f_{CP} = \text{Clock Frequency for Register Devices (Zero for Non-Register Devices)}$
 $N_{CP} = \text{Number of Clock Inputs at } f_{CP}$
 $f_i = \text{Input Frequency}$
 $N_i = \text{Number of Inputs at } f_i$

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Symbol	Parameter	Condition ⁽¹⁾	FCT16841AT/162841AT				FCT16841BT/162841BT				Unit
			Com'l.		Mil.		Com'l.		Mil.		
			Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	
tPLH tPHL	Propagation Delay xDx to xQx (LE = HIGH)	CL = 50pF RL = 500Ω	1.5	9.0	1.5	10.0	1.5	6.5	1.5	7.5	ns
		CL = 300pF ⁽⁵⁾ RL = 500Ω	1.5	13.0	1.5	15.0	1.5	13.0	1.5	15.0	
tPLH tPHL	Propagation Delay xLE to xQx	CL = 50pF RL = 500Ω	1.5	12.0	1.5	13.0	1.5	8.0	1.5	10.5	ns
		CL = 300pF ⁽⁵⁾ RL = 500Ω	1.5	16.0	1.5	20.0	1.5	15.5	1.5	18.0	
tPZH tPZL	Output Enable Time xOE to xQx	CL = 50pF RL = 500Ω	1.5	11.5	1.5	13.0	1.5	8.0	1.5	8.5	ns
		CL = 300pF ⁽⁵⁾ RL = 500Ω	1.5	23.0	1.5	25.0	1.5	14.0	1.5	15.0	
tPHZ tPLZ	Output Disable Time xOE to xQx	CL = 5pF ⁽⁵⁾ RL = 500Ω	1.5	7.0	1.5	9.0	1.5	6.0	1.5	6.5	ns
		CL = 50pF RL = 500Ω	1.5	8.0	1.5	10.0	1.5	7.0	1.5	7.5	
tsu	Set-Up Time HIGH or LOW, xDx to xLE	CL = 50pF RL = 500Ω	2.5	—	2.5	—	2.5	—	2.5	—	ns
th	Hold Time HIGH or LOW, xDx to xLE		2.5	—	3.0	—	2.5	—	2.5	—	ns
tw	xLE Pulse Width HIGH		4.0 ⁽⁴⁾	—	5.0	—	4.0 ⁽⁴⁾	—	4.0 ⁽⁴⁾	—	ns
tsk(0)	Output skew ⁽³⁾		—	0.5	—	0.5	—	0.5	—	0.5	ns

NOTES:

- See test circuit and waveforms.
- Minimum limits are guaranteed but not tested on Propagation Delays.
- Skew between any two outputs of the same package switching in the same direction. This parameter is guaranteed by design.
- This limit is guaranteed but not tested.
- This condition is guaranteed but not tested.

2556 tbl 09

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Symbol	Parameter	Condition ⁽¹⁾	FCT16841CT/162841CT				FCT16841ET/162841ET				Unit
			Com'l.		Mil.		Com'l.		Mil.		
			Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	
tPLH tPHL	Propagation Delay xDx to xQx (LE = HIGH)	CL = 50pF RL = 500Ω	1.5	5.5	1.5	6.3	1.5	3.4	—	—	ns
		CL = 300pF ⁽⁵⁾ RL = 500Ω	1.5	13.0	1.5	15.0	1.5	7.5	—	—	
tPLH tPHL	Propagation Delay xLE to xQx	CL = 50pF RL = 500Ω	1.5	6.4	1.5	6.8	1.5	3.7	—	—	ns
		CL = 300pF ⁽⁵⁾ RL = 500Ω	1.5	15.0	1.5	16.0	1.5	7.5	—	—	
tpZH tpZL	Output Enable Time xOE to xQx	CL = 50pF RL = 500Ω	1.5	6.5	1.5	7.3	1.5	4.4	—	—	ns
		CL = 300pF ⁽⁵⁾ RL = 500Ω	1.5	12.0	1.5	13.0	1.5	9.0	—	—	
tpHZ tPLZ	Output Disable Time xOE to xQx	CL = 5pF ⁽⁵⁾ RL = 500Ω	1.5	5.7	1.5	6.0	1.5	3.6	—	—	ns
		CL = 50pF RL = 500Ω	1.5	6.0	1.5	6.3	1.5	3.6	—	—	
tsu	Set-Up Time HIGH or LOW, xDx to xLE	CL = 50pF RL = 500Ω	2.5	—	2.5	—	1.0	—	—	—	ns
th	Hold Time HIGH or LOW, xDx to xLE		2.5	—	2.5	—	1.0	—	—	—	ns
tw	xLE Pulse Width HIGH		4.0 ⁽⁴⁾	—	4.0 ⁽⁴⁾	—	3.0 ⁽⁴⁾	—	—	—	ns
tsk(0)	Output skew ⁽³⁾		—	0.5	—	0.5	—	0.5	—	—	ns

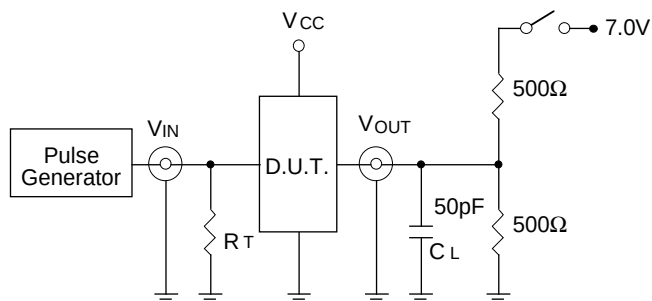
NOTES:

- See test circuit and waveforms.
- Minimum limits are guaranteed but not tested on Propagation Delays.
- Skew between any two outputs of the same package switching in the same direction. This parameter is guaranteed by design.
- This limit is guaranteed but not tested.
- This condition is guaranteed but not tested.

2556 tbl 10

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUITS FOR ALL OUTPUTS



2556 drw 05

SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Tests	Open

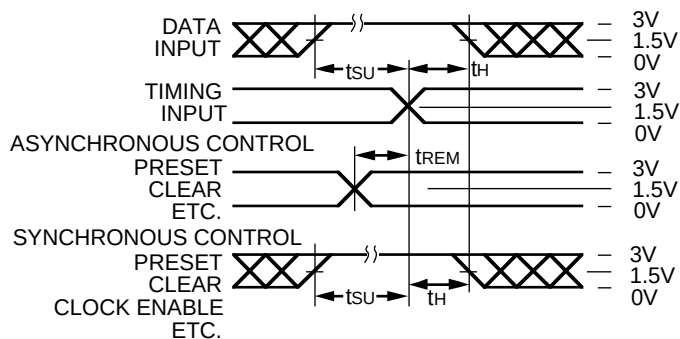
2556 Ink 11

DEFINITIONS:

C_L = Load capacitance: includes jig and probe capacitance.

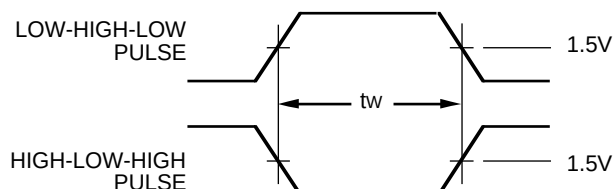
R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

SET-UP, HOLD AND RELEASE TIMES



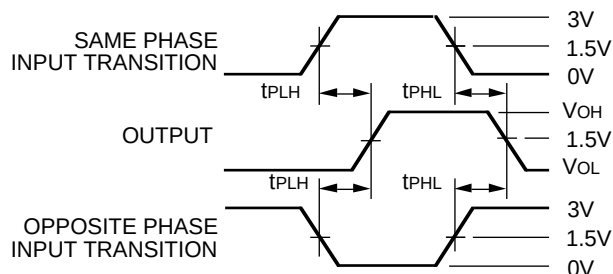
2556 drw 06

PULSE WIDTH



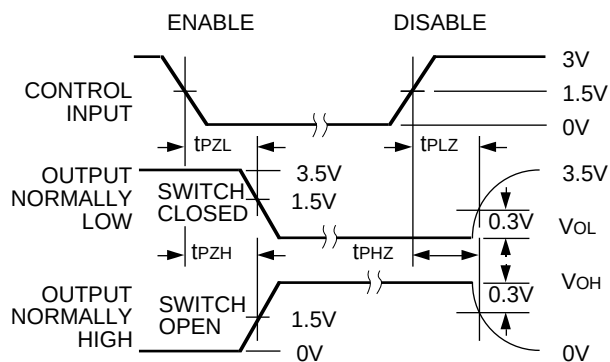
2556 drw 07

PROPAGATION DELAY



2556 drw 08

ENABLE AND DISABLE TIMES



2556 drw 09

NOTES:

- Diagram shown for input Control Enable-LOW and input Control Disable-HIGH
- Pulse Generator for All Pulses: Rate $\leq 1.0\text{MHz}$; $t_r \leq 2.5\text{ns}$; $t_f \leq 2.5\text{ns}$

ORDERING INFORMATION

IDT	XX	FCT	XXXX	X	X		
Temp. Range		Device Type		Package	Process		
					Blank B	Commercial MIL-STD-883, Class B	
					PV	Shrink Small Outline Package (SO56-1)	
					PA	Thin Shrink Small Outline Package (SO56-2)	
					PF	Thin Very Small Outline Package (SO56-3)	
					E	CERPACK (E56-1)	
					16841AT	Non-Inverting 20-Bit Transparent Latch	
					16841BT		
					16841CT		
					16841ET		
					162841AT		
					162841BT		
					162841CT		
					162841ET		
					54	-55°C to +125°C	
					74	-40°C to +85°C	

2556 drw 10