

# DATA SHEET

## **74LVC07A**

### Hex buffer with open-drain outputs

Product specification  
Supersedes data of 2003 Feb 25

2003 Nov 11

## Hex buffer with open-drain outputs

## 74LVC07A

## FEATURES

- 5 V tolerant inputs and outputs (open drain) for interfacing with 5 V logic
- Wide supply voltage range from 1.65 to 5.5 V
- CMOS low power consumption
- Direct interface with TTL levels
- Inputs accept voltages up to 5 V
- Complies with JEDEC standard no. 8-1A
- ESD protection:  
HBM EIA/JESD22-A114-A exceeds 2000 V  
MM EIA/JESD22-A115-A exceeds 200 V.

## DESCRIPTION

The 74LVC07A is a high-performance, low-power, low-voltage, Si-gate CMOS device, superior to most advanced CMOS compatible TTL families. Inputs can be driven from either 3.3 or 5 V devices. This feature allows the use of these devices as translators in a mixed 3.3 to 5 V environment.

The 74LVC07A provides six non-inverting buffers.

The outputs of the 74LVC07A are open drain and can be connected to other open-drain outputs to implement active-LOW wired-OR or active-HIGH wired-AND functions.

## QUICK REFERENCE DATA

GND = 0 V;  $T_{amb} = 25\text{ }^{\circ}\text{C}$ ;  $t_r = t_f \leq 2.5\text{ ns}$ .

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
$t_{PLZ}/t_{PZL}$	propagation delay nA to nY	$C_L = 50\text{ pF}$ ; $V_{CC} = 3.3\text{ V}$	2.2	ns
$C_I$	input capacitance		5.0	pF
$C_{PD}$	power dissipation capacitance per gate	$V_{CC} = 3.3\text{ V}$ ; notes 1 and 2	6.0	pF

## Note

1.  $C_{PD}$  is used to determine the dynamic power dissipation ( $P_D$  in  $\mu\text{W}$ ).

$$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

$f_i$  = input frequency in MHz;

$f_o$  = output frequency in MHz;

$C_L$  = output load capacitance in pF;

$V_{CC}$  = supply voltage in Volts;

$N$  = total load switching outputs;

$\Sigma(C_L \times V_{CC}^2 \times f_o)$  = sum of the outputs.

2. The condition is  $V_I = \text{GND to } V_{CC}$

## FUNCTION TABLE

See note 1.

INPUT	OUTPUT
nA	nY
L	L
H	Z

## Note

1. H = HIGH voltage level;  
L = LOW voltage level;  
Z = high-impedance OFF-state.

# Hex buffer with open-drain outputs

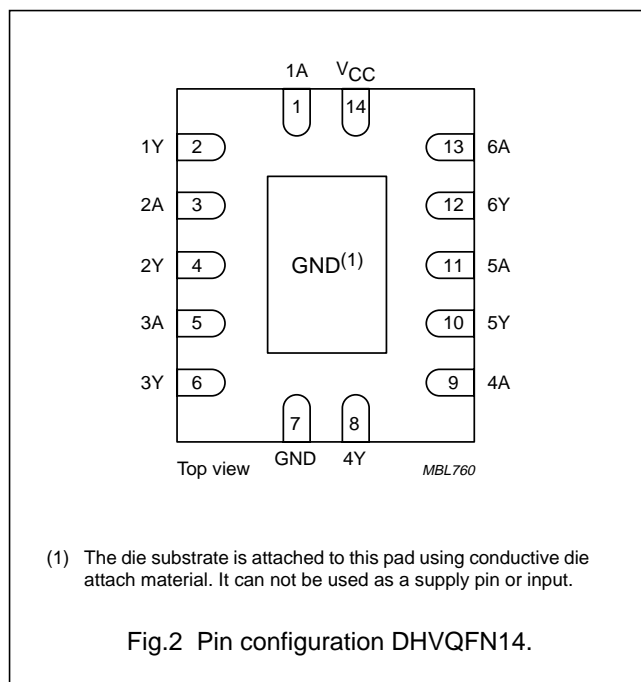
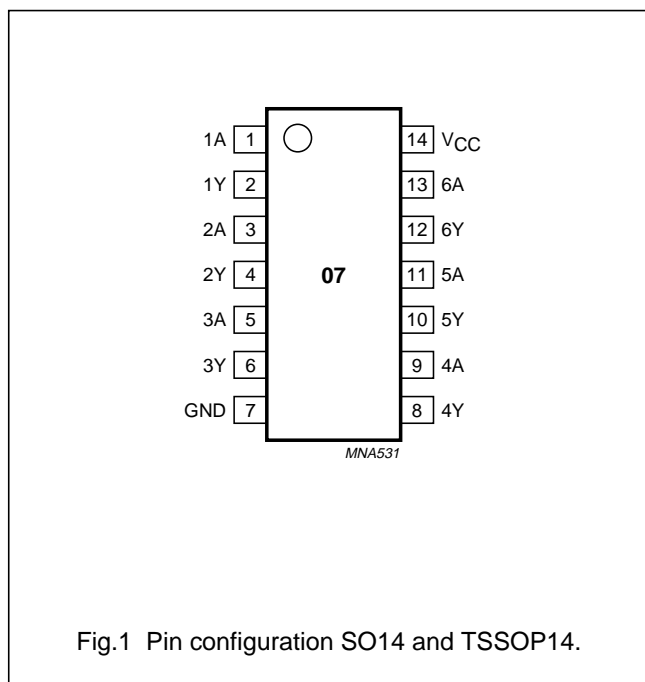
# 74LVC07A

## ORDERING INFORMATION

TYPE NUMBER	PACKAGE				
	TEMPERATURE RANGE	PINS	PACKAGE	MATERIAL	CODE
74LVC07AD	-40 to +125 °C	14	SO14	plastic	SOT108-1
74LVC07APW	-40 to +125 °C	14	TSSOP14	plastic	SOT402-1
74LVC07ABQ	-40 to +125 °C	14	DHVQFN14	plastic	SOT762-1

## PINNING

PIN	SYMBOL	DESCRIPTION
1	1A	data input
2	1Y	data output
3	2A	data input
4	2Y	data output
5	3A	data input
6	3Y	data output
7	GND	ground (0 V)
8	4Y	data output
9	4A	data input
10	5Y	data output
11	5A	data input
12	6Y	data output
13	6A	data input
14	V <sub>CC</sub>	supply voltage



# Hex buffer with open-drain outputs

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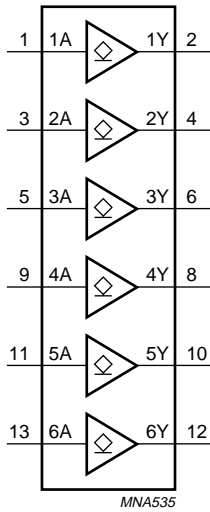


Fig.3 Logic symbol.

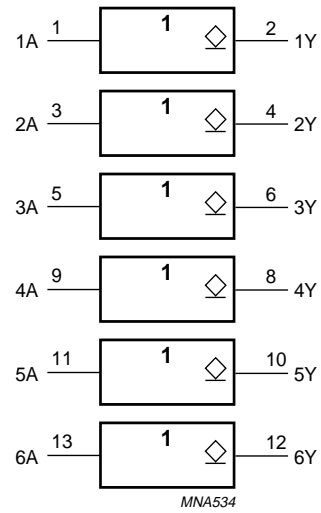


Fig.4 IEC logic symbol.

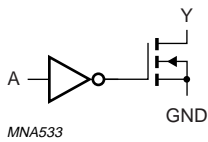


Fig.5 Logic diagram (one gate).

## Hex buffer with open-drain outputs

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## RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$V_{CC}$	supply voltage		1.65	5.5	V
$V_I$	input voltage		0	5.5	V
$V_O$	output voltage	active mode	0	5.5	V
		high-impedance mode	0	5.5	V
$T_{amb}$	operating ambient temperature		-40	+125	°C
$t_r, t_f$	input rise and fall ratios	$V_{CC} = 1.65$ to $2.7$ V	0	20	ns/V
		$V_{CC} = 2.7$ to $5.5$ V	0	10	ns/V

## LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134); voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$V_{CC}$	supply voltage		-0.5	+6.5	V
$I_{IK}$	input diode current	$V_I < 0$	-	-50	mA
$V_I$	input voltage	note 1	-0.5	+6.5	V
$I_{OK}$	output clamping diode current	$V_O < 0$	-	-50	mA
$V_O$	output voltage	active mode; note 1	-0.5	+6.5	V
		high-impedance mode; note 1	-0.5	+6.5	V
$I_O$	output source or sink current	$V_O = 0$ to $V_{CC}$	-	50	mA
$I_{CC}, I_{GND}$	$V_{CC}$ or GND current		-	±100	mA
$T_{stg}$	storage temperature		-65	+150	°C
$P_{tot}$	power dissipation	$T_{amb} = -40$ to $+125$ °C; note 2	-	500	mW

## Notes

1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. For SO14 packages: above 70 °C derate linearly with 8 mW/K.  
 For TSSOP14 packages: above 60 °C derate linearly with 5.5 mW/K.  
 For DHVQFN14 packages: above 60 °C derate linearly with 4.5 mW/K.

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**DC CHARACTERISTICS**

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
		OTHER	V <sub>CC</sub> (V)				
<b>T<sub>amb</sub> = -40 to +85 °C; note 1</b>							
V <sub>IH</sub>	HIGH-level input voltage		1.65 to 1.95	V <sub>CC</sub>	–	–	V
			2.3 to 2.7	1.7	–	–	V
			2.7 to 3.6	2.0	–	–	V
			4.5 to 5.5	0.7 × V <sub>CC</sub>	–	–	V
V <sub>IL</sub>	LOW-level input voltage		1.65 to 1.95	–	–	GND	V
			2.3 to 2.7	–	–	0.7	V
			2.7 to 3.6	–	–	0.8	V
			4.5 to 5.5	–	–	0.30 × V <sub>CC</sub>	V
V <sub>OL</sub>	LOW-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> I <sub>O</sub> = 100 μA I <sub>O</sub> = 4 mA I <sub>O</sub> = 8 mA I <sub>O</sub> = 12 mA I <sub>O</sub> = 24 mA I <sub>O</sub> = 32 mA	1.65 to 5.5	–	–	0.20	V
			1.65	–	–	0.45	V
			2.3	–	–	0.3	V
			2.7	–	–	0.4	V
			3.0	–	–	0.55	V
			4.5	–	–	0.55	V
I <sub>LI</sub>	input leakage current	V <sub>I</sub> = 5.5 V or GND	1.65 to 5.5	–	±0.1	±5	μA
I <sub>OZ</sub>	output leakage current	V <sub>I</sub> = V <sub>IH</sub> ; V <sub>O</sub> = 5.5 V or GND	1.65 to 5.5	–	0.1	±10	μA
I <sub>off</sub>	power-off leakage current	V <sub>I</sub> or V <sub>O</sub> = 5.5 V	0.0	–	±0.1	±10	μA
I <sub>CC</sub>	quiescent supply current	V <sub>I</sub> = V <sub>CC</sub> or GND; I <sub>O</sub> = 0	5.5	–	0.1	10	μA
ΔI <sub>CC</sub>	additional quiescent supply current per input pin	V <sub>I</sub> = V <sub>CC</sub> – 0.6 V; I <sub>O</sub> = 0	2.3 to 5.5	–	5	500	μA

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SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
		OTHER	V <sub>CC</sub> (V)				
<b>T<sub>amb</sub> = -40 to +125 °C</b>							
V <sub>IH</sub>	HIGH-level input voltage		1.65 to 1.95	V <sub>CC</sub>	–	–	V
			2.3 to 2.7	1.7	–	–	V
			2.7 to 3.6	2.0	–	–	V
			4.5 to 5.5	0.7 × V <sub>CC</sub>	–	–	V
V <sub>IL</sub>	LOW-level input voltage		1.65 to 1.95	–	–	GND	V
			2.3 to 2.7	–	–	0.7	V
			2.7 to 3.6	–	–	0.8	V
			4.5 to 5.5	–	–	0.30 × V <sub>CC</sub>	V
V <sub>OL</sub>	LOW-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> I <sub>O</sub> = 100 μA	1.65 to 5.5	–	–	0.20	V
		I <sub>O</sub> = 4 mA	1.65	–	–	0.45	V
		I <sub>O</sub> = 8 mA	2.3	–	–	0.3	V
		I <sub>O</sub> = 12 mA	2.7	–	–	0.4	V
		I <sub>O</sub> = 24 mA	3.0	–	–	0.55	V
		I <sub>O</sub> = 32 mA	4.5	–	–	0.55	V
I <sub>LI</sub>	input leakage current	V <sub>I</sub> = 5.5 V or GND	1.65 to 5.5	–	–	±5	μA
I <sub>OZ</sub>	output leakage current	V <sub>I</sub> = V <sub>IH</sub> ; V <sub>O</sub> = 5.5 V or GND	1.65 to 5.5	–	–	±10	μA
I <sub>off</sub>	power-off leakage current	V <sub>I</sub> or V <sub>O</sub> = 5.5 V	0.0	–	–	±10	μA
I <sub>CC</sub>	quiescent supply current	V <sub>I</sub> = V <sub>CC</sub> or GND; I <sub>O</sub> = 0	5.5	–	–	10	μA
ΔI <sub>CC</sub>	additional quiescent supply current per input pin	V <sub>I</sub> = V <sub>CC</sub> – 0.6 V; I <sub>O</sub> = 0	2.3 to 5.5	–	–	500	μA

**Note**

1. All typical values are measured at V<sub>CC</sub> = 3.3 V and T<sub>amb</sub> = 25 °C.

## Hex buffer with open-drain outputs

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**AC CHARACTERISTICS**

GND = 0 V;  $t_r = t_f \leq 2$  ns for  $V_{CC} \leq 2.7$  V and  $t_r = t_f \leq 2.5$  ns for  $V_{CC} \geq 2.7$  V.

SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
		WAVEFORMS	$V_{CC}$ (V)				
<b><math>T_{amb} = -40</math> to <math>+85</math> °C; note 1</b>							
$t_{PLZ}/t_{PZL}$	propagation delay nA to nY	see Figs 6 and 7	1.65 to 1.95	–	2.5	–	ns
			2.3 to 2.7	0.5	1.6	2.8	ns
			2.7	0.5	2.4	3.3	ns
			3.0 to 3.6	0.5	2.2	3.6	ns
			4.5 to 5.5	0.5	1.6	2.6	ns
<b><math>T_{amb} = -40</math> to <math>+125</math> °C</b>							
$t_{PLZ}/t_{PZL}$	propagation delay nA to nY	see Figs 6 and 7	1.65 to 1.95	–	–	–	ns
			2.3 to 2.7	0.5	–	3.5	ns
			2.7	0.5	–	4.5	ns
			3.0 to 3.6	0.5	–	4.5	ns
			4.5 to 5.5	0.5	–	3.5	ns

**Note**

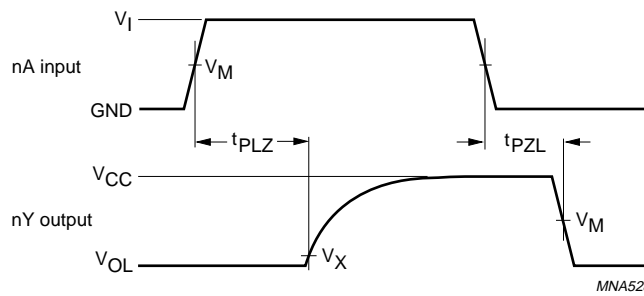
1. All typical values are measured at  $T_{amb} = 25$  °C and at  $V_{CC} = 1.8, 2.5, 2.7, 3.3$  and  $5.0$  V, respectively.



Hex buffer with open-drain outputs

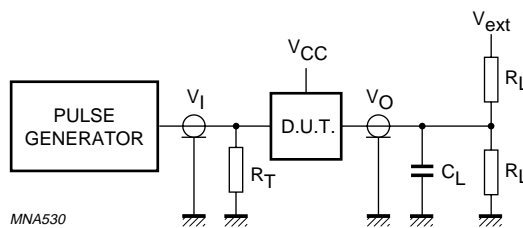
74LVC07A

AC WAVEFORMS



V <sub>CC</sub>	V <sub>M</sub>	V <sub>X</sub>
<2.7 V	0.5 × V <sub>CC</sub>	V <sub>OL</sub> + 0.15 V
≥2.7 to 3.6 V	1.5 V	V <sub>OL</sub> + 0.3 V
≥4.5 to 5.5 V	0.5 × V <sub>CC</sub>	V <sub>OL</sub> + 0.3 V

Fig.6 The input nA to output nY propagation delays.



V <sub>CC</sub>	V <sub>ext</sub>	V <sub>I</sub>	C <sub>L</sub>	R <sub>L</sub>
1.65 to 1.95 V	2 × V <sub>CC</sub>	V <sub>CC</sub>	30 pF	1 kΩ
2.3 to 2.7 V	2 × V <sub>CC</sub>	V <sub>CC</sub>	30 pF	500 Ω
2.7 V	6 V	2.7 V	50 pF	500 Ω
3.0 to 3.6 V	6 V	2.7 V	50 pF	500 Ω
4.5 to 5.5 V	2 × V <sub>CC</sub>	V <sub>CC</sub>	50 pF	500 Ω

Definitions for test circuits:

R<sub>L</sub> = Load resistor.

C<sub>L</sub> = Load capacitance including jig and probe capacitance.

R<sub>T</sub> = Termination resistance should be equal to the output impedance Z<sub>o</sub> of the pulse generator.

Fig.7 Load circuitry for switching times.

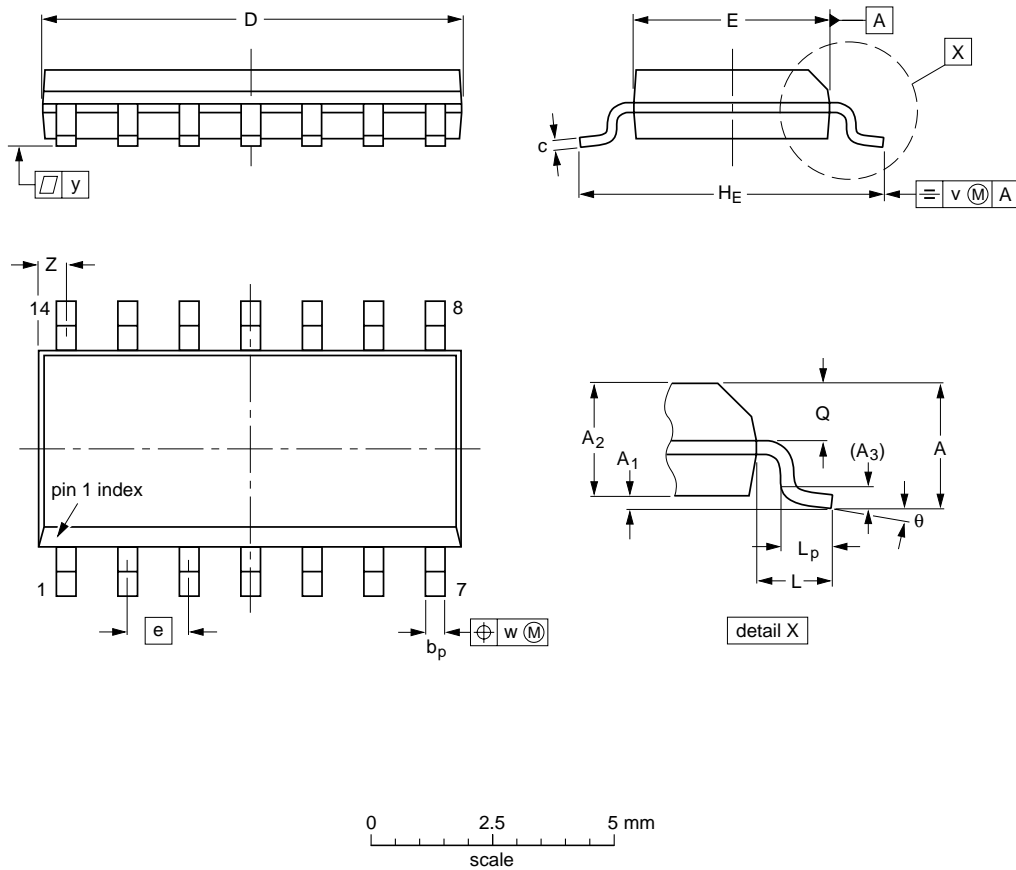
# Hex buffer with open-drain outputs

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## PACKAGE OUTLINES

SO14: plastic small outline package; 14 leads; body width 3.9 mm

SOT108-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(1)</sup>	e	H <sub>E</sub>	L	L <sub>p</sub>	Q	v	w	y	z <sup>(1)</sup>	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	8.75 8.55	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.35 0.34	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

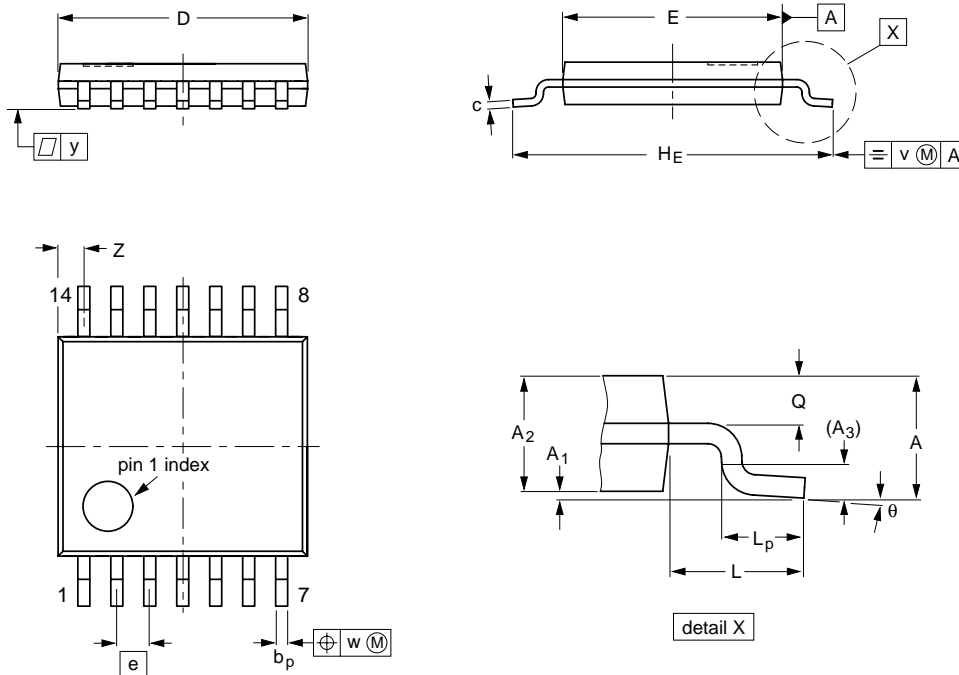
OUTLINE VERSION	REFERENCES			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
SOT108-1	076E06	MS-012			99-12-27 03-02-19

Hex buffer with open-drain outputs

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TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm

SOT402-1



**DIMENSIONS (mm are the original dimensions)**

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(2)</sup>	e	H <sub>E</sub>	L	L <sub>p</sub>	Q	v	w	y	Z <sup>(1)</sup>	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.72 0.38	8° 0°

**Notes**

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

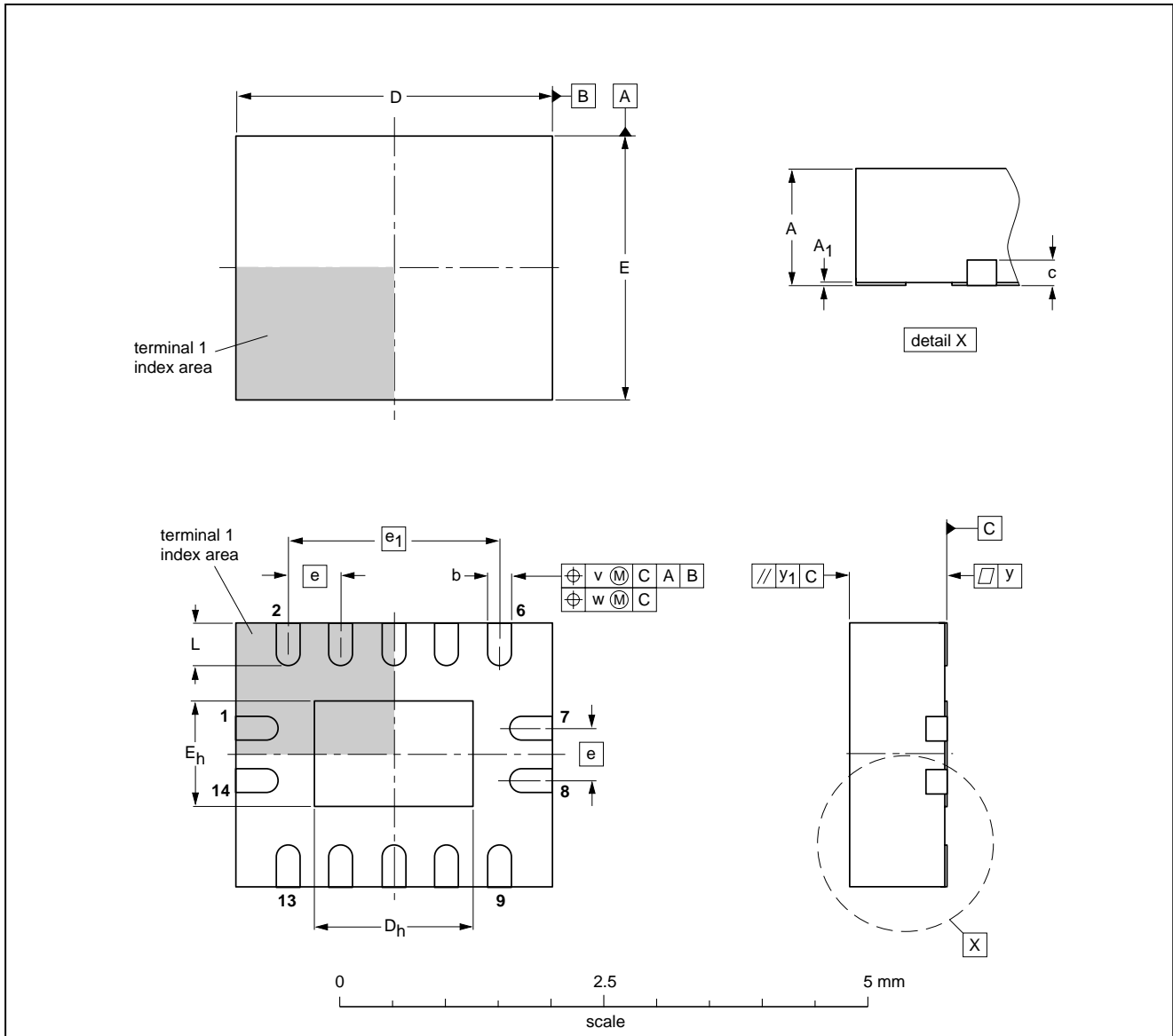
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT402-1		MO-153				99-12-27 03-02-18

Hex buffer with open-drain outputs

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DHVQFN14: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 14 terminals; body 2.5 x 3 x 0.85 mm

SOT762-1



**DIMENSIONS (mm are the original dimensions)**

UNIT	A <sup>(1)</sup> max.	A <sub>1</sub>	b	c	D <sup>(1)</sup>	D <sub>h</sub>	E <sup>(1)</sup>	E <sub>h</sub>	e	e <sub>1</sub>	L	v	w	y	y <sub>1</sub>
mm	1	0.05 0.00	0.30 0.18	0.2	3.1 2.9	1.65 1.35	2.6 2.4	1.15 0.85	0.5	2	0.5 0.3	0.1	0.05	0.05	0.1

**Note**

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
SOT762-1	---	MO-241	---		02-10-17 03-01-27

## Hex buffer with open-drain outputs

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## DATA SHEET STATUS

LEVEL	DATA SHEET STATUS <sup>(1)</sup>	PRODUCT STATUS <sup>(2)(3)</sup>	DEFINITION
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
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3. For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

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**Limiting values definition** — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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