Synchronous 4-Bit Counters

General Description

These synchronous, presettable counters feature an internal carry look-ahead for application in high-speed counting designs. The 160A, 162A, LS160, LS162, are decade counters and the 161A, 163A, LS161, LS163 are 4-bit binary counters. The carry output is decoded by means of a NOR gate, thus preventing spikes during the normal counting mode of operation. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when so instructed by the count-enable inputs and internal gating. This mode of operation eliminates the output counting spikes which are normally associated with asynchronous (ripple clock) counters. A buffered clock input triggers the four flip-flops on the rising (positive-going) edge of the clock input waveform.

These counters are fully programmable; that is, the outputs may be preset to either level. As presetting is synchronous, setting up a low level at the load input disables the counter and causes the outputs to agree with the setup data after the next clock pulse regardless of the levels of the enable input. Low-to-high transitions at the load input of the 160A through 163A or LS160 through LS163 are perfectly acceptable, regardless of the logic levels on the clock or enable inputs. The clear function for the 160A, 161A, LS160, and LS161 is asynchronous; and a low level at the clear input sets all four of the flip-flop outputs low regardless of the levels of clock, load, or enable inputs. The clear function for the 162A, 163A, LS162, LS163, is synchronous; and a low level at the clear input sets all four of the flip-flop outputs low after the next clock pulse, regardless of the levels of the enable inputs. This synchronous clear allows the count length to be modified easily, as decoding the maximum count desired can be accomplished with one external NAND gate. The gate output is connected to the clear input to synchronously clear the counter to all low outputs. Low-to-high transitions at the clear input of the 162A and 163A are also permissible regardless of the logic levels on the clock, enable, or load inputs.

The carry look-ahead circuitry provides for cascading counters for n-bit synchronous applications without additional gating. Instrumental in accomplishing this function are two count-enable inputs and a ripple carry output. Both count-enable inputs (P and T) must be high to count, and input T is fed forward to enable the ripple carry output. The ripple carry output thus enabled will produce a high-level output pulse with a duration approximately equal to the high-level portion of the Q_A output. This high-level overflow ripple carry pulse can be used to enable successive cascaded stages. High-to-low-level transitions at the enable P or T inputs of the 160A through 163A or LS160 through LS163, may occur regardless of the logic level on the clock.

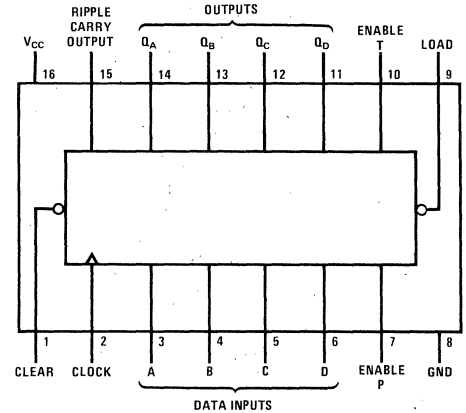
LS160 through LS163 feature a fully independent clock circuit. Changes made to control inputs (enable P or T, load or clear) that will modify the operating mode have no effect until clocking occurs. The function of the counter (whether enabled, disabled, loading, or counting) will be dictated solely by the conditions meeting the stable setup and hold times.

Features

- Synchronously programmable
- Internal look-ahead for fast counting
- Carry output for n-bit cascading
- Synchronous counting
- Load control line
- Diode-clamped inputs

TYPE	TYPICAL PROPAGATION TIME, CLOCK TO Q OUTPUT	TYPICAL CLOCK FREQUENCY	TYPICAL POWER DISSIPATION
160 thru 163	14 ns	35 MHz	315 mW
LS160 thru LS163	14 ns	32 MHz	93 mW

Connection Diagram



54160A(J), (W); 74160A(J), (N), (W);
54LS160/74LS160(J), (N), (W);
54161A(J), (W); 74161A(J), (N), (W);
54LS161/74LS161(J), (N), (W);
54162A(J), (W); 74162A(J), (N), (W);
54LS162/74LS162(J), (N), (W);
54163A(J), (W); 74163A(J), (N), (W);
54LS163/74LS163(J), (N), (W)

Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			CONDITIONS			DM54/74 160A, 161A 162A, 163A MIN	DM54/74 160A, 161A 162A, 163A TYP(1)	DM54/74 160A, 161A 162A, 163A MAX	DM54LS/74LS LS160, LS161 LS162, LS163 MIN	DM54LS/74LS LS160, LS161 LS162, LS163 TYP(1)	DM54LS/74LS LS160, LS161 LS162, LS163 MAX	UNITS
V_{IH}	High Level Input Voltage					2			2			V
V_{IL}	Low Level Input Voltage				DM54			0.8			0.7	V
					DM74			0.8			0.8	
V_I	Input Clamp Voltage		V_{CC} = Min	I_I = −12 mA				−1.5				V
				I_I = −18 mA							−1.5	
I_{OH}	High Level Output Current							−800			−400	μA
V_{OH}	High Level Output Voltage		V_{CC} = Min, V_{IH} = 2V, V_{IL} = Max, I_{OH} = Max		DM54	2.4	3.4		2.5	3.4		V
					DM74	2.4	3.4		2.7	3.4		
I_{OL}	Low Level Output Current				DM54			16			4	mA
					DM74			16			8	
V_{OL}	Low Level Output Voltage		V_{CC} = Min, V_{IH} = 2V, V_{IL} = Max	I_{OL} = Max	DM54		0.2	0.4		0.25	0.4	V
					DM74		0.2	0.4		0.35	0.5	
				I_{OL} = 4 mA	DM74					0.25	0.4	
I_I	Input Current ax Maximum Input Voltage	All	V_{CC} = Max	V_I = 5.5V				1				mA
		Data or Enable P		V_I = 7V							0.1	
		Load, Clock, or Enable T									0.2	
		Clear (LS160, LS161)									0.1	
		Clear (LS162, LS163)									0.2	
I_{IH}	High Level Input Current	Load	V_{CC} = Max, V_I = 2.4V (160A–163A), V_I = 2.7V (LS160–LS163)					40			40	μA
		Clock, Enable T						80			40	
		Data						40			20	
		Enable P						40			20	
		Clear (160, 161)						40			20	
		Clear (162, 163)						40			40	
I_{IL}	Low Level Input Current	Data, Enable P	V_{CC} = Max, V_I = 0.4V					−1.6			−0.4	mA
		Clock						−3.2			−1.2	
		Load						−1.6			−0.8	
		Enable T						−3.2			−0.8	
		Clear (160, 161)						−1.6			−0.4	
		Clear (162, 163)						−1.6			−0.8	
I_{OS}	Short Circuit Output Current		V_{CC} = Max(2)		DM54	−20		−57	−30		−130	mA
					DM74	−18		−57	−30		−130	
I_{CCH}	Supply Current, All Outputs High		V_{CC} = Max(3)		DM54		59	85		18	31	mA
					DM74		59	94		18	31	
I_{CCL}	Supply Current, All Outputs Low		V_{CC} = Max(4)		DM54		63	91		19	32	mA
					DM74		63	101		19	32	

Notes

(1) All typical values are at V_{CC} = 5V, T_A = 25°C.

(2) Not more than one output should be shorted at a time, and for DM54LS/74LS duration of short circuit should not exceed one second.

(3) I_{CCH} is measured with the load input high, then again with the load input low, with all other inputs high and all outputs open.

(4) I_{CCL} is measured with the clock input high, then again with the clock input low, with all other inputs low and all outputs open.

Switching Characteristics V_{CC} = 5V, T_A = 25°C

PARAMETER			FROM (INPUT)	TO (OUTPUT)	DM54/74 160A, 161A, 162A, 163A				DM54LS/74LS LS160, LS161, LS162, LS163				UNITS
					CONDITIONS	MIN	TYP	MAX	CONDITIONS	MIN	TYP	MAX	
f_{MAX}	Maximum Clock Frequency				C_L = 15 pF, R_L = 400Ω	25	35		C_L = 15 pF, R_L = 2 kΩ	25	32		MHz
t_{PLH}	Propagation Delay Time, Low-to-High Level Output		Clock	Ripple carry			18	27			23	35	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output						16	24			23	35	ns
t_{PLH}	Propagation Delay Time, Low-to-High Level Output		Clock (Load Input High)	Any Q			14	20			16	24	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output						16	23			18	27	ns
t_{PLH}	Propagation Delay Time, Low-to-High Level Output		Clock (Load Input Low)	Any Q			14	21			17	25	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output						18	25			19	29	ns
t_{PLH}	Propagation Delay Time, Low-to-High Level Output		Enable T	Ripple carry			10	15			15	23	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output						12	16			15	23	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output		Clear (5)	Any Q			24	36			26	38	ns
$t_{W(CLOCK)}$	Width of Clock Pulse					25				25			ns
$t_{W(CLEAR)}$	Width of Clear Pulse					20				20			ns
t_{SETUP}	Setup Time	Data Inputs A, B, C, D				20				20			ns
		Enable P				20				25			
		Load				25				25			
		Clear (6)				20				25			
t_{HOLD}	Hold Time at Any Input					0				0			ns

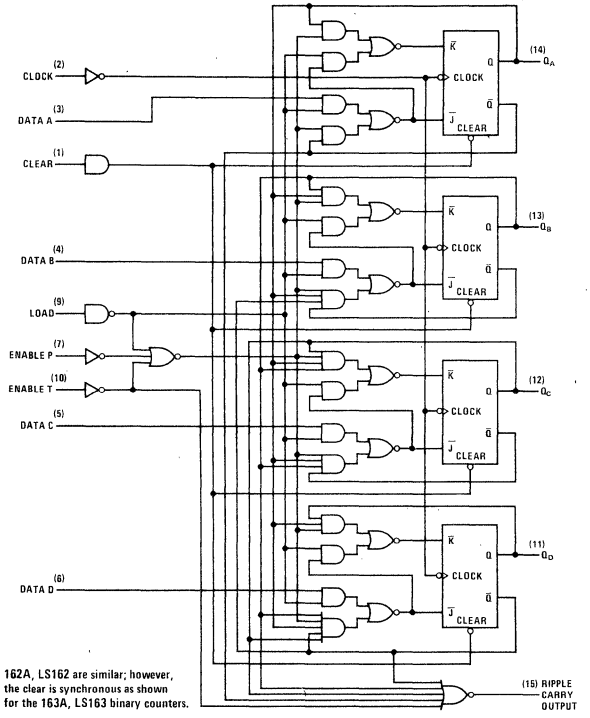
Notes

(5) Propagation delay for clearing is measured from the clear input for the 160A, LS160, 161A and LS161 or from the clock input transition for the 162A, LS162, 163A and LS163.

(6) This applies only for 162, 163, LS162 and LS163, which have synchronous clear inputs.

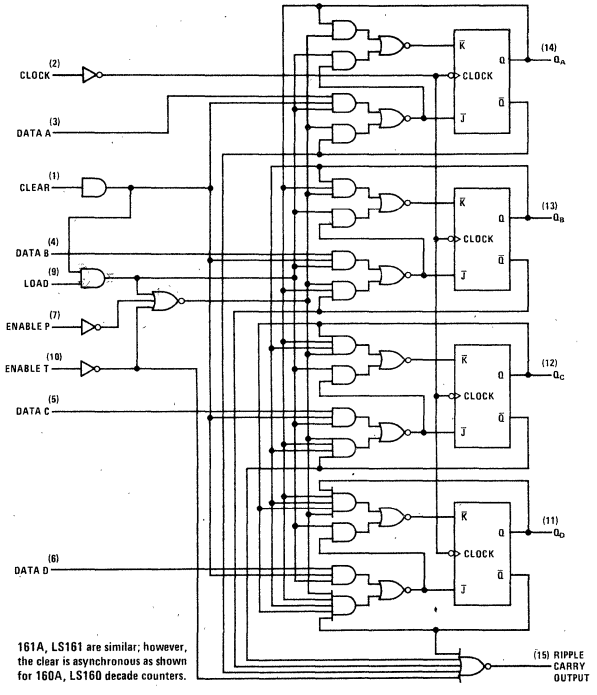
Logic Diagrams

160A, LS160



162A, LS162 are similar; however, the clear is synchronous as shown for the 163A, LS163 binary counters.

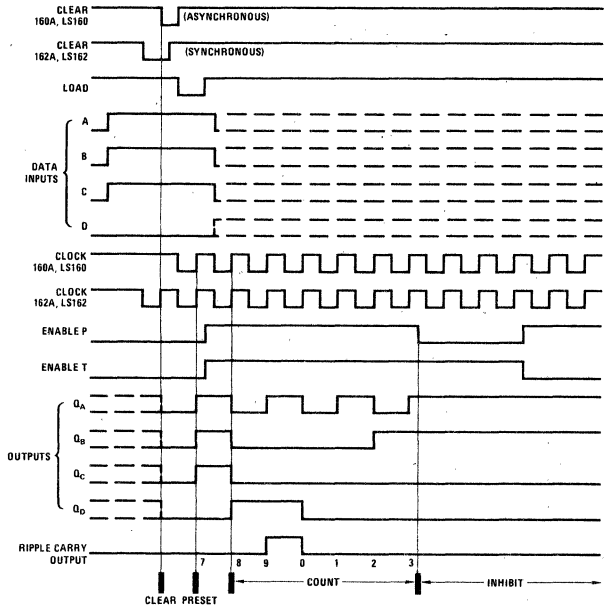
163A, LS163



161A, LS161 are similar; however, the clear is asynchronous as shown for 160A, LS160 decade counters.

Timing Diagrams

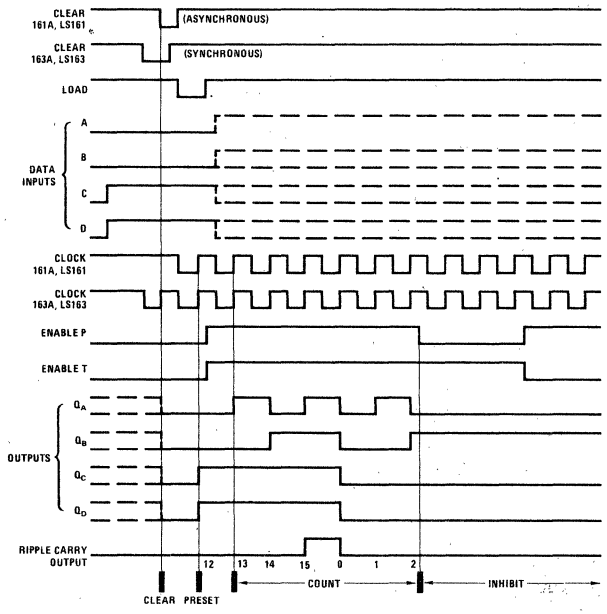
160, 162, LS160, LS162 SYNCHRONOUS DECADE COUNTERS
TYPICAL CLEAR, PRESET, COUNT AND INHIBIT SEQUENCES



Sequence:

(1) Clear outputs to zero
(2) Preset to BCD seven
(3) Count to eight, nine, zero, one, two, and three
(4) Inhibit

161, LS161, 163, LS163 SYNCHRONOUS BINARY COUNTERS
TYPICAL CLEAR, PRESET, COUNT AND INHIBIT SEQUENCES

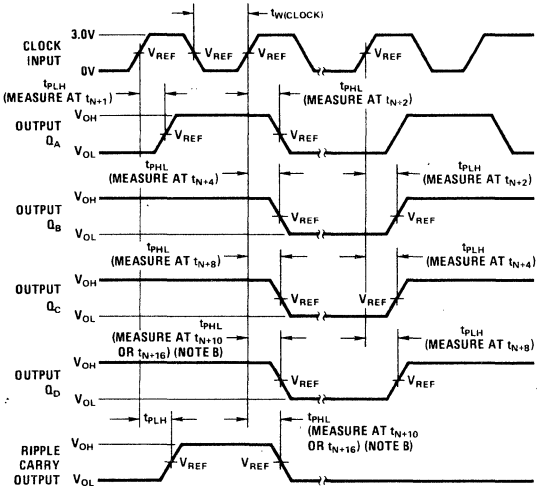


Sequence:

(1) Clear outputs to zero
(2) Preset to binary twelve
(3) Count to thirteen, fourteen, fifteen, zero, one, and two
(4) Inhibit

Parameter Measurement Information

SWITCHING TIME WAVEFORMS



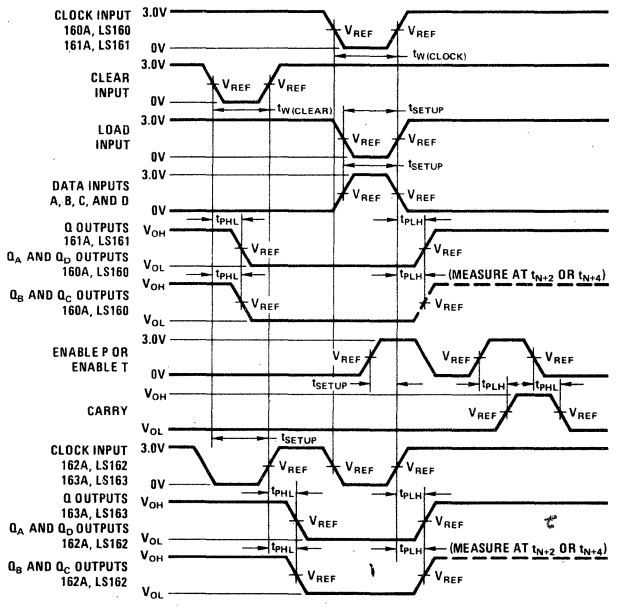
Notes:

(A) The input pulses are supplied by a generator having the following characteristics: PRR $\leq$ 1 MHz, duty cycle $\leq$ 50%, $Z_{OUT} \approx 50\Omega$, for 160A through 163A, $t_r \leq 10$ ns, $t_f \leq 10$ ns; for LS160 through LS163, $t_r \leq 15$ ns, $t_f \leq 6$ ns. Vary PRR to measure f_{MAX}.

(B) Outputs Q_D and carry are tested at t_{n+10} for 160A, 162A, LS160, LS162, and at t_{n+16} for 161A, 163A, LS161, LS163, where t_n is the bit time when all outputs are low.

(C) For 160A through 163A, V_{REF} = 1.5V; for LS160 through LS163, V_{REF} = 1.3V.

SWITCHING TIME WAVEFORMS



Notes:

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(B) Enable P and enable T setup times are measured at t_{n+0}.

(C) For 160A through 163A, V_{REF} = 1.5V; for LS160 through LS163, V_{REF} = 1.3V.