74HC4049

Hex inverting HIGH-to-LOW level shifter

Rev. 7 — 5 February 2016

Product data sheet

1. General description

The 74HC4049 is a hex inverter with over-voltage tolerant inputs. Inputs are overvoltage tolerant to 15 V. This enables the device to be used in HIGH-to-LOW level shifting applications.

2. Features and benefits

- Low-power dissipation
- Complies with JEDEC standard no. 7A
- ESD protection:
 - ♦ HBM JESD22-A114F exceeds 2 000 V
 - ◆ MM JESD22-A115-A exceeds 200 V
- Multiple package options
- Specified from -40 °C to +85 °C and from -40 °C to +125 °C

3. Ordering information

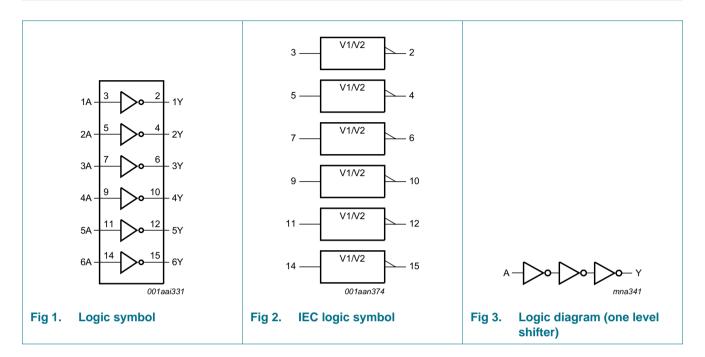
Table 1. Ordering information

Type number	Package										
	Temperature range	Name	Description	Version							
74HC4049D	–40 °C to +125 °C	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1							
74HC4049DB	−40 °C to +125 °C	SSOP16	plastic shrink small outline package; 16 leads; body width 5.3 mm	SOT338-1							
74HC4049PW	-40 °C to +125 °C	TSSOP16	plastic thin shrink small outline package; 16 leads; body width 4.4 mm	SOT403-1							



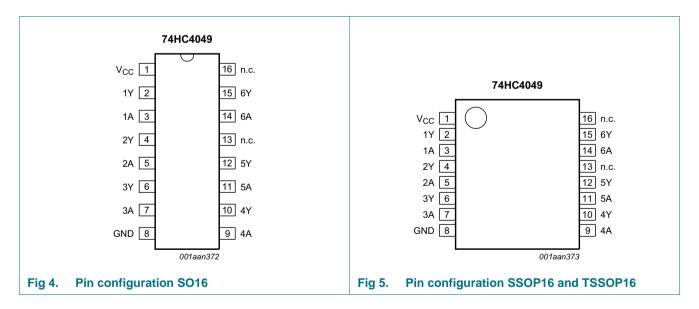
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4. Functional diagram



5. Pinning information

5.1 Pinning



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5.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
V _{CC}	1	supply voltage
1Y to 6Y	2, 4, 6, 10, 12, 15	output
1A to 6A	3, 5, 7, 9, 11, 14	input
GND	8	ground (0 V)
n.c.	13, 16	not connected

6. Functional description

Table 3. Function table [1]

Input	Output
nA	nY
L	Н
Н	L

^[1] H = HIGH voltage level; L = LOW voltage level; X = don't care; Z = high-impedance OFF-state.

7. Limiting values

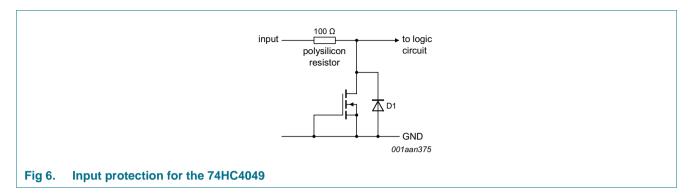
Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Max	Unit
V _{CC}	supply voltage			-0.5	+7	V
V _{IK}	input clamping voltage			-0.5	+16	V
I _{IK}	input clamping current	V _I < -0.5 V		-20	-	mA
I _{OK}	output clamping current	$V_{O} < -0.5 \text{ V or } V_{O} > V_{CC} + 0.5 \text{ V}$		-	±20	mA
Io	output current	$V_{O} = -0.5 \text{ V to } (V_{CC} + 0.5 \text{ V})$		-	±25	mA
I _{CC}	supply current			-	+50	mA
I _{GND}	ground current			-	-50	mA
T _{stg}	storage temperature			-65	+150	°C
P _{tot}	total power dissipation	SO16, SSOP16 and TSSOP16 packages	[1]	-	500	mW

^[1] For SO16 package: P_{tot} derates linearly with 8 mW/K above 70 °C.
For SSOP16 and TSSOP16 packages: P_{tot} derates linearly with 5.5 mW/K above 60 °C.

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8. Recommended operating conditions

Table 5. Recommended operating conditions

Voltages are referenced to GND (ground = 0 V)

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
V_{CC}	supply voltage		2.0	5.0	6.0	V
VI	input voltage		0	-	15	V
Vo	output voltage		0	-	V _{CC}	V
T _{amb}	ambient temperature		-40	+25	+125	°C
Δt/ΔV	input transition rise and fall rate	$V_{CC} = 2.0 \text{ V}; V_I = 2.0 \text{ V}$	-	-	625	ns/V
		$V_{CC} = 4.5 \text{ V}; V_I = 4.5 \text{ V}$	-	1.67	139	ns/V
		$V_{CC} = 6.0 \text{ V}; V_I = 6.0 \text{ V}$	-	-	83	ns/V
		$V_{CC} = 6.0 \text{ V}; V_I = 10.0 \text{ V}$	-	-	81	ns/V
		$V_{CC} = 6.0 \text{ V}; V_I = 15.0 \text{ V}$	-	-	83	ns/V

9. Static characteristics

Table 6. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Tar	_{nb} = 25	°C	T _{amb} =		T _{amb} = - +12	Unit	
			Min	Тур	Max	Min	Max	Min	Max	
V _{IH}	HIGH-level	V _{CC} = 2.0 V	1.5	1.3	-	1.5	-	1.5	-	V
	input voltage	V _{CC} = 4.5 V	3.15	2.4	-	3.15	-	3.15	-	V
		V _{CC} = 6.0 V	4.2	3.1	-	4.2	-	4.2	-	V
V _{IL} LOW-level		V _{CC} = 2.0 V	-	0.7	0.5	-	0.5	-	0.5	V
	input voltage	V _{CC} = 4.5 V	-	1.8	1.35	-	1.35	-	1.35	V
		V _{CC} = 6.0 V	-	2.3	1.8	-	1.8	-	1.8	V
V _{OH}	HIGH-level	$V_I = V_{IH}$ or V_{IL}								
	output voltage	$I_{O} = -20 \mu A; V_{CC} = 2.0 V$	1.9	2.0	-	1.9	-	1.9	-	V
		$I_O = -20 \mu A; V_{CC} = 4.5 V$	4.4	4.5	-	4.4	-	4.4	-	V
		$I_{O} = -20 \mu A; V_{CC} = 6.0 V$	5.9	6.0	-	5.9	-	5.9	-	V
		$I_{O} = -4.0 \text{ mA}; V_{CC} = 4.5 \text{ V}$	3.98	-	-	3.84	-	3.7	-	V
		$I_{O} = -5.2 \text{ mA}; V_{CC} = 6.0 \text{ V}$	5.48	-	-	5.34	-	5.2	-	V

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Table 6. Static characteristics ... continued

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

V _{OL} L	Parameter	Conditions	Tai	_{mb} = 25	°C		40 °C to 5 °C		-40 °C to 5 °C	Unit
			Min	Тур	Max	Min	Max	Min	Max	
V _{OL}	LOW-level	$V_I = V_{IH}$ or V_{IL}								
	output voltage	$I_O = 20 \mu A; V_{CC} = 2.0 \text{ V}$	-	-	0.1	-	0.1	-	0.1	V
		$I_O = 20 \mu A; V_{CC} = 4.5 V$	-	-	0.1	-	0.1	-	0.1	V
		$I_O = 20 \mu A; V_{CC} = 6.0 V$	-	-	0.1	-	0.1	-	0.1	V
		$I_O = 4.0 \text{ mA}; V_{CC} = 4.5 \text{ V}$	-	-	0.26	-	0.33	-	0.4	V
		$I_O = 5.2 \text{ mA}; V_{CC} = 6.0 \text{ V}$	-	-	0.26	-	0.33	-	0.4	V
II	input leakage current	$V_I = V_{CC}$ or GND; $V_{CC} = 6.0 \text{ V}$	-	-	±0.1	-	±1.0	-	±1.0	μΑ
		V _I = 15 V; V _{CC} = 2.0 V to 6.0 V	-	-	±0.5	-	±5.0	-	±5.0	μА
I _{CC}	supply current	$V_I = 15 \text{ V or GND}; I_O = 0 \text{ A}; V_{CC} = 6.0 \text{ V}$	-	-	2.0	-	20	-	40	μА
Cı	input capacitance		-	3.5	-	-	-	-	-	pF

10. Dynamic characteristics

Table 7. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V); $C_L = 50 \text{ pF}$ unless otherwise specified; for test circuit see Figure 8.

Symbol	Parameter	Conditions	T _{an}	_{nb} = 25	°C		= –40 °C 85 °C	T _{amb} =	Unit	
			Min	Тур	Max	Min	Max	Min	Max	
t _{pd}	propagation	nA to nY; see Figure 7 [1]								
delay		V _{CC} = 2.0 V	-	28	85	-	105	-	130	ns
		V _{CC} = 4.5 V	-	10	17	-	21	-	26	ns
		V _{CC} = 5 V; C _L = 15 pF	-	8	-	-	-	-	-	ns
		V _{CC} = 6.0 V	-	8	14	-	18	-	22	ns
t _t	transition	Yn; see Figure 7 [2]								
	time	V _{CC} = 2.0 V	-	19	75	-	95	-	110	ns
		V _{CC} = 4.5 V	-	7	15	-	19	-	22	ns
		V _{CC} = 6.0 V	-	6	13	-	16	-	19	ns

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 Table 7.
 Dynamic characteristics ...continued

Voltages are referenced to GND (ground = 0 V); C_L = 50 pF unless otherwise specified; for test circuit see Figure 8.

Symbol	Parameter	Conditions	T _{an}	_{nb} = 25	°C		- –40 °C 85 °C	T _{amb} = to +1	Unit	
			Min	Тур	Max	Min	Max	Min	Max	
C _{PD}	power dissipation capacitance	C_L = 50 pF; f = 1 MHz; V_I = GND to V_{CC}	-	14	-	-	-	-	-	pF

- [1] t_{pd} is the same as t_{PLH} and t_{PHL} .
- [2] t_t is the same as t_{THL} and t_{TLH} .
- [3] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

 $P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \sum (C_L \times V_{CC}^2 \times f_o)$ where:

 f_i = input frequency in MHz;

f_o = output frequency in MHz;

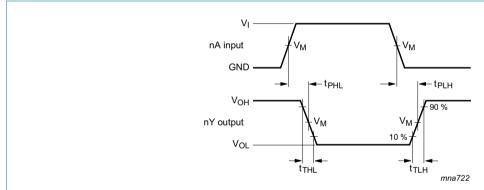
C_L = output load capacitance in pF;

V_{CC} = supply voltage in V;

N = number of inputs switching;

 $\sum (C_L \times V_{CC}^2 \times f_o) = \text{sum of outputs.}$

11. Waveforms



Measurement points are given in Table 8.

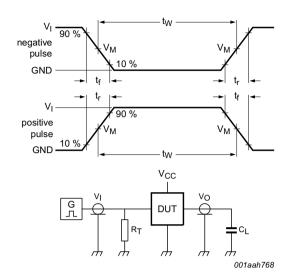
 V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig 7. The input (nA) to output (nY) propagation delays

Table 8. Measurement points

Туре	Input	Output
	V _M	V _M
74HC4049	0.5V _{CC}	0.5V _{CC}

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Test data is given in Table 9.

Definitions test circuit:

 R_T = Termination resistance should be equal to output impedance Z_0 of the pulse generator.

 C_L = Load capacitance including jig and probe capacitance.

R_L = Load resistance.

S1 = Test selection switch.

Fig 8. Test circuit for measuring switching times

Table 9. Test data

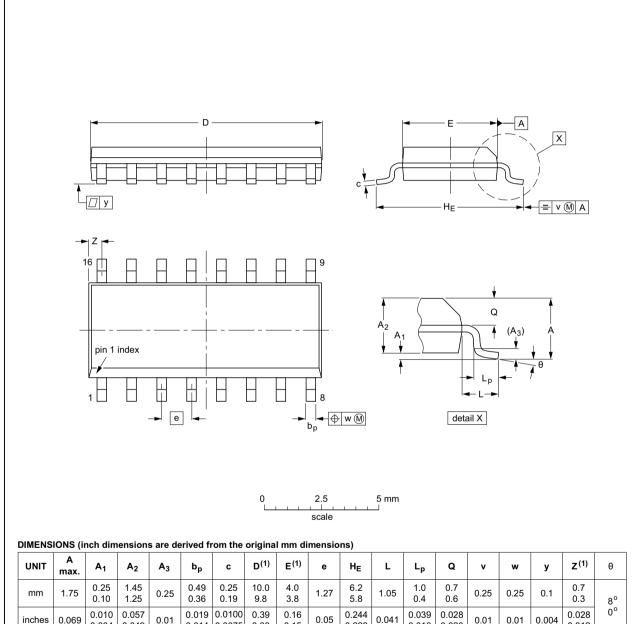
Туре	Input		Load	Test
	VI	t _r , t _f	CL	
74HC4049	V _{CC}	6.0 ns	15 pF, 50 pF	t _{PLH} , t _{PHL}

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12. Package outline

SO16: plastic small outline package; 16 leads; body width 3.9 mm

SOT109-1



U	NIT	max.	A ₁	A ₂	A ₃	b _p	С	D ⁽¹⁾	E ⁽¹⁾	е	HE	L	Lp	Q	v	w	У	Z ⁽¹⁾	θ
r	nm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	10.0 9.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8°
in	ches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.39 0.38	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.020	0.01	0.01	0.004	0.028 0.012	0°

^{1.} Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

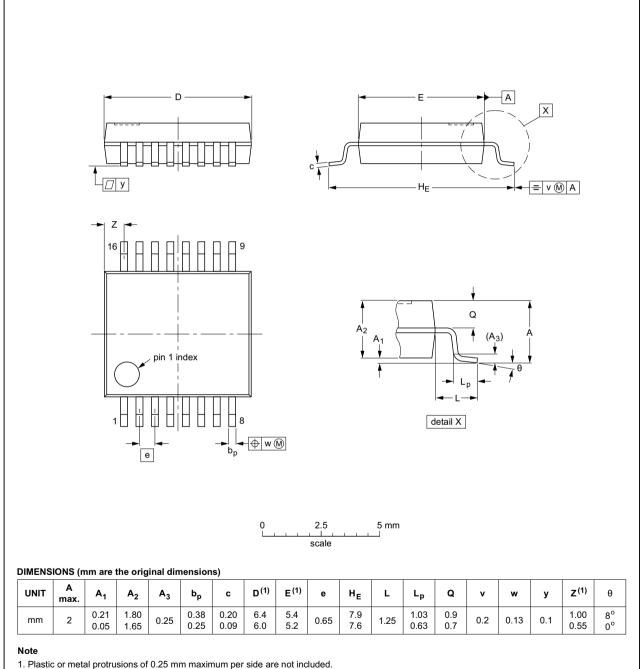
OUTLINE		REFER	ENCES	EUROPEAN	1SSUE DATE
VERSION	IEC	JEDEC	JEITA	PROJECTION	ISSUE DATE
SOT109-1	076E07	MS-012			99-12-27 03-02-19

Fig 9. Package outline SOT109-1 (SO16)

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SSOP16: plastic shrink small outline package; 16 leads; body width 5.3 mm

SOT338-1



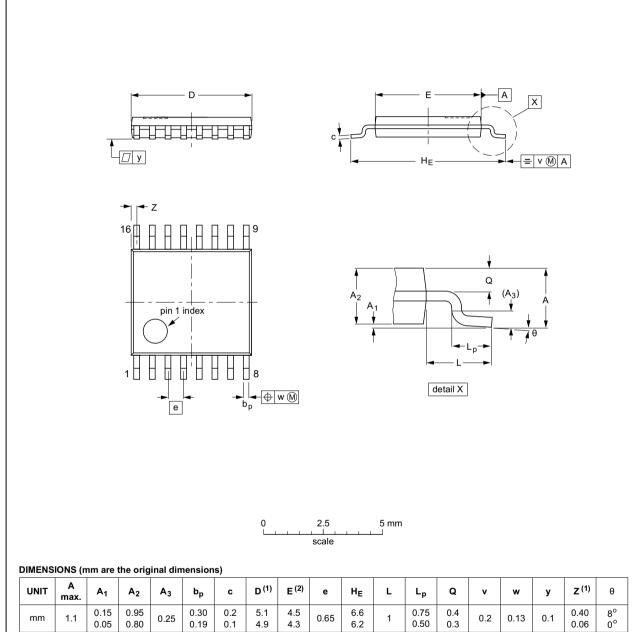
OUTLINE		REFER	ENCES	EUROPEAN	99-12-27	
VERSION	IEC	JEDEC	JEITA	PROJECTION	ISSUE DATE	
SOT338-1		MO-150			99-12-27 03-02-19	

Fig 10. Package outline SOT338-1 (SSOP16)

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TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm

SOT403-1



UNIT	A max.	A ₁	A ₂	A ₃	bp	С	D ⁽¹⁾	E (2)	е	HE	L	Lp	Q	٧	w	у	Z ⁽¹⁾	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.40 0.06	8° 0°

Notes

- 1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
- 2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE		REFER	ENCES	EUROPEAN	99-12-27	
VERSION	IEC	JEDEC	JEITA	PROJECTION	ISSUE DATE	
SOT403-1		MO-153			99-12-27 03-02-18	

Fig 11. Package outline SOT403-1 (TSSOP16)

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13. Abbreviations

Table 10. Abbreviations

Acronym	Description
CMOS	Complementary Metal Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
НВМ	Human Body Model
MM	Machine Model

14. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74HC4049 v.7	20160205	Product data sheet	-	74HC4049 v.6
Modifications:	Type num	ber 74HC4049N (SOT38-4	4) removed.	
74HC4049 v.6	20130108	Product data sheet	-	74HC4049 v.5
Modifications:	New gene	eral description.	,	
74HC4049 v.5	20120803	Product data sheet	-	74HC4049 v.4
Modifications:	 Measurer 	nent points added to figure	7 (errata).	
74HC4049 v.4	20111212	Product data sheet	-	74HC4049 v.3
74HC4049 v.3	20101230	Product data sheet	-	74HC4049_CNV v.2
74HC4049_CNV v.2	19970827	Product specification	-	-

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Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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Product [short] data sheet	Production	This document contains the product specification.

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