LPDDR4 SDRAM

MT53B128M32

Features

- Ultra-low-voltage core and I/O power supplies
  - V_{DD1} = 1.70–1.95V; 1.8V nominal
  - V_{DD2}/V_{DDQ} = 1.06–1.17V; 1.10V nominal
- Frequency range
  - 1600–10 MHz (data rate range: 3200–20 Mb/s/pin)
- 16*n* prefetch DDR architecture
- 2-channel partitioned architecture for low RD/WR energy and low average latency
- 8 internal banks per channel for concurrent operation
- Single-data-rate CMD/ADR entry
- Bidirectional/differential data strobe per byte lane
- Programmable READ and WRITE latencies (RL/WL)
- Programmable and on-the-fly burst lengths (BL = 16, 32)
- Directed per-bank refresh for concurrent bank operation and ease of command scheduling
- Up to 12.8 GB/s per die (2 channels x 6.4 GB/s)
- On-chip temperature sensor to control self refresh rate
- Partial-array self refresh (PASR)
- Selectable output drive strength (DS)
- Clock-stop capability
- RoHS-compliant, "green" packaging
- Programmable V_{SSQ} (ODT) termination

Options	Marking
• V_{DD1}/V_{DD2}: 1.8V/1.1V	B
• Array configuration	
– 128 Meg x 32 (2 - x16 channels)	128M32
• Device configuration	
– 1 x 128M32 die in package	D1
• FBGA "green" package	
– 200-ball WFBGA (10mm x 14.5mm), Ø0.28 SMD	NP
– 200-ball WFBGA (10mm x 14.5mm), Ø0.35 SMD	DS
• Speed grade, cycle time	
– 625ps @ RL = 28/32	-062
• Special option	
– standard	–
• Operating temperature range	
– –30°C to +85°C	WT
– –40°C to +95°C	IT
• Revision	:A

Table 1: Key Timing Parameters

Speed Grade	Clock Rate (MHz)	Data Rate (Mb/s/pin)	WRITE Latency Set A	WRITE Latency Set B	READ Latency (DBI Disabled)	READ Latency (DBI Enabled)
-062	1600	3200	14	26	28	32

SDRAM Addressing

The table below shows addressing for the 4Gb die density. Where applicable, a distinction is made between per-channel and per-die parameters. All bank, row, and column addresses are shown per-channel.

Table 2: Device Addressing

Configuration		**128M32 (4Gb)**
Die per package		**1**
Device density (per die)		**4Gb**
Device density (per channel)		**2Gb**
Configuration		16Mb x 16 DQ x 8 banks x 2 channels x 1 rank
Number of channels (per die)		2
Number of ranks per channel		1
Number of banks (per channel)		8
Array prefetch (bits) (per channel)		256
Number of rows (per bank)		16,384
Number of columns (fetch boundaries)		64
Page size (bytes)		2048
Channel density (bits per channel)		2,147,483,648
Total density (bits per die)		4,294,967,296
Bank address		BA[2:0]
x16	Row addresses	R[13:0]
	Column addresses	C[9:0]
Burst starting address boundary		64-bit

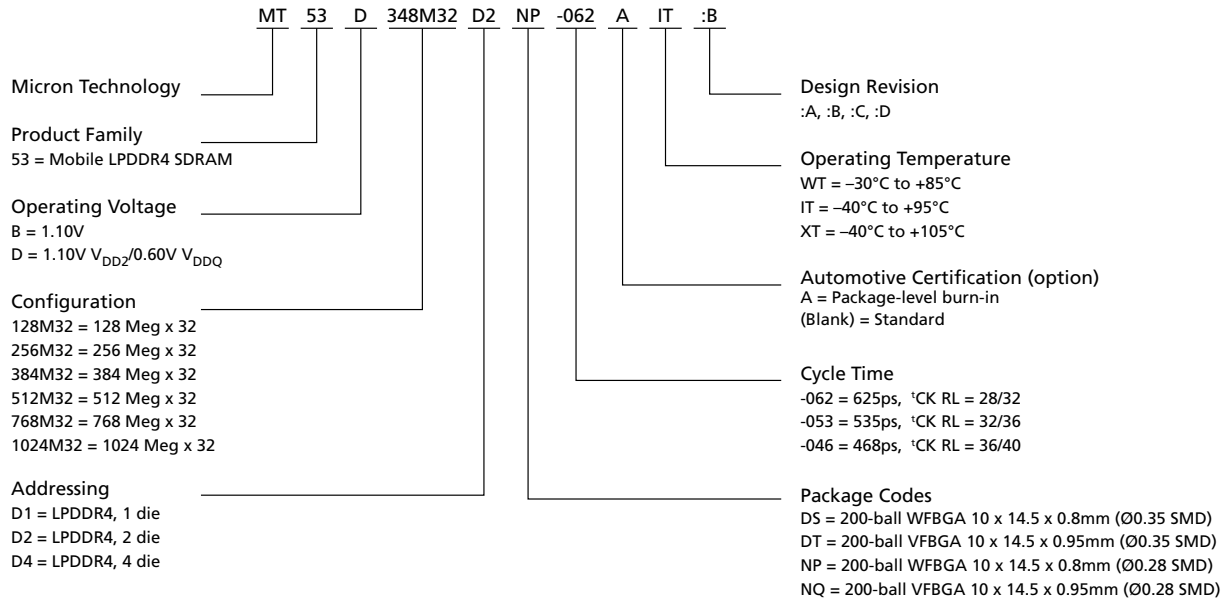
Notes:
1. The lower two column addresses (C0–C1) are assumed to be zero and are not transmitted on the CA bus.
2. Row and column address values on the CA bus that are not used for a particular density are "Don't Care."
3. For non-binary memory densities, only half of the row address space is valid. When the MSB address bit is HIGH, the MSB - 1 address bit must be LOW.

Part Number and Part Marking Information

Part Number Ordering

Micron LPDDR4 devices are available in different configurations and densities. Verify valid part numbers by using Micron's part catalog search at www.micron.com. To compare features and specifications by device type, visit www.micron.com/products. Contact the factory for devices not found.

Figure 1: Part Number Chart



FBGA Part Marking Decoder

Due to space limitations, FBGA-packaged components have an abbreviated part marking that is different from the part number. Micron's FBGA part marking decoder is available at www.micron.com/decoder.

Full specification can be acquired through a Micron representative and under NDA