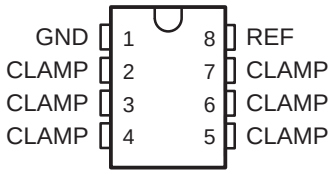
- **Protects Against Latch-Up**
- **25-mA Current Sink in Active State**
- **Less Than 1-mW Dissipation in Standby Condition**
- **Ideal for Applications in Environments Where Large Transient Spikes Occur**
- **Stable Operation for All Values of Capacitive Load**
- **No Output Overshoot**

D OR P PACKAGE
(TOP VIEW)



description

The TL7726 consists of six identical clamping circuits that monitor an input voltage with respect to a reference value, REF. For an input voltage (V_I) in the range of GND to < REF, the clamping circuits present a very high impedance to ground, drawing current of less than 10 μA. The clamping circuits are active for V_I < GND or V_I > REF when they have a very low impedance and can sink up to 25 mA.

These characteristics make the TL7726 ideal as protection devices for CMOS semiconductor devices in environments where there are large positive or negative transients to protect analog-to-digital converters in automotive or industrial systems. The use of clamping circuits provides a safeguard against potential latch-up.

The TL7726C is characterized for operation over the temperature range of 0°C to 70°C. The TL7726I is characterized for operation over the temperature range of –40°C to 85°C. The TL7726Q is characterized for operation over the temperature range of –40°C to 125°C.

AVAILABLE OPTIONS

T_A	SOIC (D)	PLASTIC DIP (P)
0°C to 70°C	TL7726CD	TL7726CP
–40°C to 85°C	TL7726ID	TL7726IP
–40°C to 125°C	TL7726QD	TL7726QP

The D package is available taped and reeled. Add the suffix R to the device type (i.e., TL7726CDR).

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

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absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Reference voltage, V_{ref} . . . . . 6 V
Clamping current, I_{IK} . . . . . ±50 mA
Junction temperature, T_J . . . . . 150°C
Package thermal impedance, θ_{JA} (see Notes 1 and 2): D package . . . . . 97°C/W
P package . . . . . 127°C/W
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C
Storage temperature range, T_{stg} . . . . . –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. Maximum power dissipation is a function of $T_J(max)$, θ_{JA}, and T_A. The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_J(max) – T_A)/\theta_{JA}$. Operating at the absolute maximum T_J of 150°C can impact reliability.
2. The package thermal impedance is calculated in accordance with JESD 51, except for through-hole packages, which use a trace length of zero.

recommended operating conditions

		MIN	MAX	UNIT
Reference voltage, V_{ref}		4.5	5.5	V
Input clamping current, I_{IK}	$V_I \geq V_{ref}$		25	mA
	$V_I \leq$ GND	–25		
Operating free-air temperature range, T_A	TL7726C	0	70	°C
	TL7726I	–40	85	
	TL7726Q	–40	125	

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

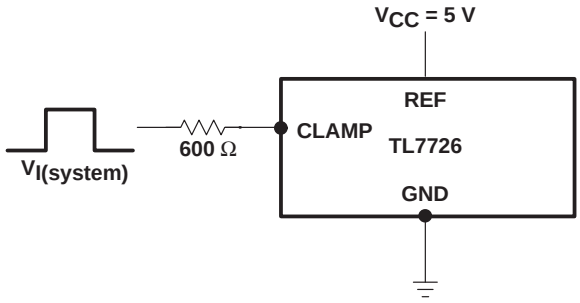
PARAMETER		TEST CONDITIONS	MIN	TYP‡	MAX	UNIT
V_{IK+}	Positive clamp voltage	I_I = 20 mA	V_{ref}		V_{ref} + 200	mV
$V_{IK–}$	Negative clamp voltage	I_I = 20 mA	–200		0	mV
I_Z	Reference current	V_{ref} = 5 V		25	60	µA
I_I	Input current	V_{ref} – 50 mV ≤ V_I ≤ V_{ref}			10	µA
		GND ≤ V_I ≤ 50 mV	–10			
		50 mV ≤ V_I ≤ V_{ref} – 50 mV	–1		1	

‡ All typical values are at T_A = 25°C.

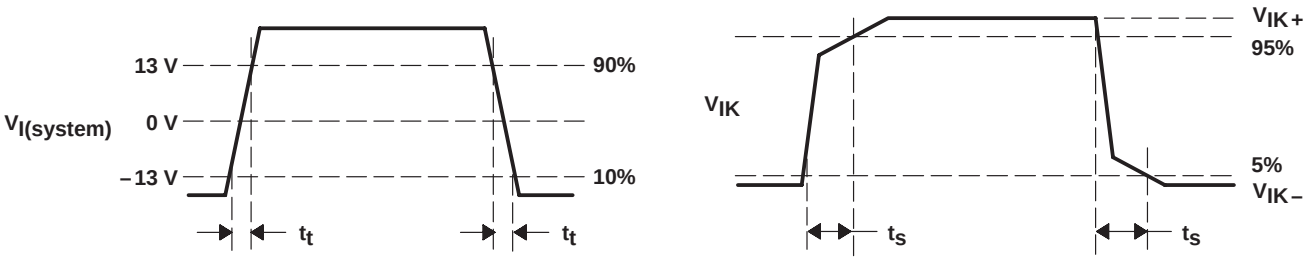
switching characteristics specified at T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
t_s	Settling time	$V_{I(system)}$ = ±13 V, R_I = 600 Ω, t_t < 1 µs, Measured at 10% to 90%, See Figure 1		30	µs

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



INPUT WAVEFORM

CLAMP WAVEFORM

Figure 1. Switching Characteristics

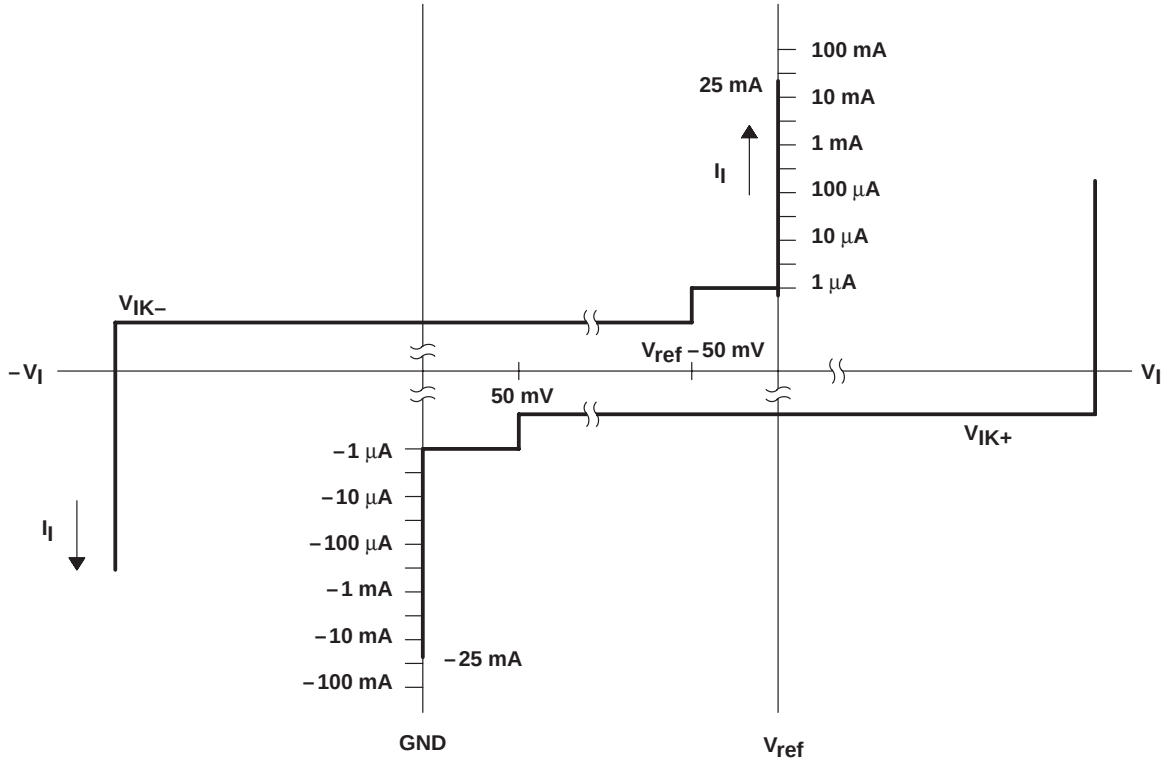
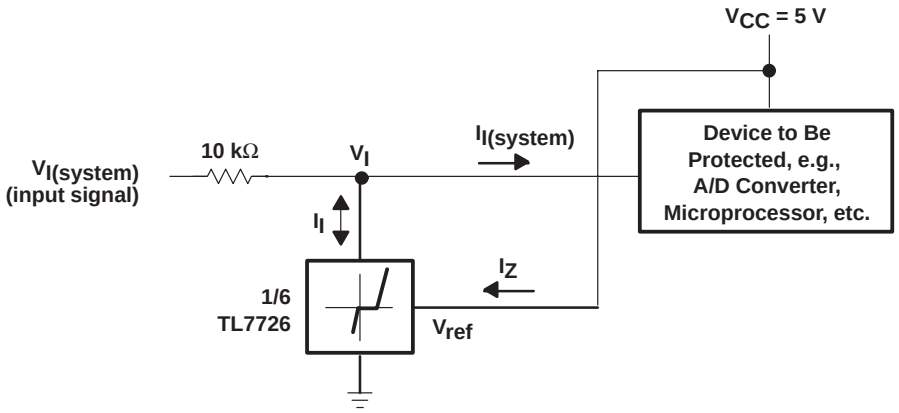


Figure 2. Tolerance Band for Clamping Circuit

APPLICATION INFORMATION



Example: If $I_I >> I_{I(system)}$, i.e., $V_{I(system)} > V_{ref}$ + 200 mV
where:

$I_{I(system)}$ = Input current to the device being protected
$V_{I(system)}$ = Input voltage to the device being protected

then the maximum input voltage

$V_{I(system)max} = V_{ref} + I_I max(10k\Omega)$
$= 5\ V + 25\ mA(10k\Omega)$
$= 5\ V + 250\ V$
$= 255\ V$

Figure 3. Typical Application

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
TL7726CD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1YEAR
TL7726CDE4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1YEAR
TL7726CDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1YEAR
TL7726CDRE4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1YEAR
TL7726CP	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
TL7726CPE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
TL7726ID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1YEAR
TL7726IDE4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1YEAR
TL7726IDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1YEAR
TL7726IDRE4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1YEAR
TL7726IP	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
TL7726IPE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
TL7726QD	ACTIVE	SOIC	D	8	75	TBD	CU NIPDAU	Level-1-220C-UNLIM
TL7726QDR	ACTIVE	SOIC	D	8	2500	TBD	CU NIPDAU	Level-1-220C-UNLIM
TL7726QP	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPD	N / A for Pkg Type

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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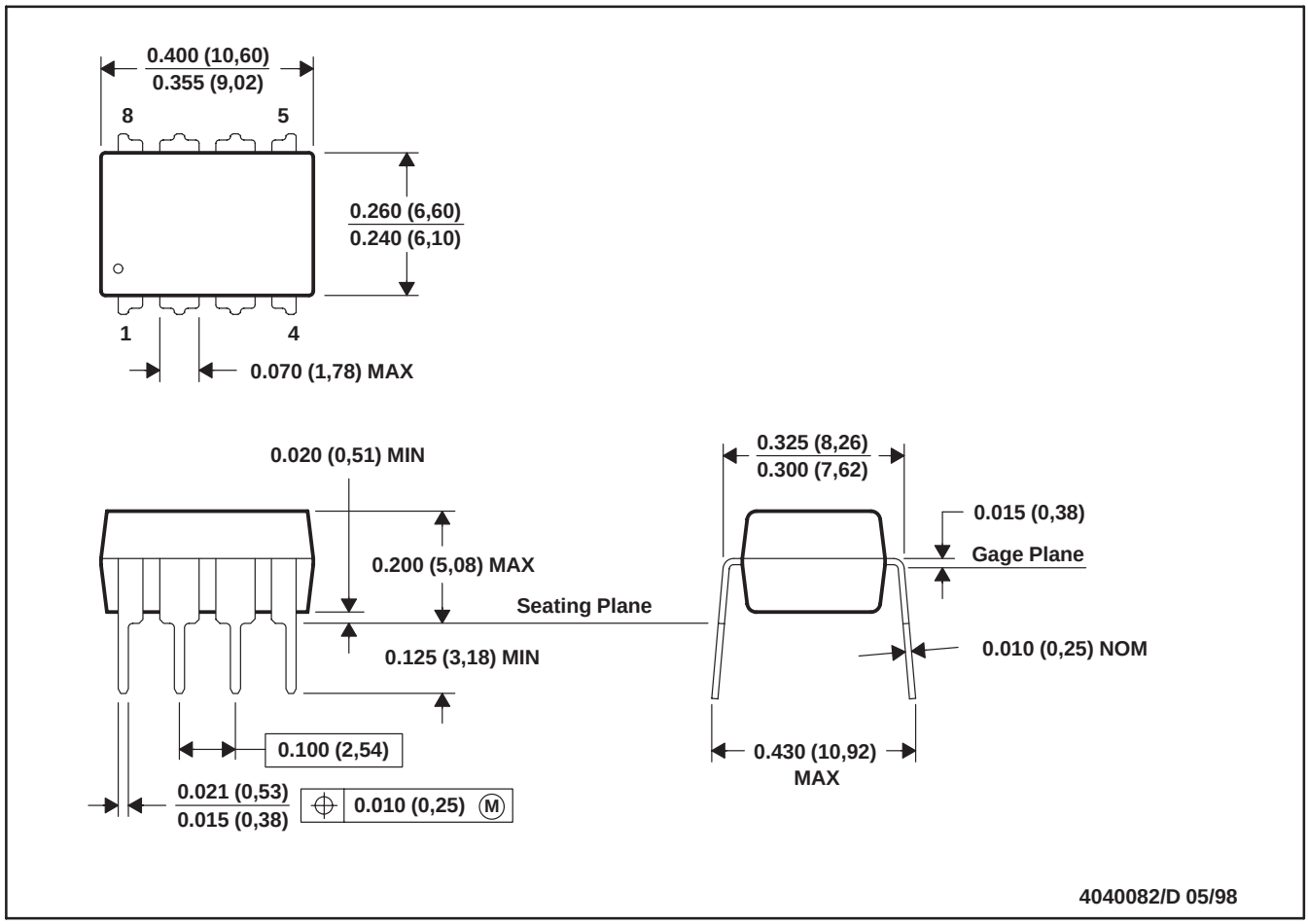
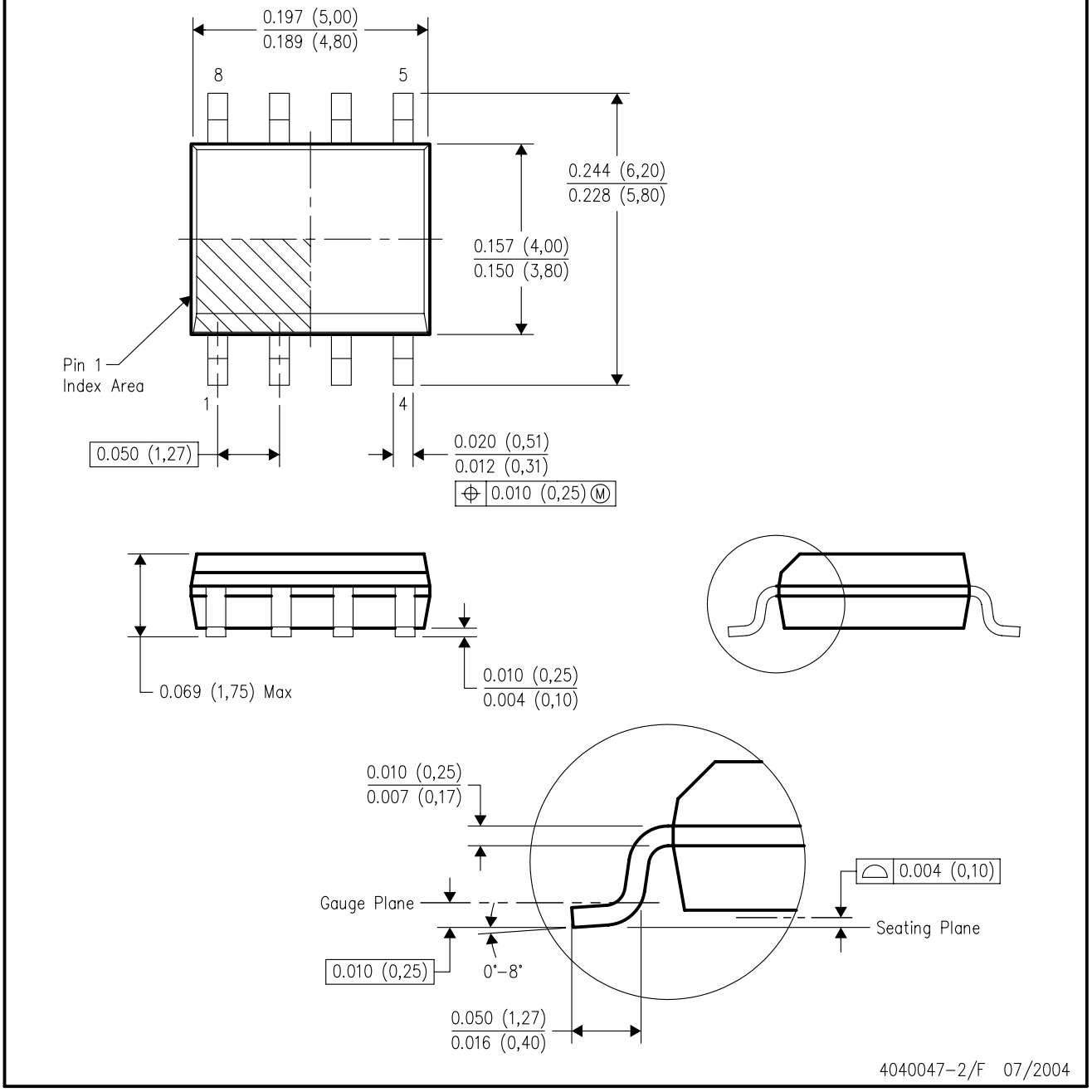
P (R-PDIP-T8) **PLASTIC DUAL-IN-LINE**



NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-001

For the latest package information, go to http://www.ti.com/sc/docs/package/pkg_info.htm

D (R–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MS–012 variation AA.

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