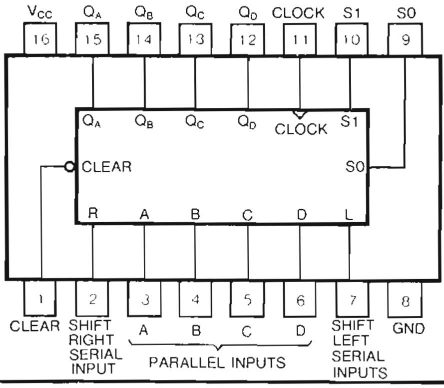
GD54/74LS194A

4-BIT BIDIRECTIONAL UNIVERSAL SHIFT REGISTER

Feature

- Parallel Inputs and Outputs
- Four Operating Modes;
  - Synchronous Parallel Load
  - Right Shift
  - Left Shift
  - Do Nothing
- Positive Edge-Triggered Clocking
- Direct Overding Clear

Pin Configuration



Suffix-Blank: Plastic Dual In Line Package
Suffix-J . Ceramic Dual In Line Package

Description

This bidirectional shift register is designed to incorporate virtually all of the features a system designer may want in a shift register. The circuit contains 46 equivalent gates and features parallel inputs, parallel outputs, right-shift and left shift serial inputs, operating-mode-control inputs, and a direct overriding clear line. The register has four distinct modes of operation, namely:

Parallel (broadside) load
Shift right (in the direction Q_A toward Q_D)
Shift left (in the direction Q_D toward Q_A)
Inhibit clock (do nothing)

Synchronous parallel loading is accomplished by applying the four bits of data and taking both mode control inputs, SO and S1, high. The data are loaded into the associated flip-flops and appear and outputs after the positive transition of the clock input. During loading, serial data flow is inhibited.

Shift right is accomplished synchronously with the rising edge of the clock pulse when SO is high and S1 is low. Serial data for this mode is entered at the shift-right data input. When SO is low and S1 is high, data shifts left synchronously and new data is entered at the shift-left serial input.

Function Table

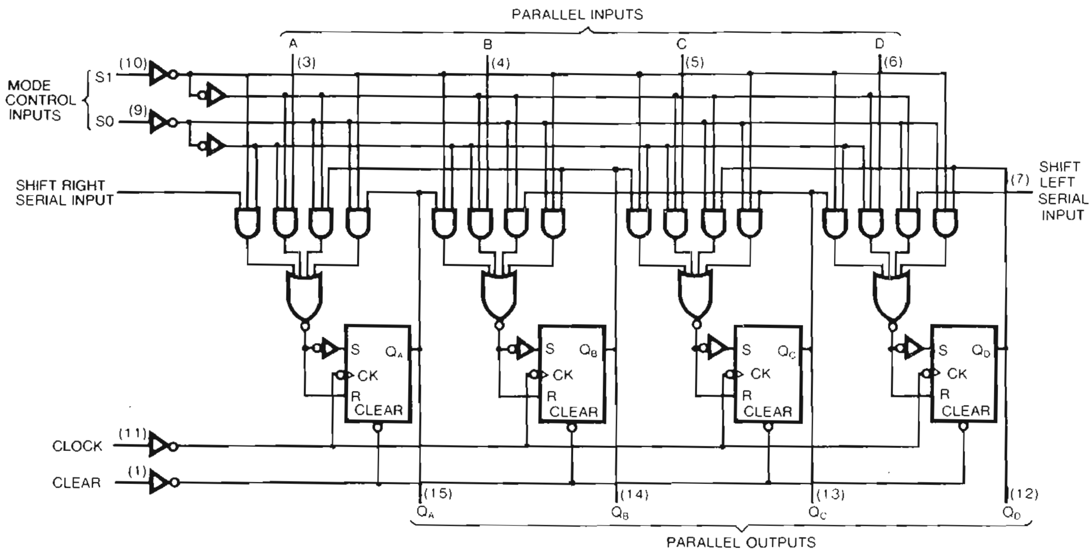
INPUTS							OUTPUTS			
CLEAR	MODE		CLOCK	SERIAL		PARALLEL	Q_A	Q_B	Q_C	Q_D
	S1	SO		LEFT	RIGHT	A B C D				
L	X	X	X	X	X	X X X X	L	L	L	L
H	X	X	L	X	X	X X X X	Q_{AO}	Q_{BO}	Q_{CO}	Q_{DO}
H	H	H	↑	X	X	a b c d	a	b	c	d
H	L	H	↑	X	H	X X X X	H	Q_{An}	Q_{Bn}	Q_{Cn}
H	L	H	↑	X	L	X X X X	L	Q_{An}	Q_{Bn}	Q_{Cn}
H	H	L	↑	H	X	X X X X	Q_{Bn}	Q_{Cn}	Q_{Dn}	H
H	H	L	↑	L	X	X X X X	Q_{Bn}	Q_{Cn}	Q_{Dn}	L
H	L	L	X	X	X	X X X X	Q_{AO}	Q_{BO}	Q_{CO}	Q_{DO}

H=high level (steady state)
L=low level (steady state)
X=irrelevant (any input, including transitions)
↑=transition from low to high level
a,b,c,d=the level of steady state input at inputs A, B, C, or D, respectively.
Q_{AO}, Q_{BO}, Q_{CO}, Q_{DO}=the level of Q_A, Q_B, Q_C or Q_D, respectively, before the indicated steady state input conditions were established.
Q_{An}, Q_{Bn}, Q_{Cn}, Q_{Dn}=the level of Q_A, Q_B, Q_C or Q_D respectively, before the mostrecent ↑ transition of the clock.

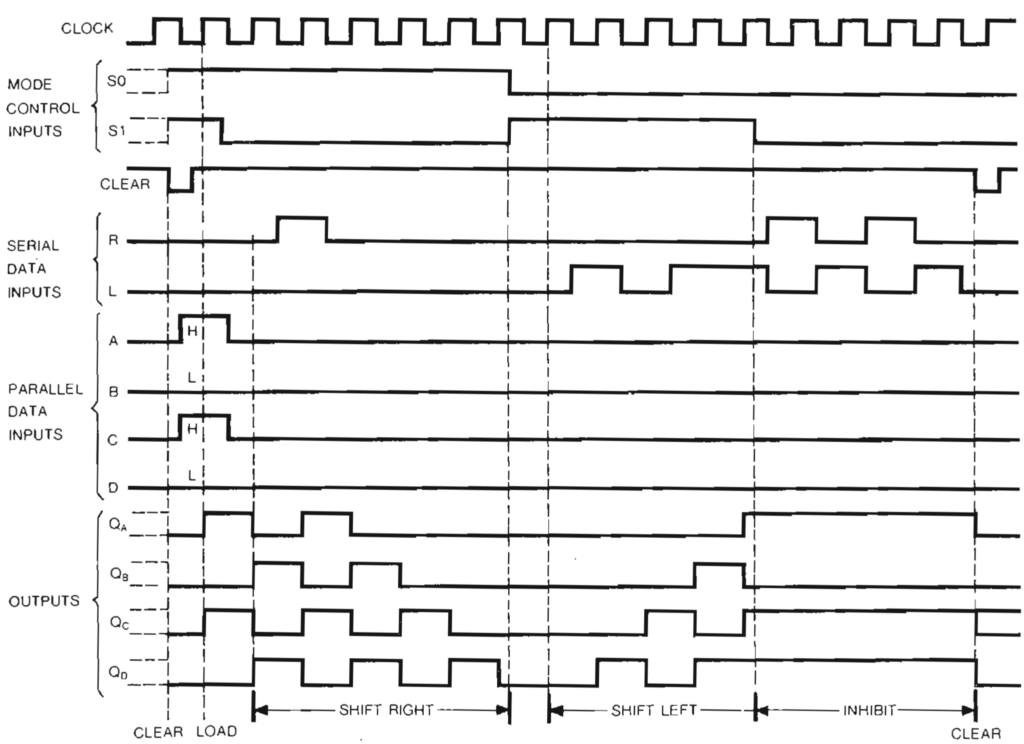
Absolute Maximum Ratings

- Supply voltage, Vcc 7V
- Input voltage 7V
- Operating free-air temperature range 54LS .... −55°C to 125°C
  74LS .... 0°C to 70°C
- Storage temperature range .... −65°C to 150°C

Function Block Diagram



Typical Clear, Load, Right-Shift, Inhibit, and Clear Sequences.



Recommended Operating Conditions

SYMBOL	PARAMETER			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		54	4.5	5	5.5	V
			74	4.75	5	5.25	
I_{OH}	High-level output current		54,74			−400	μA
I_{OL}	Low-level output current		54			4	mA
			74			8	
f_{clock}	Clock frequency			0		25	MHz
t_w	Width of clock or clear pulse			20			ns
t_{su}	Set up time	Mode control		30			ns
		Serial and parallel data		20			ns
		Clear inactive-state		25			
t_h	Hold time at any input			0			ns
T_A	Operating free-air temperature		54	−55		125	°C
			74	0		70	

Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

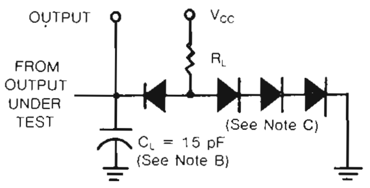
SYMBOL	PARAMETER	TEST CONDITIONS			MIN	TYP (Note 1)	MAX	UNIT
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage			54			0.7	V
				74			0.8	
V_{IK}	Input clamp voltage	V_{CC}=Min, I_I=−18mA					−1.5	V
V_{OH}	High-level output voltage	V_{CC}=Min, V_{IL}=Max		54	2.5	3.4		V
		I_{OH}=Max, V_{IH}=Min		74	2.7	3.4		
V_{OL}	Low-level output voltage	V_{CC}=Min V_{IL}=Max V_{IH}=Min	I_{OL}=4mA	54,74		0.25	0.4	V
			I_{OL}=8mA	74		0.35	0.5	
I_I	Input current at maximum input voltage	V_{CC}=Max, V_I=7V					0.1	mA
I_{IH}	High-level input current	V_{CC}=Max, V_I=2.7V					20	μA
I_{IL}	Low-level input current	V_{CC}=Max, V_I=0.4V					−0.4	mA
I_{OS}	Short-circuit output current	V_{CC}=Max (Note 2)			−20		−100	mA
I_{CC}	Supply current	V_{CC}=5.25V, (Note 3)				15	23	mA

Note 1: All typical values are at V_{CC}=5V, T_A=25°C.
Note 2: Not more than one output should be shorted at a time, and duration should not exceed one second.
Note 3: With all outputs open and 4.5V applied to all data and clear inputs. I_{CC} is measured after a momentary ground, then 4.5V is applied to clock.

Switching Characteristics, V_{CC}=5V, T_A=25°C

SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
f_{max}	Maximum clock frequency	C_L=15pF, R_L=2kΩ See Figure 1	25	36		MHz
t_{PHL}	Propagation delay time, high-to-low level output from clear			19	30	ns
t_{PLH}	Propagation delay time, low-to-high level outputs from clock			14	22	ns
t_{PHL}	Propagation delay time, high-to-low level output from clock			17	26	ns

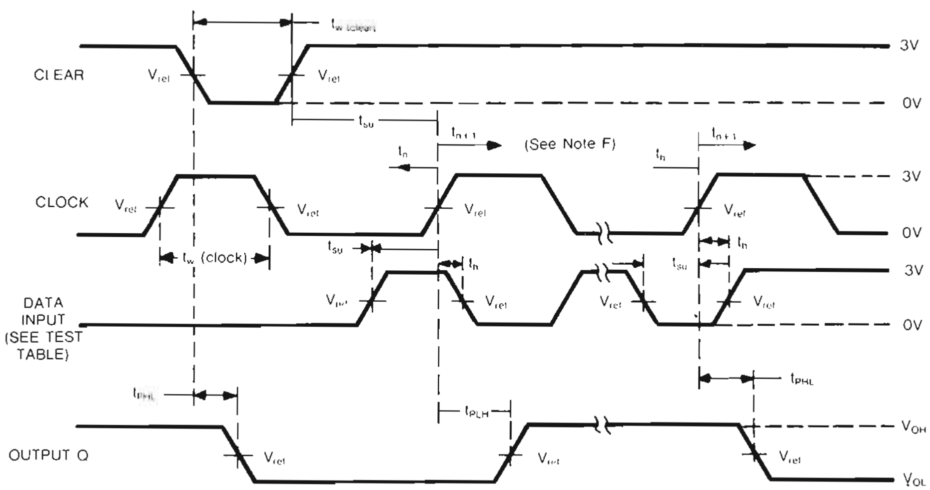
Parameter Measurement Information



LOAD FOR OUTPUT UNDER TEST

Test Table for Synchronous Inputs

Data Input For Test	S1	S0	Output Tested (See Note E)
A	4.5V	4.5V	Q_A at t_{n+1}
B	4.5V	4.5V	Q_B at t_{n+1}
C	4.5V	4.5V	Q_C at t_{n+1}
D	4.5V	4.5V	Q_D at t_{n+1}
L Serial Input	4.5V	0V	Q_A at t_{n+4}
R Serial Input	0V	4.5V	Q_D at t_{n+4}



VOLTAGE WAVEFORMS

Note: A. The clock pulse generator has the following characteristics: $Z_{out} \approx 500\Omega$ and PRR$\leqslant$1MHz, tr$\leqslant$15ns and tf$\leqslant$6ns
B. C_L includes probe and jig capacitance.
C. All diodes are 1N3064 or 1N916
D. A clear pulse is applied prior to each test.
E. V_{ref} = 1.3V
F. Propagation delay times (t_{PLH} and t_{PHL}) are measured at t_{n+1}
Proper shifting of data is verified at t_{n+4} with a function test
G. t_n = bit time before clocking transition.
t_{n+1} = bit time after one clocking transition.
t_{n+4} = bit time after four clocking transition.

Figure 1. Switching Times