



## CD4034BM/CD4034BC 8-Stage TRI-STATE® Bidirectional Parallel/Serial Input/Output Bus Register

### General Description

The CD4034BM/CD4034BC is an 8-bit CMOS static shift register with two parallel bidirectional data ports (A and B) which, when combined with serial shifting operations, can be used to (1) bidirectionally transfer parallel data between two buses, (2) convert serial data to parallel form and direct them to either of two buses, (3) store (recirculate) parallel data, or (4) accept parallel data from either of two buses and convert them to serial form. These operations are controlled by five control inputs:

**A ENABLE (AE):** "A" data port is enabled only when AE is at logical "1". This allows the use of a common bus for multiple packages.

**A-BUS-TO-B-BUS/B-BUS-TO-A-BUS (A/B):** This input controls the direction of data flow. When at logical "1", data flows from port A to B (A is input, B is output). When at logical "0", the data flow direction is reversed.

**ASYNCHRONOUS/SYNCHRONOUS (A/S):** When A/S is at logical "0", data transfer occurs at positive transition of the CLOCK. When A/S is at logical "1", data transfer is independent of the CLOCK for parallel operation. In serial mode, A/S input is internally disabled such that operation is always synchronous. (Asynchronous serial operation is not possible.)

**PARALLEL/SERIAL (P/S):** A logical "1" P/S input allows data transfer into the registers via A or B port (synchronous if A/S = logical "0", asynchronous if A/S = logical "1"). A logical "0" P/S allows serial data to transfer into the register synchronously with the positive transition of the CLOCK, independent of the A/S input.

**CLOCK:** Single phase, enabled only in synchronous mode. (Either P/S = logical "1" and A/S = logical "0" or P/S = logical "0".)

All register stages are D-type master-slave flip-flops with separate master and slave clock inputs generated internally to allow synchronous or asynchronous data transfer from master to slave.

All inputs are protected against damage due to static discharge by diode clamps to  $V_{DD}$  and  $V_{SS}$ .

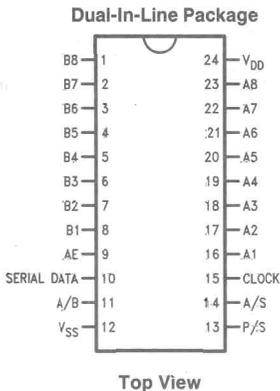
### Features

- Wide supply voltage range 3.0V to 16V
- High noise immunity 0.45  $V_{DD}$  (typ.)
- Low power TTL compatibility Fan out of 2 driving 74L or 1 driving 74LS
- RCA CD4034B second source

### Applications

- Parallel Input/Parallel Output
- Parallel Input/Serial Output
- Serial Input/Parallel Output
- Serial Input/Serial Output register
- Shift right/shift left register
- Shift right/shift left with parallel loading
- Address register
- Buffer register
- Bus system register with enable parallel lines at bus side
- Double bus register system
- Up-down Johnson or ring counter
- Pseudo-random code generators
- Sample and hold register (storage, counting, display)
- Frequency and phase comparator

### Connection Diagram



Order Number CD4034B\*

\*Please look into Section 8, Appendix D for availability of various package types.

TU/F/5193-1

**Absolute Maximum Ratings** (Notes 1 & 2)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/Distributors for availability and specifications.

|                                |  |
|--------------------------------|--|
| DC Supply Voltage ( $V_{DD}$ ) | -0.5 $V_{DC}$ to +18 $V_{DC}$            |
| Input Voltage ( $V_{IN}$ )     | -0.5 $V_{DC}$ to $V_{DD}$ + 0.5 $V_{DC}$ |
| Storage Temp. Range ( $T_S$ )  | -65°C to +150°C                          |
| Power Dissipation ( $P_D$ )    |  |
| Dual-In-Line                   | 700 mW                                   |
| Small Outline                  | 500 mW                                   |
| Lead Temperature ( $T_L$ )     |  |
| (Soldering, 10 seconds)        | 260°C                                    |

**Recommended Operating Conditions** (Note 2)

|                                       |                                 |
|---------------------------------------|---------------------------------|
| DC Supply Voltage ( $V_{DD}$ )        | +3 $V_{DC}$ to +15 $V_{DC}$     |
| Input Voltage ( $V_{IN}$ )            | 0 $V_{DC}$ to $V_{DD}$ $V_{DC}$ |
| Operating Temperature Range ( $T_A$ ) |                                 |
| CD4034BM                              | -55°C to +125°C                 |
| CD4034BC                              | -40°C to +85°C                  |

**DC Electrical Characteristics** CD4034BM (Note 2)

| Symbol   | Parameter                             | Conditions   | -55°C                 |                      | +25°C                 |                                       |     | +125°C               |                       | Units                         |
|----------|---------------------------------------|--|-----------------------|----------------------|-----------------------|---------------------------------------|-----|----------------------|-----------------------|-------------------------------|
|          |                                       |  | Min                   | Max                  | Min                   | Typ                                   | Max | Min                  | Max                   |                               |
| $I_{DD}$ | Quiescent Device Current              | $V_{DD} = 5V, V_{IN} = V_{DD}$ or $V_{SS}$<br>$V_{DD} = 10V, V_{IN} = V_{DD}$ or $V_{SS}$<br>$V_{DD} = 15V, V_{IN} = V_{DD}$ or $V_{SS}$ |                       | 5<br>10<br>20        |                       |                                       |     | 5<br>10<br>20        | 150<br>300<br>600     | $\mu A$<br>$\mu A$<br>$\mu A$ |
| $V_{OL}$ | Low Level Output Voltage              | $V_{DD} = 5V$<br>$V_{DD} = 10V$<br>$V_{DD} = 15V$  |                       | 0.05<br>0.05<br>0.05 |                       |                                       |     | 0.05<br>0.05<br>0.05 | 0.05<br>0.05<br>0.05  | V<br>V<br>V                   |
| $V_{OH}$ | High Level Output Voltage             | $V_{DD} = 5V$<br>$V_{DD} = 10V$<br>$V_{DD} = 15V$  | 4.95<br>9.95<br>14.95 |                      | 4.95<br>9.95<br>14.95 |                                       |     |                      | 4.95<br>9.95<br>14.95 | V<br>V<br>V                   |
| $V_{IL}$ | Low Level Input Voltage               | $V_{DD} = 5V, V_O = 0.5V$ or 4.5V<br>$V_{DD} = 10V, V_O = 1.0V$ or 9.0V<br>$V_{DD} = 15V, V_O = 1.5V$ or 13.5V                           |                       | 1.5<br>3.0<br>4.0    |                       |                                       |     | 1.5<br>3.0<br>4.0    | 1.5<br>3.0<br>4.0     | V<br>V<br>V                   |
| $V_{IH}$ | High Level Input Voltage              | $V_{DD} = 5V, V_O = 0.5V$ or 4.5V<br>$V_{DD} = 10V, V_O = 1.0V$ or 9.0V<br>$V_{DD} = 15V, V_O = 1.5V$ or 13.5V                           | 3.5<br>7.0<br>11.0    |                      | 3.5<br>7.0<br>11.0    |                                       |     |                      | 3.5<br>7.0<br>11.0    | V<br>V<br>V                   |
| $I_{OL}$ | Low Level Output Current<br>(Note 3)  | $V_{DD} = 5V, V_O = 0.4V$<br>$V_{DD} = 10V, V_O = 0.5V$<br>$V_{DD} = 15V, V_O = 1.5V$  | 0.64<br>1.6<br>4.2    |                      | 0.51<br>1.3<br>3.4    |                                       |     |                      | 0.36<br>0.9<br>2.4    | mA<br>mA<br>mA                |
| $I_{OH}$ | High Level Output Current<br>(Note 3) | $V_{DD} = 5V, V_O = 4.6V$<br>$V_{DD} = 10V, V_O = 9.5V$<br>$V_{DD} = 15V, V_O = 13.5V$   | -0.64<br>-1.6<br>-4.2 |                      | -0.51<br>-1.3<br>-3.4 |                                       |     |                      | -0.36<br>-0.9<br>-2.4 | mA<br>mA<br>mA                |
| $I_{IN}$ | Input Current                         | $V_{DD} = 15V, V_{IN} = 0V$<br>$V_{DD} = 15V, V_{IN} = 15V$  | -0.1                  | 0.1                  | -0.1                  | -10 <sup>-5</sup><br>10 <sup>-5</sup> | 0.1 | -1.0                 | 1.0                   | $\mu A$<br>$\mu A$            |
| $I_{OZ}$ | TRI-STATE Leakage Current             | $V_{DD} = 15V, V_O = 0V$<br>$V_{DD} = 15V, V_O = 15V$  | -0.1                  | 0.1                  | -0.1                  | -10 <sup>-5</sup><br>10 <sup>-5</sup> | 0.1 | -1.0                 | 1.0                   | $\mu A$<br>$\mu A$            |

**Note 1:** "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

**Note 2:**  $V_{SS} = 0V$  unless otherwise specified.

**Note 3:**  $I_{OH}$  and  $I_{OL}$  are tested one output at a time.

## DC Electrical Characteristics CD4034BC (Note 2)

| Symbol   | Parameter                             | Conditions  | -40°C                 |                      | +25°C                 |                         |                      | +85°C                 |                      | Units                         |
|----------|---------------------------------------|---|-----------------------|----------------------|-----------------------|-------------------------|----------------------|-----------------------|----------------------|-------------------------------|
|          |                                       |   | Min                   | Max                  | Min                   | Typ                     | Max                  | Min                   | Max                  |                               |
| $I_{DD}$ | Quiescent Device Current              | $V_{DD} = 5V, V_{IN} = V_{DD} \text{ or } V_{SS}$<br>$V_{DD} = 10V, V_{IN} = V_{DD} \text{ or } V_{SS}$<br>$V_{DD} = 15V, V_{IN} = V_{DD} \text{ or } V_{SS}$ |                       | 20<br>40<br>80       |                       |                         | 20<br>40<br>80       |                       | 150<br>300<br>600    | $\mu A$<br>$\mu A$<br>$\mu A$ |
| $V_{OL}$ | Low Level Output Voltage              | $V_{DD} = 5V$<br>$V_{DD} = 10V$<br>$V_{DD} = 15V$   |                       | 0.05<br>0.05<br>0.05 |                       |                         | 0.05<br>0.05<br>0.05 |                       | 0.05<br>0.05<br>0.05 | V<br>V<br>V                   |
| $V_{OH}$ | High Level Output Voltage             | $V_{DD} = 5V$<br>$V_{DD} = 10V$<br>$V_{DD} = 15V$   | 4.95<br>9.95<br>14.95 |                      | 4.95<br>9.95<br>14.95 |                         |                      | 4.95<br>9.95<br>14.95 |                      | V<br>V<br>V                   |
| $V_{IL}$ | Low Level Input Voltage               | $V_{DD} = 5V, V_O = 0.5V \text{ or } 4.5V$<br>$V_{DD} = 10V, V_O = 1.0V \text{ or } 9.0V$<br>$V_{DD} = 15V, V_O = 1.5V \text{ or } 13.5V$                     |                       | 1.5<br>3.0<br>4.0    |                       |                         | 1.5<br>3.0<br>4.0    |                       | 1.5<br>3.0<br>4.0    | V<br>V<br>V                   |
| $V_{IH}$ | High Level Input Voltage              | $V_{DD} = 5V, V_O = 0.5V \text{ or } 4.5V$<br>$V_{DD} = 10V, V_O = 1.0V \text{ or } 9.0V$<br>$V_{DD} = 15V, V_O = 1.5V \text{ or } 13.5V$                     | 3.5<br>7.0<br>11.0    |                      | 3.5<br>7.0<br>11.0    |                         |                      | 3.5<br>7.0<br>11.0    |                      | V<br>V<br>V                   |
| $I_{OL}$ | Low Level Output Current<br>(Note 3)  | $V_{DD} = 5V, V_O = 0.4V$<br>$V_{DD} = 10V, V_O = 0.5V$<br>$V_{DD} = 15V, V_O = 1.5V$   | 0.52<br>1.3<br>3.6    |                      | 0.44<br>1.1<br>3.0    |                         |                      | 0.36<br>0.9<br>2.4    |                      | mA<br>mA<br>mA                |
| $I_{OH}$ | High Level Output Current<br>(Note 3) | $V_{DD} = 5V, V_O = 4.6V$<br>$V_{DD} = 10V, V_O = 9.5V$<br>$V_{DD} = 15V, V_O = 13.5V$  | -0.52<br>-1.3<br>-3.6 |                      | -0.44<br>-1.1<br>-3.0 |                         |                      | -0.36<br>-0.9<br>-2.4 |                      | mA<br>mA<br>mA                |
| $I_{IN}$ | Input Current                         | $V_{DD} = 15V, V_{IN} = 0V$<br>$V_{DD} = 15V, V_{IN} = 15V$   | -0.3                  | 0.3                  | -0.3                  | $-10^{-5}$<br>$10^{-5}$ | 0.3                  | -1.0                  | 1.0                  | $\mu A$<br>$\mu A$            |
| $I_{OZ}$ | TRI-STATE Leakage<br>Current          | $V_{DD} = 15V, V_O = 0V$<br>$V_{DD} = 15V, V_O = 15V$   | -0.3                  | 0.3                  | -0.3                  | $-10^{-5}$<br>$10^{-5}$ | 0.3                  | -1.0                  | 1.0                  | $\mu A$<br>$\mu A$            |

## AC Electrical Characteristics\*

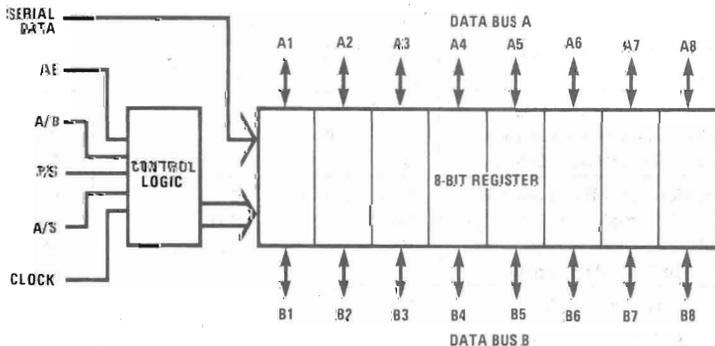
$T_A = 25^\circ C, C_L = 50 \text{ pF}, R_L = 200k, \text{input } t_r = t_f = 20 \text{ ns, unless otherwise specified}$

| Symbol             | Parameter   | Conditions   | Min | Typ              | Max               | Units          |
|--------------------|---|--|-----|------------------|-------------------|----------------|
| $t_{PHL}, t_{PLH}$ | Propagation Delay Time, A (B)<br>Synchronous Parallel Data or Serial<br>Data Input, B (A) Parallel Data<br>Output   | $V_{DD} = 5V$<br>$V_{DD} = 10V$<br>$V_{DD} = 15V$  |     | 280<br>120<br>85 | 700<br>270<br>190 | ns<br>ns<br>ns |
| $t_{PHL}, t_{PLH}$ | Propagation Delay Time, A (B)<br>A (B) Asynchronous Parallel Data<br>Input, B (A) Parallel Data Output  | $V_{DD} = 5V$<br>$V_{DD} = 10V$<br>$V_{DD} = 15V$  |     | 280<br>120<br>85 | 700<br>270<br>190 | ns<br>ns<br>ns |
| $t_{PHZ}, t_{PLZ}$ | Propagation Delay Time from A/B<br>or AE to High Impedance State at A<br>Outputs or from A/B to High<br>Impedance State at B Outputs                            | $V_{DD} = 5V, R_L = 1.0 \text{ k}\Omega$<br>$V_{DD} = 10V, R_L = 1.0 \text{ k}\Omega$<br>$V_{DD} = 15V, R_L = 1.0 \text{ k}\Omega$ |     | 95<br>60<br>45   | 220<br>130<br>100 | ns<br>ns<br>ns |
| $t_{PZH}, t_{PZL}$ | Propagation Delay Time from A/B<br>or AE to Logical "1" or Logical "0"<br>State at A Outputs or from A/B to<br>Logical "1" or Logical "0" State at<br>B Outputs | $V_{DD} = 5V, R_L = 1.0 \text{ k}\Omega$<br>$V_{DD} = 10V, R_L = 1.0 \text{ k}\Omega$<br>$V_{DD} = 15V, R_L = 1.0 \text{ k}\Omega$ |     | 180<br>75<br>55  | 480<br>190<br>140 | ns<br>ns<br>ns |

**AC Electrical Characteristics\***T<sub>A</sub> = 25°C, C<sub>L</sub> = 50 pF, R<sub>L</sub> = 200k, input t<sub>r</sub> = t<sub>f</sub> = 20 ns, unless otherwise specified (Continued)

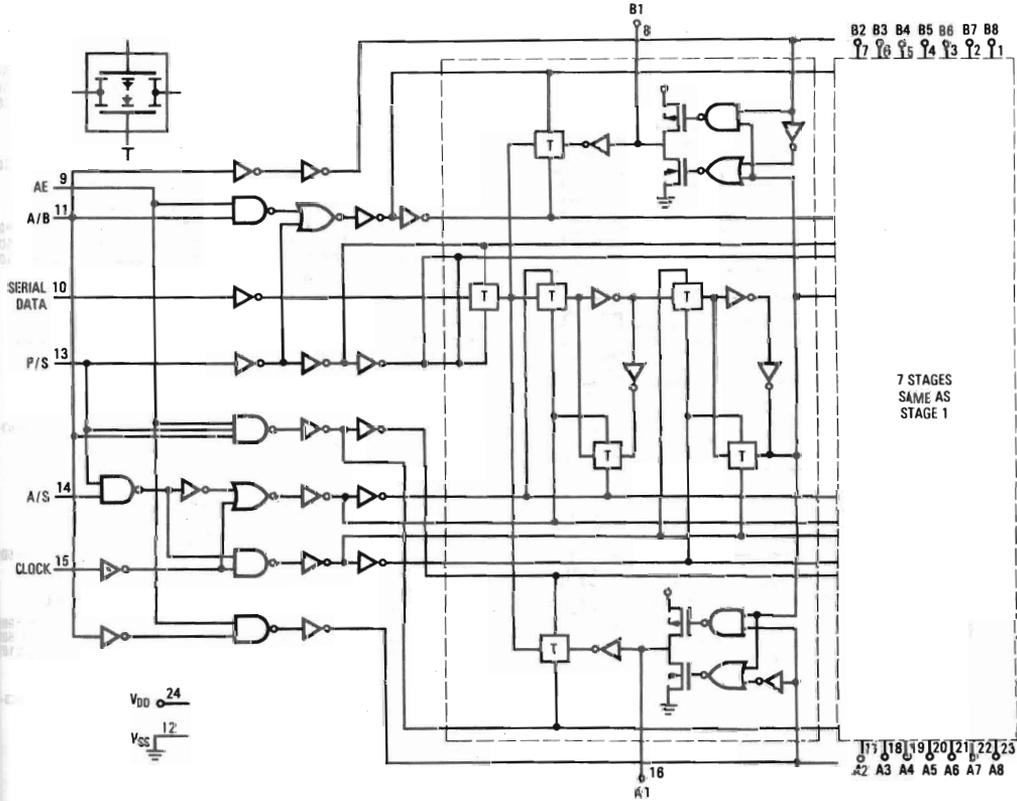
| Symbol                              | Parameter  | Conditions   | Min            | Typ             | Max              | Units             |
|-------------------------------------|--|--|----------------|-----------------|------------------|-------------------|
| t <sub>THL</sub> , t <sub>TLH</sub> | Output Transition Time                           | V <sub>DD</sub> = 5V<br>V <sub>DD</sub> = 10V<br>V <sub>DD</sub> = 15V |                | 100<br>50<br>40 | 200<br>100<br>80 | ns<br>ns<br>ns    |
| f <sub>CL</sub>                     | Maximum Clock Input Frequency                    | V <sub>DD</sub> = 5V<br>V <sub>DD</sub> = 10V<br>V <sub>DD</sub> = 15V | 2<br>5<br>7    | 4<br>10<br>14   |                  | MHz<br>MHz<br>MHz |
| t <sub>WL</sub> , t <sub>WH</sub>   | Minimum Clock Pulse Width                        | V <sub>DD</sub> = 5V<br>V <sub>DD</sub> = 10V<br>V <sub>DD</sub> = 15V |                | 125<br>50<br>35 | 250<br>100<br>70 | ns<br>ns<br>ns    |
| t <sub>RCL</sub> , t <sub>FCL</sub> | Maximum Clock Rise & Fall Time                   | V <sub>DD</sub> = 5V<br>V <sub>DD</sub> = 10V<br>V <sub>DD</sub> = 15V | 15<br>15<br>15 |                 |                  | μs<br>μs<br>μs    |
| t <sub>SU</sub>                     | Parallel (A or B) and Serial Data Setup Time     | V <sub>DD</sub> = 5V<br>V <sub>DD</sub> = 10V<br>V <sub>DD</sub> = 15V |                | 25<br>10<br>7   | 70<br>30<br>20   | ns<br>ns<br>ns    |
| t <sub>SU</sub>                     | Control Inputs AE, A/B, P/S, A/S Setup Time      | V <sub>DD</sub> = 5V<br>V <sub>DD</sub> = 10V<br>V <sub>DD</sub> = 15V |                | 110<br>35<br>60 | 280<br>100<br>60 | ns<br>ns<br>ns    |
| t <sub>WH</sub>                     | Minimum High Level AE, A/B, P/S, A/S Pulse Width | V <sub>DD</sub> = 5V<br>V <sub>DD</sub> = 10V<br>V <sub>DD</sub> = 15V |                | 160<br>70<br>40 | 400<br>160<br>90 | ns<br>ns<br>ns    |
| C <sub>IN</sub>                     | Average Input Capacitance                        | A and B Data I/O and A/B Control Input<br>Any Other Input              |                | 7<br>5          | 15<br>7.5        | pF<br>pF          |
| C <sub>PD</sub>                     | Power Dissipation Capacitance                    | (Note 4)   |                | 155             |                  | pF                |

\*AC Parameters are guaranteed by DC correlated testing.

**Note 4:** C<sub>PD</sub> determines the no-load power consumption of any CMOS device. For complete explanation see 54C/74C Family Characteristics application note AN-90.**Logic Diagram**

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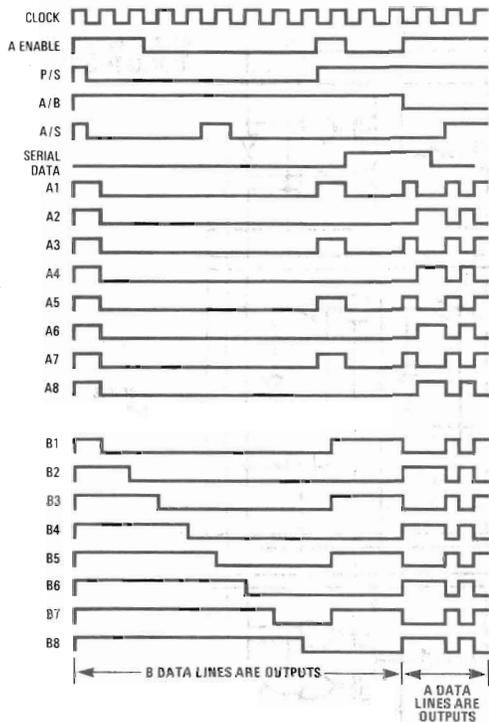
# Schematic Diagram



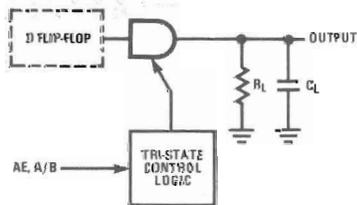
7 STAGES  
SAME AS  
STAGE 1

TL/F/5963-3

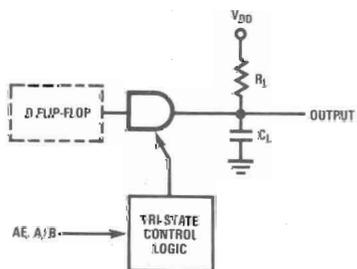
# Switching Time Waveforms and Test Circuits



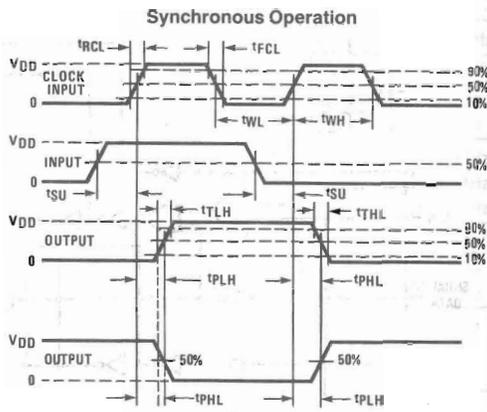
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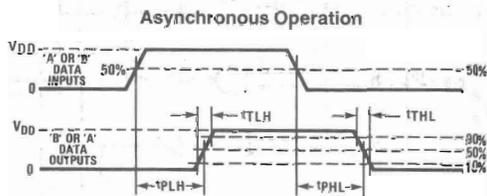


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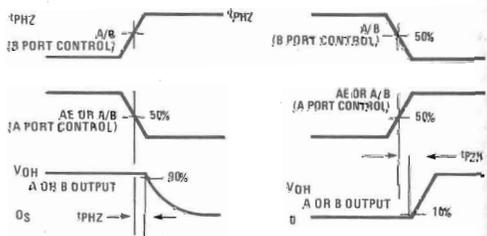


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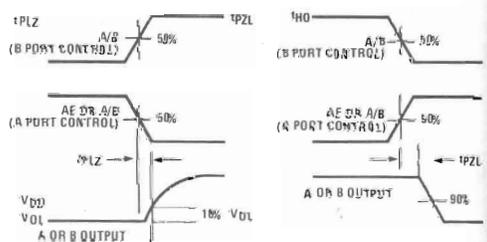
$t_r, C_L = t_f, C_L = 20 \text{ ns}$



TL/F/5963-6



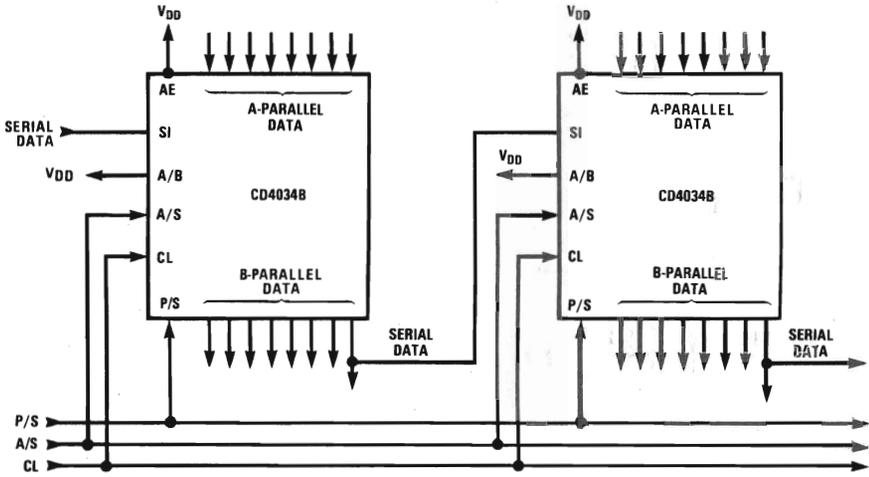
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TL/F/5963-10

# Applications

16-Bit Parallel In/Parallel Out, Parallel In/Serial Out,  
Serial In/Parallel Out, Serial In/Serial Out Register

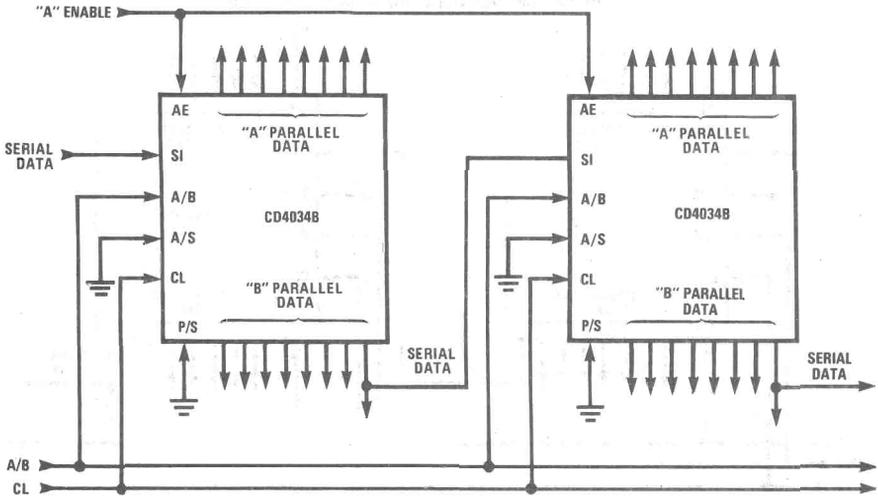


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CD4034BM/CD4034BC

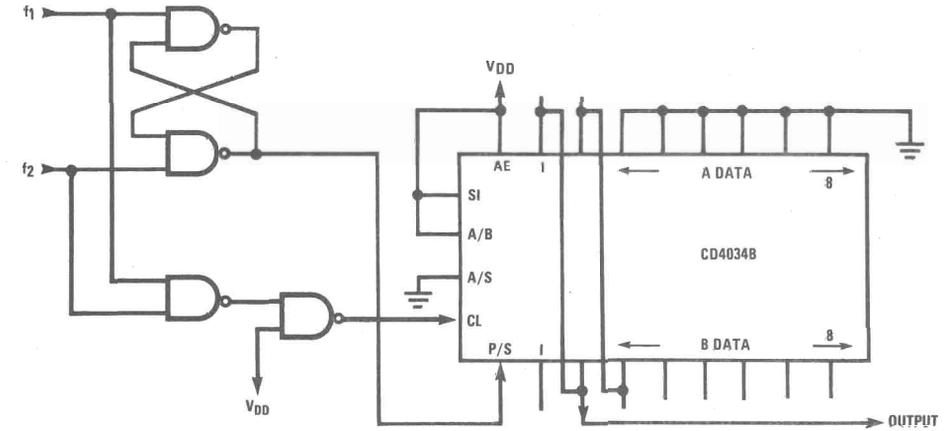
Applications (Continued)

16-Bit Serial In/Gated Parallel Out Register

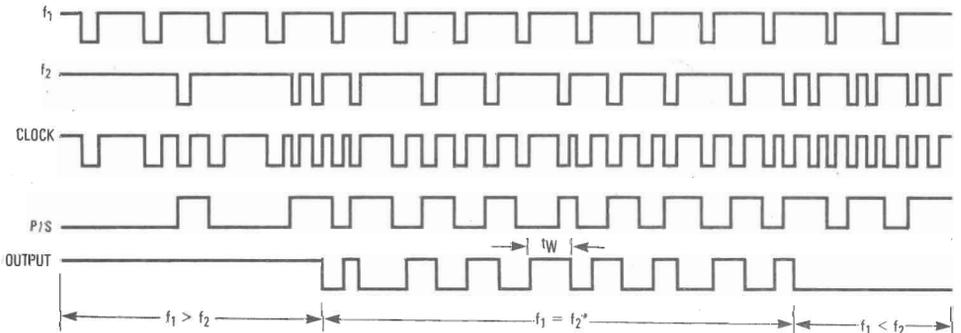


TL/F/5963-12

Frequency and Phase Comparator



TL/F/5963-13

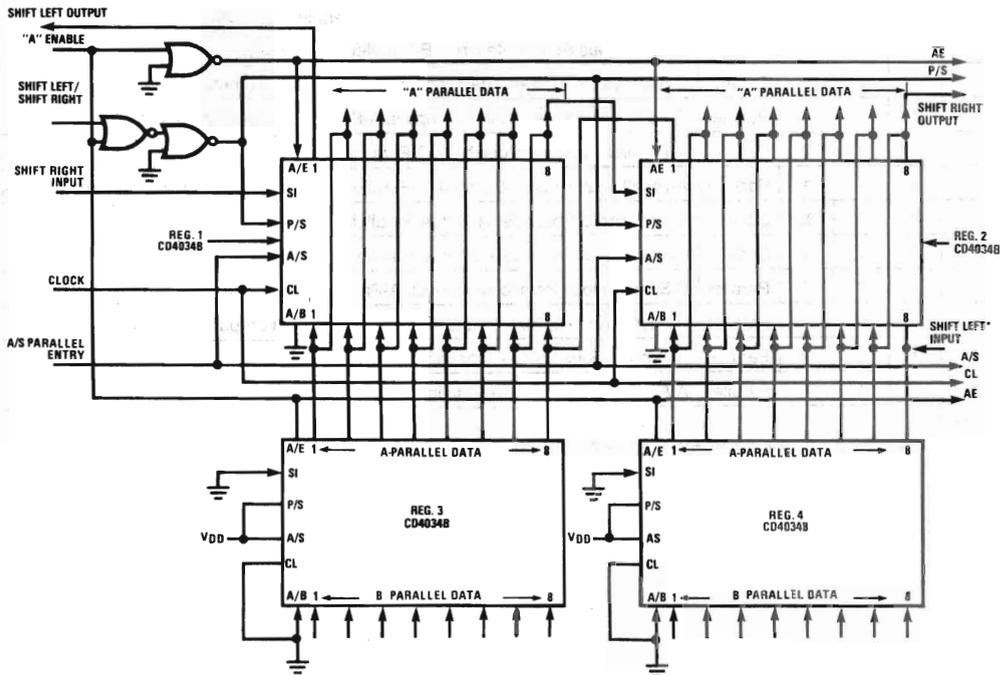


\*When  $f_1 = f_2$ ,  $t_w$  is proportional to the phase of  $f_1$  with respect to  $f_2$ .

TL/F/5963-14

Applications (Continued)

Shift Right/Shift Left with Parallel Inputs



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Shift left input must be disabled during parallel entry.

A "High" ("Low") on the Shift Left/Shift Right input allows serial data on the Shift Left Input (Shift Right Input) to enter the register on the positive transition of the clock signal. A "high" on the "A" Enable Input disables the "A" parallel data lines on Registers 1 and 2 and enables the "A" data

lines on Registers 3 and 4 and allows parallel data into Registers 1 and 2. Other logic schemes may be used in place of registers 3 and 4 for parallel loading.

When parallel inputs are not used Registers 3 and 4 and associated logic are not required.

## Truth Table

| "A" Enable | P/S | A/B | A/S | Mode     | Operation*   |
|------------|-----|-----|-----|----------|--|
| 0          | 0   | 0   | X   | Serial   | Synchronous Serial data input, A- and B-Parallel data outputs disabled.                    |
| 0          | 0   | 1   | X   | Serial   | Synchronous Serial data input, B-Parallel data output.                                     |
| 0          | 1   | 0   | 0   | Parallel | B Synchronous Parallel data inputs, A-Parallel data outputs disabled.                      |
| 0          | 1   | 0   | 1   | Parallel | B Asynchronous Parallel data inputs, A-Parallel data outputs disabled.                     |
| 0          | 1   | 1   | 0   | Parallel | A-Parallel data inputs disabled, B-Parallel data outputs, synchronous data recirculation.  |
| 0          | 1   | 1   | 1   | Parallel | A-Parallel data inputs disabled, B-Parallel data outputs, asynchronous data recirculation. |
| 1          | 0   | 0   | X   | Serial   | Synchronous Serial data input, A-Parallel data output.                                     |
| 1          | 0   | 1   | X   | Serial   | Synchronous Serial data input, B-Parallel data output.                                     |
| 1          | 1   | 0   | 0   | Parallel | B Synchronous Parallel data input, A-Parallel data output.                                 |
| 1          | 1   | 0   | 1   | Parallel | B Asynchronous Parallel data input, A-Parallel data output.                                |
| 1          | 1   | 1   | 0   | Parallel | A Synchronous Parallel data input, B-Parallel data output.                                 |
| 1          | 1   | 1   | 1   | Parallel | A Asynchronous Parallel data input, B-Parallel data output.                                |

X = Don't Care

\*For synchronous operation (serial mode or when A/S = 0 in parallel mode), outputs change state at positive transition of the clock.