



CYPRESS
SEMICONDUCTOR

CY7C168
CY7C169

4096 x 4 Static RAM

Features

- Automatic power-down when deselected (7C168)
- CMOS for optimum speed/power
- High speed
 - $t_{AA} = 25$ ns
 - $t_{ACE} = 15$ ns (7C169)
- Low active power
 - 385 mW
- Low standby power (7C168)
 - 83 mW
- TTL-compatible inputs and outputs
- Capable of withstanding greater than 2001V electrostatic discharge

Functional Description

The CY7C168 and CY7C169 are high-performance CMOS static RAMs organized as 4096 by 4 bits. Easy memory expansion is provided by an active LOW chip enable ($\overline{CE}$) and three-state drivers. The CY7C168 has an automatic power-down feature, reducing the power consumption by 77% when deselected.

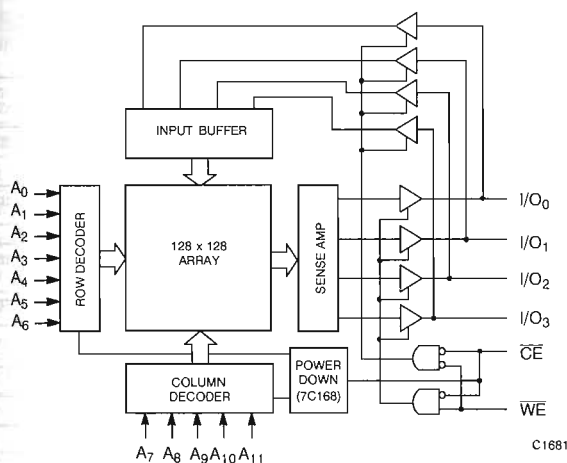
Writing to the device is accomplished when the chip select ($\overline{CE}$) and write enable ($\overline{WE}$) inputs are both LOW. Data on the four data input/output pins (I/O_0 through I/O_3) is written into the memory location specified on the address pins (A_0 through A_{11}).

Reading the device is accomplished by taking the chip enable ($\overline{CE}$) LOW while ($\overline{WE}$) remains HIGH. Under these conditions, the contents of the location specified on the address pins will appear on the four data input/output pins (I/O_0 through I/O_3).

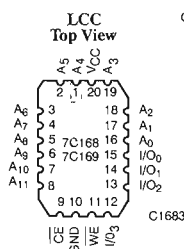
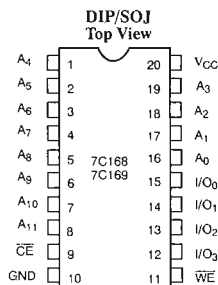
The input/output pins remain in a high-impedance state when chip enable is HIGH, or write enable ($\overline{WE}$) is LOW.

A die coat is used to insure alpha immunity.

Logic Block Diagram



Pin Configurations



Selection Guide

		7C168-25 7C169-25	7C168-35 7C169-35	7C169-40	7C168-45
Maximum Access Time (ns)		25	35	40	45
Maximum Operating Current (mA)	Commercial	90	90	70	70
	Military		90	70	70

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature	– 65°C to +150°C
Ambient Temperature with Power Applied	– 55°C to +125°C
Supply Voltage to Ground Potential (Pin 28 to Pin 14)	– 0.5V to +7.0V
DC Voltage Applied to Outputs in High Z State	– 0.5V to +7.0V
DC Input Voltage	– 3.0V to +7.0V

Output Current into Outputs (Low)	20 mA
Static Discharge Voltage (per MIL-STD-883, Method 3015)	> 2001V
Latch-Up Current	> 200 mA

Operating Range

Range	Ambient Temperature	V _{CC}
Commercial	0°C to +70°C	5V ± 10%
Military ^[1]	– 55°C to +125°C	5V ± 10%

Electrical Characteristics Over the Operating Range^[2]

Parameters	Description	Test Conditions	7C168–25 7C169–25		7C168–35 7C169–35		7C168–45 7C169–245		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
V _{OH}	Output High Voltage	V _{CC} = Min., I _{OH} = –4.0 mA	2.4		2.4		2.4		V
V _{OL}	Output Low Voltage	V _{CC} = Min., I _{OL} = 8.0 mA		0.4		0.4		0.4	V
V _{IH}	Input High Voltage		2.0	V _{CC}	2.0	V _{CC}	2.0	V _{CC}	V
V _{IL}	Input Low Voltage		–3.0	0.8	–3.0	0.8	–3.0	0.8	V
I _{LX}	Input Load Current	GND ≤ V _I ≤ V _{CC}	–10	10	–10	10	–10	10	μA
I _{OZ}	Output Leakage Current	GND ≤ V _O ≤ V _{CC} , Output Disabled	–50	50	–50	50	–50	50	μA
I _{OS}	Output Short Circuit Current ^[3]	V _{CC} = Max., V _{OUT} = GND		–350		–350		–350	mA
I _{CC}	V _{CC} Operating Supply Current	V _{CC} = Max., I _{OUT} = 0 mA	Com'l	90		70		70	mA
			Mil			90		70	
I _{SB1}	Automatic CE Power-Down Current	Max. V _{CC} , CE ≥ V _{IH}	Com'l	20		20		15	mA
			Mil			20		20	
I _{SB2}	Automatic CE Power-Down Current	Max. V _{CC} , CE ≥ V _{CC} – 0.3 V	Com'l	11		11		11	mA
			Mil			20		20	

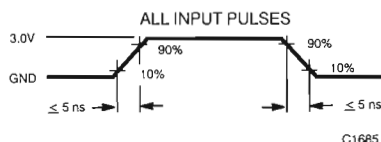
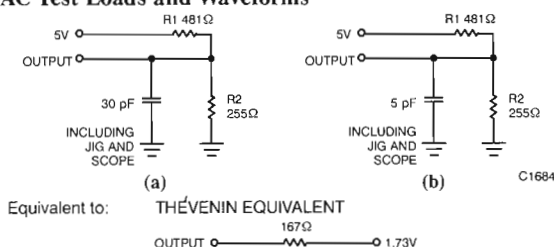
Capacitance^[4]

Parameters	Description	Test Conditions	Max.	Units
C _{IN}	Input Capacitance	T _A = 25°C, f = 1 MHz, V _{CC} = 5.0V	10	pF
C _{OUT}	Output Capacitance		10	pF

Notes:

1. T_A is the "instant on" case temperature.
2. See the last page of this specification for Group A subgroup testing information.
3. Not more than 1 output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.
4. Tested initially and after any design or process changes that may affect these parameters.

AC Test Loads and Waveforms



Switching Characteristics Over the Operating Range^[2,5]

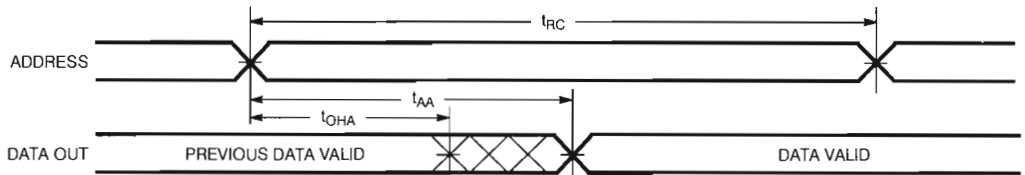
Timing Characteristics Over the Operating Range										
Parameters	Description	7C168-25 7C169-25		7C168-35 7C169-35		7C169-40		7C168-45		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE										
t _{RC}	Read Cycle Time	25		35		40		45		ns
t _{AA}	Address to Data Valid		25		35		40		45	ns
t _{OHA}	Output Hold from Address Change	3		3		3		3		ns
t _{ACE}	CE LOW to Data Valid	7C168	25		35				45	ns
		7C169	15		25		25			ns
t _{LZCE}	CE LOW to Low Z ^[6]	5		5		5		5		ns
t _{HZCE}	CE HIGH to High Z ^[6,7]		15		20		20		25	ns
t _{PU}	CE LOW to Power-Up(7C168)	0		0		0		0		ns
t _{PD}	CE HIGH to Power-Down(7C168)		25		25				30	ns
t _{RCS}	Read Command Set-Up	0		0		0		0		ns
t _{RCH}	Read Command Hold	0		0		0		0		ns
WRITE CYCLE^[8]										
t _{WC}	Write Cycle Time	25		35		40		40		ns
t _{SCE}	CE LOW to Write End	25		30		30		35		ns
t _{AW}	Address Set-Up to Write End	20		30		40		35		ns
t _{HA}	Address Hold from Write End	0		0		0		0		ns
t _{SA}	Address Set-Up to Write Start	0		0		0		0		ns
t _{PWE}	WE Pulse Width	20		30		35		35		ns
t _{SD}	Data Set-Up to Write End	10		15		15		15		ns
t _{HD}	Data Hold from Write End	0		0		3		3		ns
t _{LZWE}	WE HIGH to Low Z ^[6]	6		6		6		6		ns
t _{HZWE}	WE LOW to High Z ^[6,7]		10		15		20		20	ns

Notes:

- Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
- At any given temperature and voltage condition, t_{HZ} is less than t_{LZ} for any given device.
- t_{HZCE} and t_{HZWE} are tested with C_L = 5 pF as in part (b) of AC Test Loads. Transition is measured ±500 mV from steady state voltage.
- The internal write time of the memory is defined by the overlap of CE LOW and WE LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.

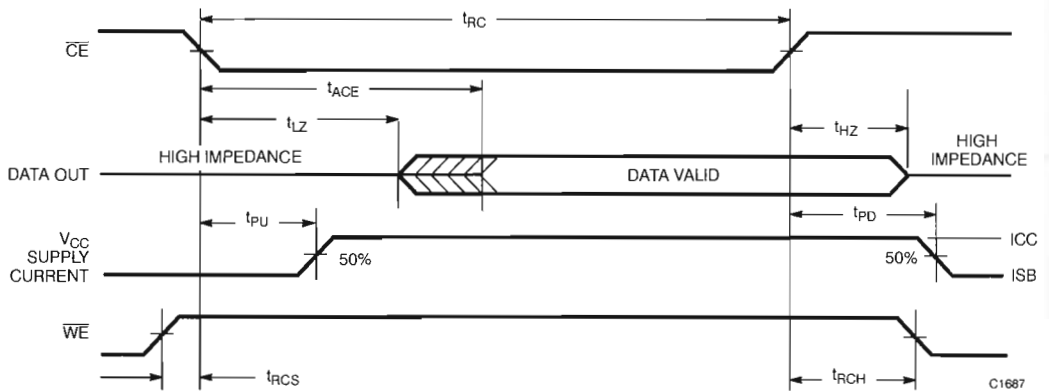
Switching Waveforms

Read Cycle No. 1^[9, 10]



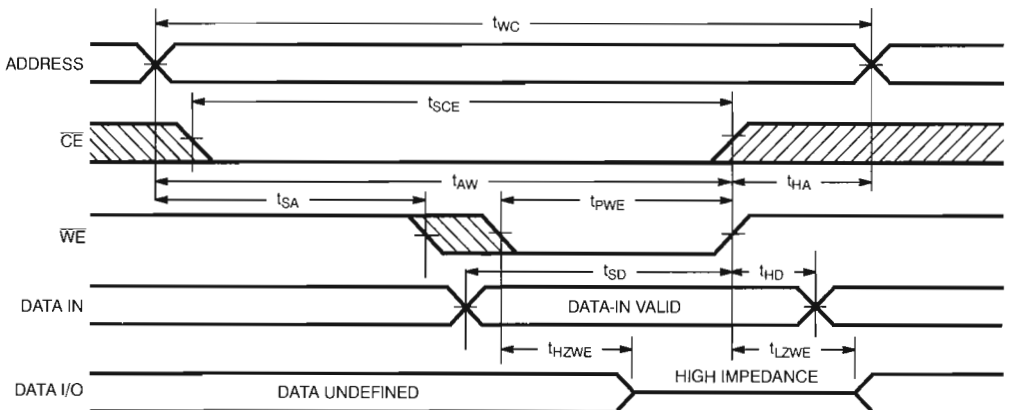
C1686

Read Cycle^[9, 11]



C1687

Write Cycle No. 1 ($\overline{WE}$ Controlled)^[8]



C1688

Notes:

9. $\overline{WE}$ is high for read cycle.

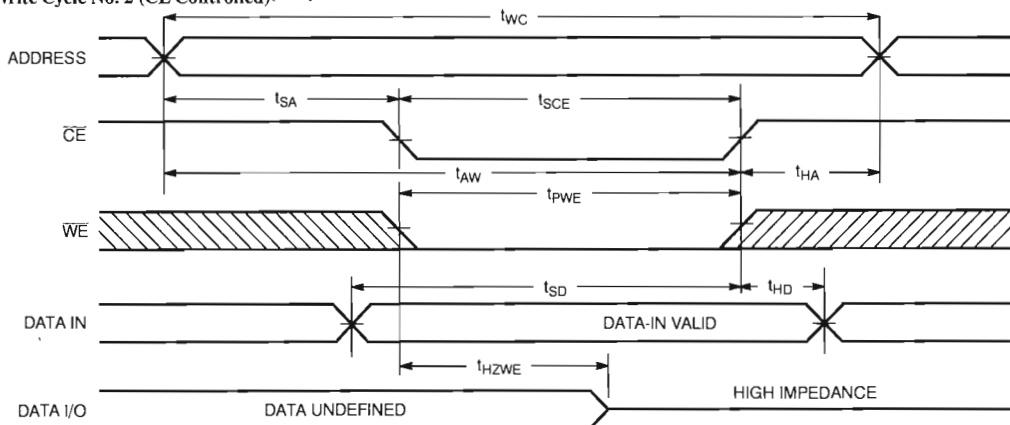
10. Device is continuously selected, $\overline{CE} = V_{IL}$.

11. Address valid prior to or coincident with $\overline{CE}$ transition low.

12. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ HIGH, the output remains in a high-impedance state.

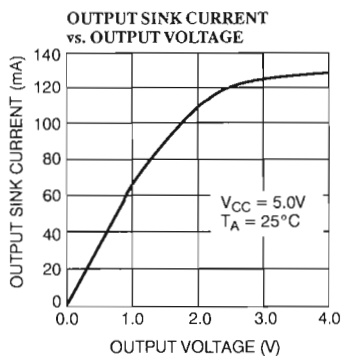
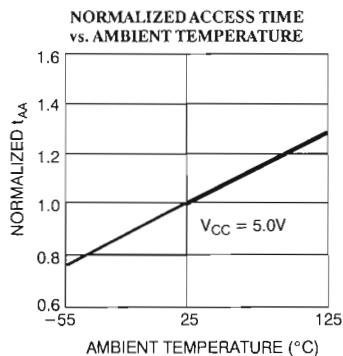
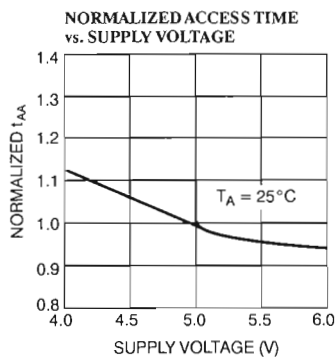
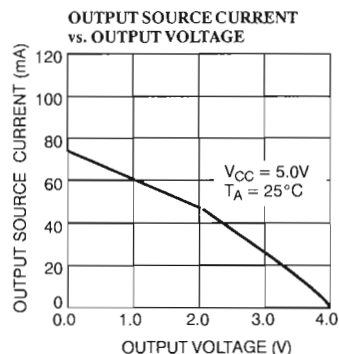
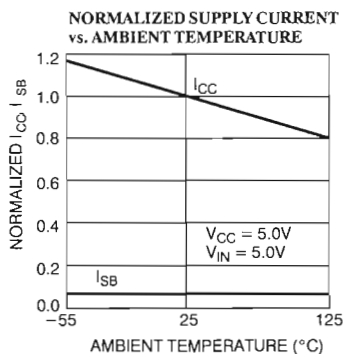
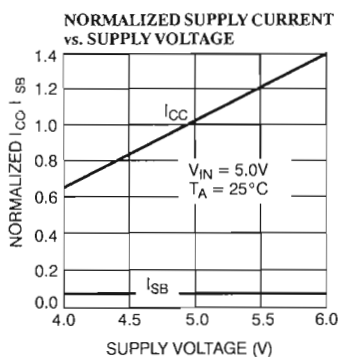
Switching Waveforms (continued)

Write Cycle No. 2 ($\overline{CE}$ Controlled)^[8, 12]

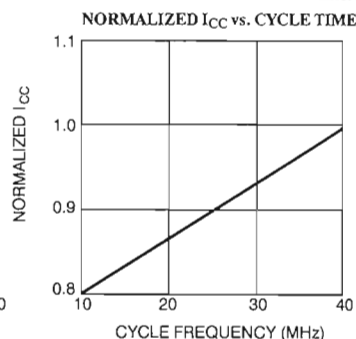
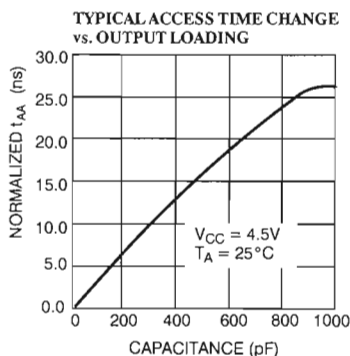
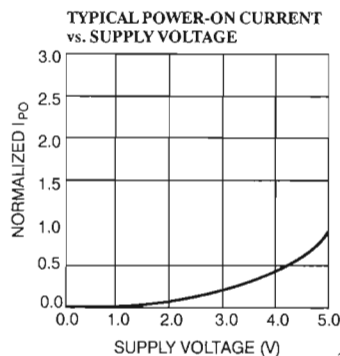


C1689

Typical DC and AC Characteristics



Typical DC and AC Characteristics (continued)



Ordering Information

Speed (ns)	I_{CC} (mA)	Ordering Code	Package Type	Operating Range
25	90	CY7C168-25PC	P5	Commercial
		CY7C168-25DC	D6	
		CY7C168-25LC	L51	
		CY7C168-25VC	V5	
35	90	CY7C168-35PC	P5	Commercial
		CY7C168-35DC	D6	
		CY7C168-35LC	L51	
		CY7C168-35VC	V5	
		CY7C168-35DMB	D6	Military
		CY7C168-35LMB	L51	
45	70	CY7C168-45PC	P5	Commercial
		CY7C168-45DC	D6	
		CY7C168-45LC	L51	
		CY7C168-45VC	V5	
		CY7C168-45DMB	D6	Military
		CY7C168-45LMB	L51	

Speed (ns)	I_{CC} (mA)	Ordering Code	Package Type	Operating Range
25	90	CY7C169-25PC	P5	Commercial
		CY7C169-25DC	D6	
		CY7C169-25LC	L51	
		CY7C169-25VC	V5	
35	90	CY7C169-35PC	P5	Commercial
		CY7C169-35DC	D6	
		CY7C169-35LC	L51	
		CY7C169-35VC	V5	
		CY7C169-35DMB	D6	Military
		CY7C169-35LMB	L51	
40	70	CY7C169-40PC	P5	Commercial
		CY7C169-40DC	D6	
		CY7C169-40LC	L51	
		CY7C169-40VC	V5	
		CY7C169-40DMB	D6	Military
		CY7C169-40LMB	L51	

MILITARY SPECIFICATIONS
Group A Subgroup Testing
DC Characteristics

Parameters	Subgroups
V_{OH}	1,2,3
V_{OL}	1,2,3
V_{IH}	1,2,3
V_{IL} Max.	1,2,3
I_{IX}	1,2,3
I_{OZ}	1,2,3
I_{CC}	1,2,3
$I_{SB1}^{[13]}$	1,2,3
$I_{SB2}^{[13]}$	1,2,3

Notes:

13. 7C168 only.

Switching Characteristics

Parameters	Subgroups
READ CYCLE	
t_{RC}	7,8,9,10,11
t_{AA}	7,8,9,10,11
t_{OHA}	7,8,9,10,11
t_{ACE}	7,8,9,10,11
t_{RCS}	7,8,9,10,11
t_{RCH}	7,8,9,10,11
WRITE CYCLE	
t_{WC}	7,8,9,10,11
t_{SCE}	7,8,9,10,11
t_{AW}	7,8,9,10,11
t_{HA}	7,8,9,10,11
t_{SA}	7,8,9,10,11
t_{PWE}	7,8,9,10,11
t_{SD}	7,8,9,10,11
t_{HD}	7,8,9,10,11

Document #: 38-00034-D