

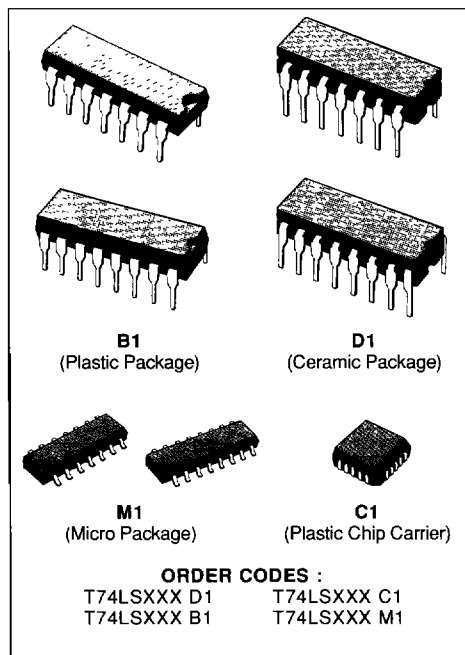
DUAL DECADE COUNTER DUAL 4-STAGE BINARY COUNTER

- DUAL VERSION OF LS290 AND 293
- LS390 HAS SEPARATE CLOCKS ALLOWING +2, +2.5, +5
- INDIVIDUAL ASYNCHRONOUS CLEAR FOR EACH COUNTER
- TYPICAL MAX COUNT FREQUENCY OF 50 MHz
- INPUT CLAMP DIODES MINIMIZE HIGH SPEED TERMINATION EFFECTS

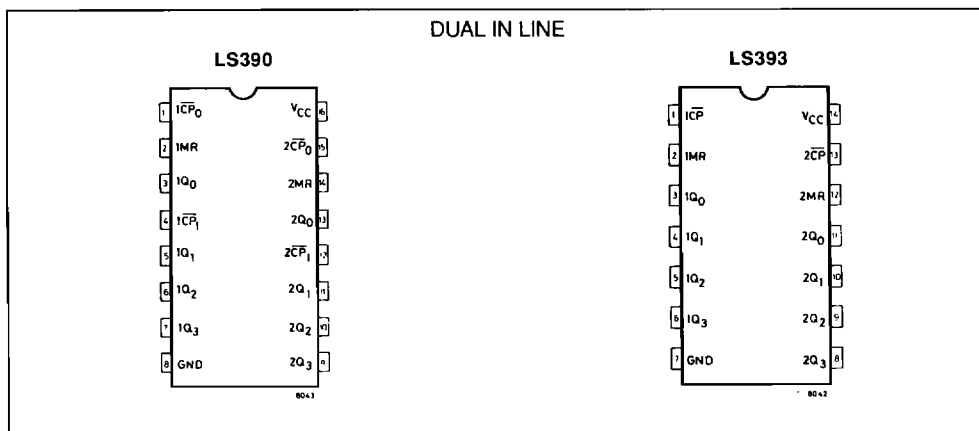
DESCRIPTION

The T74LS390 and T74LS393 each contain a pair of high-speed 4-stage ripple counters. Each half of the LS390 is partitioned into a divide-by-two section and a divide-by-five section, with a separate clock input for each section. The two sections can be connected to count in the 8.4.2.1 BCD code or they can count in a biquinary sequence to provide a square wave (50 % duty cycle) at the final output.

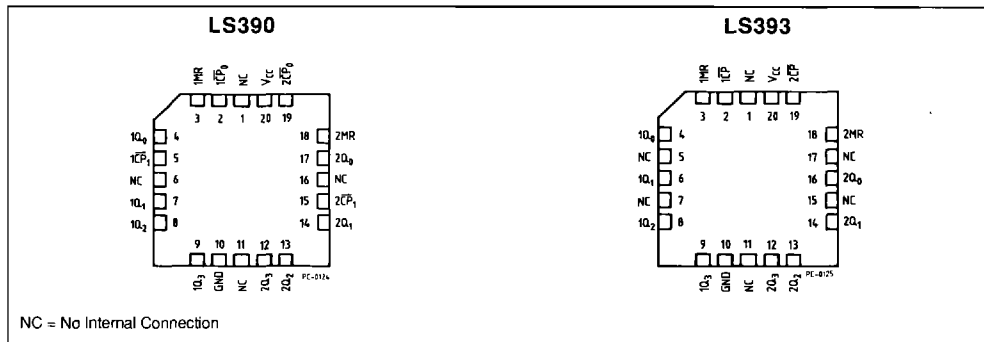
Each half of the LS393 operates as a Modulo-16 binary divider, with the last three stages triggered in a ripple fashion. In both the LS390 and the LS393, the flip-flops are triggered by a HIGH-to-LOW transition of their CP inputs. Each circuit type has a Master Reset input which responds to a HIGH signal by forcing all four outputs to the LOW state.



PIN CONNECTION (top view)



CHIP CARRIER



PIN NAMES

\overline{CP}	CLOCK ACTIVE LOW GOING EDGE INPUT TO - 16 (LS393)
\overline{CP}_0	CLOCK ACTIVE LOW GOING EDGE INPUT TO - 2 (LS390)
\overline{CP}_1	CLOCK ACTIVE LOW GOING EDGE INPUT TO - 5 (LS390)
MR	MASTER RESET (active HIGH) INPUT
Q_0-Q_3	FLIP-FLOPS OUTPUTS

TRUTH TABLES

LS390 BCD (Input on \overline{CP}_0 ; Q_0 \overline{CP}_1)					LS390 $\div 5$ (Input on \overline{CP}_1)				LS393				
COUNT	OUTPUTS				COUNT	OUTPUTS			COUNT	OUTPUTS			
	Q_3	Q_2	Q_1	Q_0		Q_3	Q_2	Q_1		Q_3	Q_2	Q_1	Q_0
0	L	L	L	L	0	L	L	L	0	L	L	L	L
1	L	L	L	H	1	L	L	H	1	L	L	L	H
2	L	L	H	L	2	L	H	L	2	L	L	H	L
3	L	L	H	H	3	L	H	H	3	L	L	H	H
4	L	H	L	L	4	H	L	L	4	L	H	L	L
5	L	H	L	H					5	L	H	L	H
6	L	H	H	L					6	L	H	H	L
7	L	H	H	H					7	L	H	H	H
8	H	L	L	L					8	H	L	L	L
9	H	L	L	H					9	H	L	L	H
									10	H	L	H	L
									11	H	L	H	H
									12	H	H	L	L
									13	H	H	L	H
									14	H	H	H	L
									15	H	H	H	H

H = HIGH Voltage Level
L = LOW Voltage Level

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	- 0.5 to 7	V
V_I	Input Voltage, Applied to Input	- 0.5 to 15	V
V_O	Output Voltage, Applied to Output	- 0.5 to 10	V
I_I	Input Current, into Inputs	- 30 to 5	mA
I_O	Output Current, into Outputs	50	mA

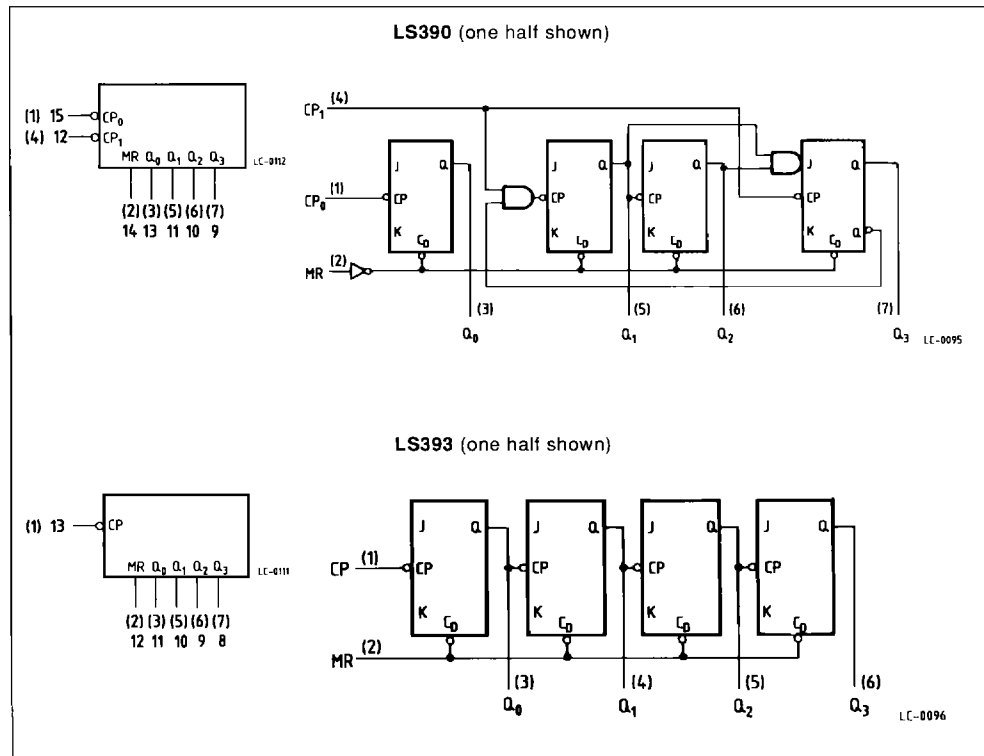
Stresses in excess of those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions in excess of those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

GUARANTEED OPERATING RANGE

Part Numbers	Supply Voltage			Temperature
	Min.	Typ.	Max.	
T74LS390XX	4.75 V	5.0 V	5.25 V	0 °C to + 70 °C

XX = package type.

LOGIC SYMBOLS AND LOGIC DIAGRAMS



FUNCTIONAL DESCRIPTION

Each half of the LS393 Operates in the Modulo 16 binary sequences, as indicated in the $\div 16$ Truth Table. The first flip-flop is triggered by HIGH-to-LOW transitions of the CP input signal. Each of the other flip-flops is triggered by a HIGH-to-LOW transition of the Q output of the preceding flip-flop. Thus state changes of the Q outputs for not occur simultaneously. This means that logic signals derived from combinations of these outputs will be subject to decoding spikes and, therefore, should not be used as clocks for other counters, registers or flip-flops. A HIGH signal on MR forces all outputs to the LOW state and prevents counting.

Each half of the LS390 contains a $\div 5$ section that is independent except for the common MR function.

The $\div 5$ section operates in 4.2.1 binary sequence, as shown in the $\div 5$ Truth Table, with the third stage output exhibiting a 20 % duty cycle when the input frequency is constant. To obtain a $\div 10$ function having a 50 % duty cycle output, connect the input signal to CP₁ and connect Q₃ output to the CP₀ input ; the Q₀ output provides the 50 % duty cycle output. If the input frequency is connected to CP₀ and the Q₀ output is connected to CP₁, a decade divider operating in the 8.4.2.1 BCD code is obtained, as show in the BCD Truth Table. Since the flip-flops change state asynchronously, logic signal derived from combinations of LS390 outputs are also subject to decoding spikes. A HIGH signal on MR forces all outputs LOW and prevents counting.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

Symbol	Parameter		Limits			Test Condition (note 1)	Unit	
			Min.	Typ. (*)	Max.			
V _{IH}	Input HIGH Voltage		2.0			Guaranteed Input HIGH Voltage for All Inputs	V	
V _{IL}	Input LOW Voltage				0.8	Guaranteed Input LOW Voltage for All Inputs	V	
V _{CD}	Input Clamp Diode Voltage			- 0.65	- 1.5	V _{CC} = MIN, I _{IN} = -18 mA	V	
V _{OH}	Output HIGH Voltage		2.7	3.4		V _{CC} = MIN, I _{OH} = - 400 μ A V _{IN} = V _{IH} or V _{IL} per Truth Table	V	
V _{OL}	Output LOW Voltage			0.25	0.4	I _{OL} = 4.0 mA	V _{CC} = MIN, V _{IN} = V _{IH} or V _{IL} per Truth Table	V
				0.35	0.5	I _{OL} = 8.0 mA		V
I _{IH}	Input HIGH Current	CP ₀ , CP ₁ MR			40 80 20	V _{CC} = MAX, V _{IN} = 2.7 V	μ A	
		CP ₀ , CP ₁ MR			400 800 100	V _{CC} = MAX, V _{IN} = 7.0 V	μ A	
I _{IL}	Input LOW Current	CP ₀ , CP ₁ MR			- 2.4 - 3.2 - 0.4	V _{CC} = MAX, V _{IN} = 0.4 V	mA	
I _{OS}	Output Short Circuit Current (note 2)		- 20		- 120	V _{CC} = MAX, V _{OUT} = 0 V	mA	
I _{CC}	Power Supply Current	LS290		20	30	V _{CC} = MAX	mA	
		LS293		20	30		mA	

- Notes : 1. For conditions shown as MIN or MAX, use the appropriate value specified under guaranteed operating conditions for the device type.
2. Not more than one output should be shorted at a time.
(*) Typical values are at V_{CC} = 5.0 V, T_A = 25 C.

AC CHARACTERISTICS : $T_A = 25\text{ }^\circ\text{C}$, $V_{CC} = 5.0\text{ V}$

Symbol	Parameter	Limits			Test Conditions	Unit
		Min.	Typ.	Max.		
f_{MAX}	Maximum Clock Frequency CP ₀ to Q ₀	25	35		C _L = 15 pF	MHz
f_{MAX}	Maximum Clock Frequency CP ₁ to Q ₁	12.5	20			MHz
t_{PLH} t_{PHL}	Propagation Delay, CP to Q ₀ LS393		12 13	20 20		ns
t_{PLH} t_{PHL}	CP ₀ to Q ₀ LS390		12 13	20 20		ns
t_{PLH} t_{PHL}	CP to Q ₃ LS393		40 40	60 60		ns
t_{PLH} t_{PHL}	CP ₀ to Q ₂ LS390		37 39	60 60		ns
t_{PLH} t_{PHL}	CP ₁ to Q ₁ LS390		13 14	21 21		ns
t_{PLH} t_{PHL}	CP ₁ to Q ₂ LS390		24 26	39 39		ns
t_{PLH} t_{PHL}	CP ₁ to Q ₃ LS390		13 14	21 21		ns
t_{PHL}	MR to any Input LS390/393		24	39		ns

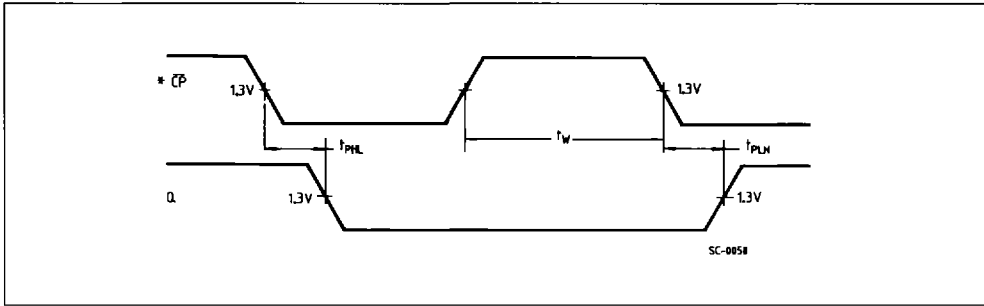
AC SET-UP REQUIREMENTS : $T_A = 25\text{ }^\circ\text{C}$

Symbol	Parameter	Limits			Test Conditions	Unit
		Min.	Typ.	Max.		
t_w	clock pulse width LS390	20			V _{CC} = 5.0 V	ns
t_w	CP ₀ Pulse Width LS390	20				ns
t_w	CP ₁ Pulse Width LS390	40				ns
t_w	MR Pulse Width LS390/393	20				ns
t_{rec}	Recovery Time LS390/393	25				ns

RECOVERY TIME (t_{rec}) - is defined as the minimum time required between the end of the reset pulse and the clock transition from HIGH to LOW in order to recognized and transfer HIGH Data to the Q outputs.

AC WAVEFORMS

Figure 1.



* The number of Clock Pulses required between the t_{PHL} and t_{PLH} measurements can be determined from the appropriate Truth Table.

Figure 2.

