256 Bit	Commercial Industrial	X2444 X2444I	16 x 16 Bit

Nonvolatile Static RAM

FEATURES

- **Low Cost 8-Pin Mini-Dip**
- **Ideal for use with Single Chip Microcomputers**
  - **— Static Timing**
  - **— Minimum I/O Interface**
  - **— Serial Port Compatible (COPS™, 8051)**
  - **— Easily Interfaces to Microcontroller Ports**
  - **— Minimum Support Circuits**
- **Software and Hardware Control of Nonvolatile Functions**
  - **— Maximum Store Protection**
- **TTL Compatible**
- **16 x 16 Organization**
- **Low Power Dissipation**
  - **— Active Current: 15mA Typ.**
  - **— Store Current: 8mA Typ.**
  - **— Standby Current: 6mA Typ.**
  - **— Sleep Current: 5mA Typ.**

DESCRIPTION

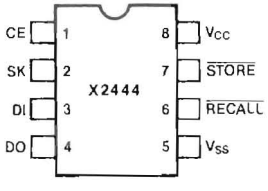
The Xicor X2444 is a serial 256 bit NOVRAM* featuring a static RAM configured 16 x 16, overlaid bit for bit with a nonvolatile E^2PROM array. The X2444 is fabricated with the same reliable N-channel floating gate MOS technology used in all Xicor 5 volt nonvolatile memories.

The Xicor NOVRAM design allows data to be transferred between the two memory arrays by means of software commands or external hardware inputs. A store operation (RAM data to E^2PROM) is completed in 10ms or less and a recall operation (E^2PROM data to RAM) is completed in 2.5μs or less.

Xicor NOVRAMs are designed for unlimited write operations to RAM, either from the host or recalls from E^2PROM and a minimum 100,000 store operations. Data retention is specified to be greater than 100 years.

*NOVRAM is Xicor's nonvolatile static RAM device.
COPS™ is a trademark of National Semiconductor Corp.

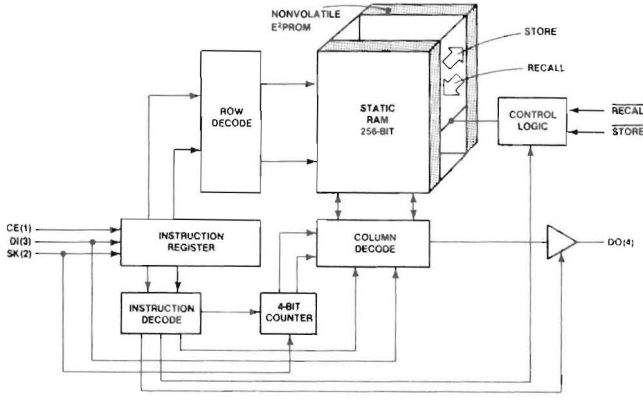
PIN CONFIGURATION



PIN NAMES

CE	Chip Enable
SK	Serial Clock
DI	Serial Data In
DO	Serial Data Out
$\overline{\text{RECALL}}$	Recall
$\overline{\text{STORE}}$	Store
V_{CC}	+5V
V_{SS}	Ground

FUNCTIONAL DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias X2444 ..... −10°C to +85°C
X2444I ..... −65°C to +135°C
Storage Temperature ..... −65°C to +150°C
Voltage on any Pin with
Respect to Ground ..... −1.0V to +7V
D.C. Output Current ..... 5 mA
Lead Temperature (Soldering,
10 Seconds) ..... 300°C

*COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. OPERATING CHARACTERISTICS

X2444 T_A = 0°C to +70°C, V_{CC} = +5V ±5%, unless otherwise specified.
X2444I T_A = −40°C to +85°C, V_{CC} = +5V ±10%, unless otherwise specified.

Symbol	Parameter	X2444 Limits		X2444I Limits		Units	Conditions
		Min.	Max.	Min.	Max.		
I_{CC}	Power Supply Current		15		25	mA	All Inputs=V_{CC}, $I_{I/O}$= 0 mA
I_{SL}	Sleep Current		7		10	mA	
I_{SB}	Standby Current		10		15	mA	CE=V_{IL}
I_{STO}	Store Current		12		15	mA	
I_{LI}	Input Load Current		10		10	µA	V_{IN} = V_{CC}
I_{LO}	Output Leakage Current		10		10	µA	V_{OUT} = V_{CC}
V_{IL}	Input Low Voltage	−1.0	0.8	−1.0	0.8	V	
V_{IH}	Input High Voltage	2.0	V_{CC} +0.5	2.0	V_{CC} +1.0	V	
V_{OL}	Output Low Voltage		0.4		0.4	V	I_{OL} = 2.4 mA
V_{OH}	Output High Voltage	2.4		2.4		V	I_{OH} = −0.8 mA

CAPACITANCE T_A = 25°C, f = 1.0 MHz, V_{CC} = 5V

Symbol	Test	Max.	Unit	Conditions
$C_{I/O}$[1]	Input/Output Capacitance	8	pF	$V_{I/O}$ = 0V
C_{IN}[1]	Input Capacitance	6	pF	V_{IN} = 0V

Note: (1) This parameter is periodically sampled and not 100% tested.

A.C. CONDITIONS OF TEST

Input Pulse Levels	0 to 3.0 Volts
Input Rise and Fall Times	10 nsec
Input and Output Timing Levels	1.5 Volts
Output Load	1 TTL Gate and C_L = 100 pF

NONVOLATILE OPERATIONS

Operation	$\overline{\text{STORE}}$	$\overline{\text{RECALL}}$	INST	WRITE ENABLE LATCH	Previous RECALL
Hardware Recall	1	0	NOP(2)	X	X
Software Recall	1	1	RCL	X	X
Hardware Store	0	1	NOP(2)	SET	True
Software Store	1	1	STO	SET	True

Note: (2) NOP designates when the X2444 is not currently executing an instruction.

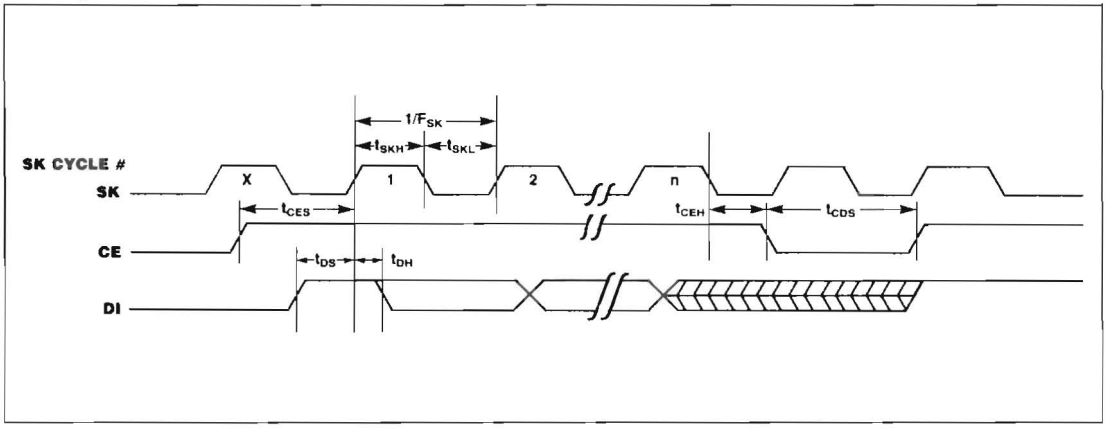
A.C. CHARACTERISTICS

X2444 T_A = 0°C to +70°C, V_{CC} = +5V ±5%, unless otherwise specified.
X2444I T_A = −40°C to +85°C, V_{CC} = +5V ±10%, unless otherwise specified.

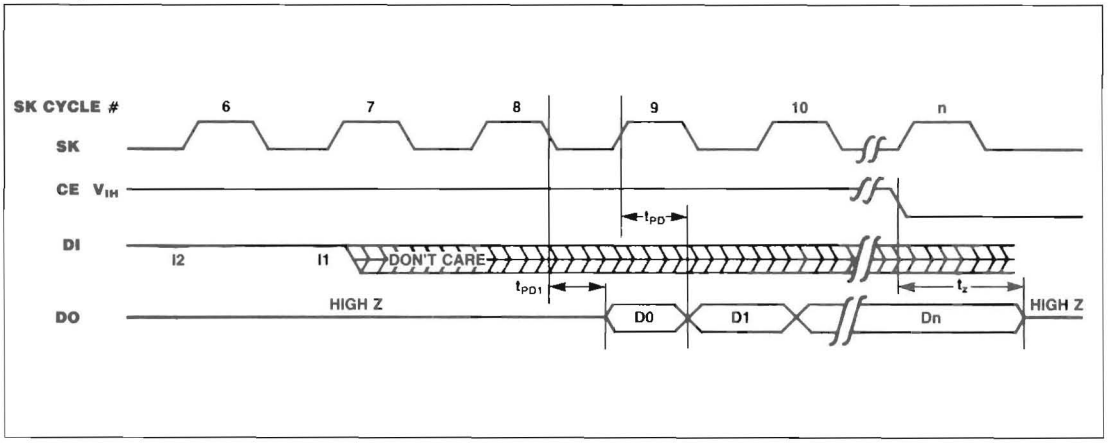
Read and Write Cycle Limits

Symbol	Parameter	Min.	Max.	Units
F_{SK}	SK Frequency		1.0	MHz
t_{SKH}	SK Positive Pulse Width	0.4		µs
t_{SKL}	SK Negative Pulse Width	0.4		µs
t_{DS}	Data Setup Time	0.4		µs
t_{DH}	Data Hold Time	0.08		µs
t_{PD1}	SK ↓ to Data 0 Valid		375	ns
t_{PD}	SK ↑ to Data Valid		375	ns
t_Z	Chip Enable to Output High Z		1.0	µs
t_{CES}	Chip Enable Setup	0.8		µs
t_{CEH}	Chip Enable Hold	0.4		µs
t_{CDS}	Chip De-select	0.8		µs

Write Cycle



Read Cycle

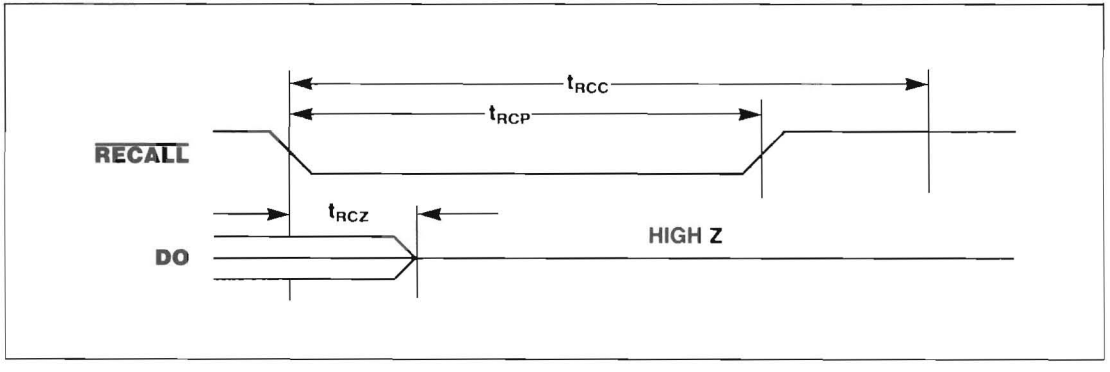


Array Recall Cycle Limits

Symbol	Parameter	Min.	Max.	Units
t_{RCC}	Recall Cycle Time	2.5		µs
t_{RCP}	Recall Pulse Width(3)	1.0		µs
t_{RCZ}	Recall to Output High Z		0.5	µs

Note: (3) Recall rise time must be <10µs.

Recall Cycle



Store Cycle Limits

Symbol	Parameter	Min.	Typ.(4)	Max.	Units
t_{ST}	Store Time		5	10	ms
t_{STP}	Store Pulse Width	0.2			µs
t_{STZ}	Store To Output High Z			1.0	µs
V_{CC}	Store Inhibit		3		V

Note: (4) Typical values are for T_A=25°C and nominal supply voltage.

Hardware Store

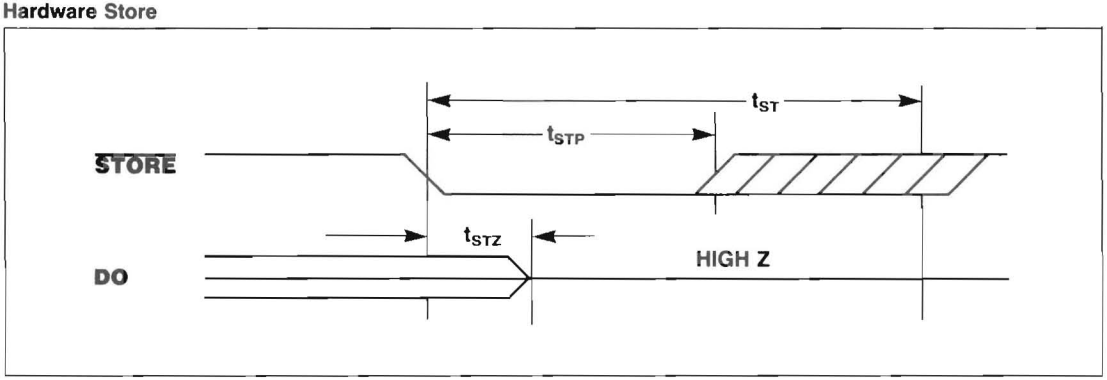


Figure 1: RAM Read

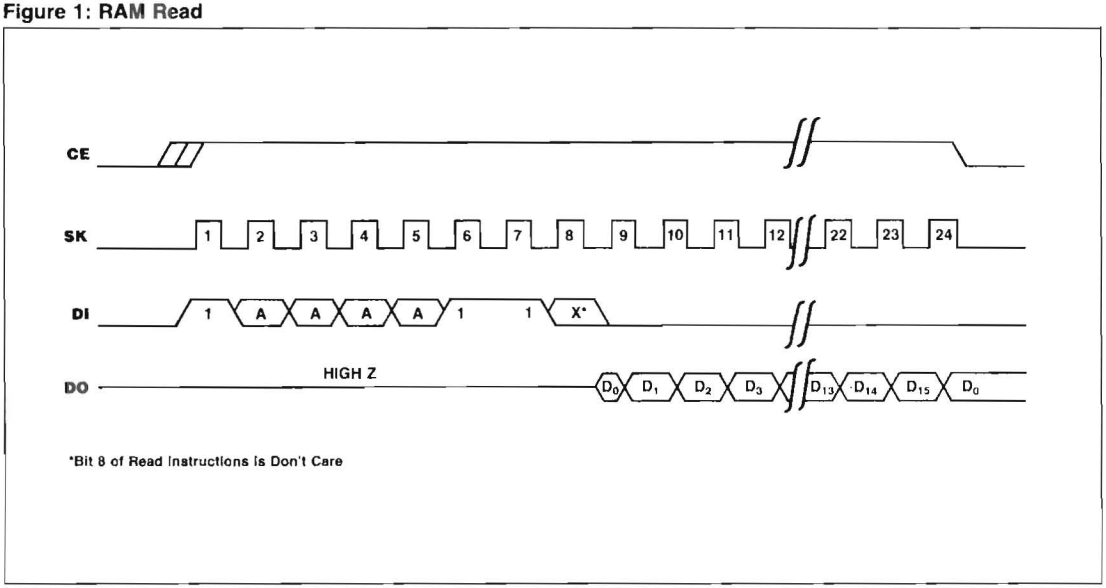


Figure 2: RAM Write

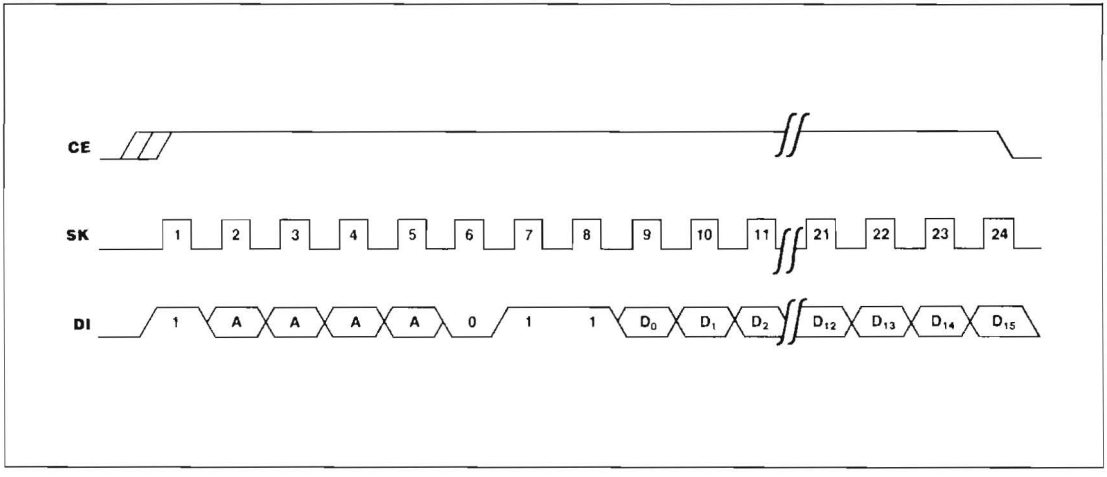


Figure 3: Non-Data Operations

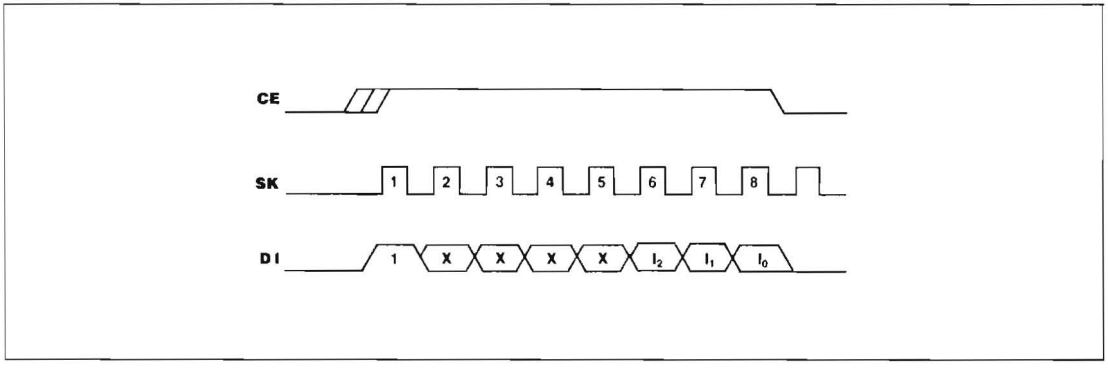


TABLE 1: INSTRUCTION SET

Instruction	Format, I_2 I_1 I_0	Operation
WRDS (Figure 3)	1XXXX000	Reset Write Enable Latch (Disables writes and stores)
STO (Figure 3)	1XXXX001	Store RAM data in E^2PROM
SLEEP (Figure 3)	1XXXX010	Enter SLEEP Mode
WRITE (Figure 2)	1AAAA011	Write Data into RAM Address AAAA
WREN (Figure 3)	1XXXX100	Set Write Enable Latch (Enables writes and stores)
RCL (Figure 3)	1XXXX101	Recall E^2PROM Data into RAM
READ (Figure 1)	1AAAA11X	Read Data from RAM Address AAAA

X=Don't Care
A=Address Bit

PIN DESCRIPTIONS

Chip Enable (CE)

The Chip Enable input must be HIGH to enable all read/write operations. CE LOW resets the instruction register and places the X2444 in the standby low power mode.

Serial Clock (SK)

The Serial Clock input is used to clock all data into and out of the device.

Data In (DI)

Data In is the serial data input.

Data Out (DO)

Data Out is the serial data output. It is in the high impedance state except during data output cycles in response to a READ instruction.

$\overline{\text{STORE}}$

$\overline{\text{STORE}}$ LOW will initiate an internal transfer of data from RAM to E^2PROM.

$\overline{\text{RECALL}}$

$\overline{\text{RECALL}}$ LOW will initiate an internal transfer of data from E^2PROM to RAM.

DEVICE OPERATION

The X2444 contains an 8-bit instruction register. It is accessed via the DI input, with data being clocked in on the rising edge of SK. CE must be HIGH during the entire data transfer operation.

Table 1 contains a list of the instructions and their operation codes. The most significant bit (MSB) of all instructions is a one, bits 6 through 3 are either RAM address (A) or don't care (X) and bits 2 through 0 are the operation codes. The X2444 requires the instruction to be shifted in with the MSB first.

After CE is HIGH, the X2444 will not begin to interpret the data stream until a one has been shifted in on DI. Therefore, CE may be brought HIGH with SK running and DI LOW. DI must then go HIGH to indicate the start condition of an instruction before the X2444 will begin any action.

In addition, the SK clock is totally static. The user can completely stop the clock and data shifting will be stopped. Restarting the clock will resume shifting of data.

WRDS and WREN

Internally the X2444 contains a "write enable" latch. This latch must be set for either writes to the RAM or store operations to the E^2PROM. The WREN instruction sets the latch and the WRDS instruction resets the latch, disabling *both* RAM writes and E^2PROM stores. The write enable latch is automatically reset on power-up.

SLEEP

The SLEEP instruction removes power from the RAM, placing the X2444 in a very low power quiescent state. Data in the RAM is lost once a SLEEP instruction is issued; however, data from the last store operation is retained in the E^2PROM. The sleep mode can be exited by either a software or hardware recall operation.

RCL and $\overline{\text{RECALL}}$

Either the RCL instruction or a LOW on the $\overline{\text{RECALL}}$ input will initiate a transfer of E^2PROM data into RAM. A recall operation must be performed after a power-up before any store or RAM write operation can be enabled. This recall operation and the recall recovery from the sleep mode guarantees a known state of data in RAM. Both recall operations set an internal "previous recall" latch which must be set to enable any write or store operations.

STO and $\overline{\text{STORE}}$

Either the STO instruction or a LOW on the $\overline{\text{STORE}}$ input will initiate the transfer of data from RAM to E^2PROM. In order to safeguard against unwanted store operations, the following conditions must be true:

1. STO instruction issued or $\overline{\text{STORE}}$ input is LOW;
2. The internal write enable latch must be set (WREN instruction issued);
3. The "previous recall" latch must be set.

Once the store cycle is initiated, all other device functions are inhibited. Upon completion of the store cycle, the write enable latch is reset.

WRITE

The write instruction contains the 4 bit address of the word to be written. The write instruction is immediately followed by the 16-bit word to be written. CE must remain HIGH during the entire operation. If CE is brought LOW prematurely (after the instruction but before 16 bits of data are transferred), the instruction register will be reset and the data that was shifted in will be written to RAM. If CE is kept HIGH for more than 24 SK clock cycles (8-bit instruction plus 16-bit data) the data already shifted in will be overwritten.

READ

The read instruction contains the 4 bit address of the word to be accessed. Unlike the other six instructions, I_0 is a "don't care" for the read instruction. This provides two advantages. In a design that ties both DI and DO together, the absence of an eighth bit in the instruction allows the host time to convert an I/O line from an output to an input. Secondly, it allows for valid data output during the ninth SK clock cycle.

D0, the first bit output during a read operation, is truncated. That is, it is internally clocked by the falling edge of the eighth SK clock; whereas, all succeeding bits are clocked by the rising edge of SK (refer to Read Cycle Diagram).

WRITE PROTECTION

The X2444 provides four hardware and software write protection mechanisms to prevent inadvertent stores of unknown data.

Power-down Condition

(when "write enable" latch and "previous recall" latch are not in the reset state):

- V_{CC} Sense—All functions are inhibited when V_{CC} is ≤3v, typically.
- Write Inhibit—Holding either $\overline{\text{RECALL}}$ LOW, CE LOW or $\overline{\text{STORE}}$ HIGH during power-down will prevent an inadvertent store.

Power-up Condition

- Write Enable Latch—Upon power-up the "write enable" latch is in the reset state, disabling any store operation.

Unknown Data Store

- Previous Recall Latch—The "previous recall" latch must be reset after power-up and after exiting the sleep mode. It may be reset only by performing a recall operation, which assures that data in all RAM locations is valid.

LOW POWER MODES

The X2444 provides two power conservation modes. When CE is LOW, non-critical internal devices are powered-down, placing the device in the standby power mode. Entering the sleep mode removes power from the entire RAM array, placing the device in a very low power quiescent state (sleep mode).

ENDURANCE

The endurance specification of a device is characterized by the predicted *first* bit failure to occur in the entire memory (device or system) array rather than the average or *typical* value for the array. Since endurance is limited by the number of electrons trapped in the oxide by data changes, Xicor NOVRAMs are designed to minimize the number of changes an E^2PROM bit cell undergoes during store operations. Only those bits in the E^2PROM that are different from their corresponding location in RAM will be "cycled" during a nonvolatile store. This characteristic reduces unnecessary cycling of any of the rest of the bits in the array, thereby increasing the potential endurance of each bit and increasing the potential endurance of the entire array. Reliability data documented in RR504, the *Xicor Reliability Report on Endurance*, and additional reports are available from Xicor.

Part Number	Store Cycles	Data Changes Per Bit
X2444	100,000	1,000
X2444/10	100,000	10,000