UNIVERSAL PCM-IR-REMOTE CONTROL RECEIVER

Technology: N-MOS, Si-gate

Features:

- o High interference rejection through dual transmission frequencies and several built-in checks within the received words
- o High information transmission rate through low-consumption pulse-code-modulated (PCM) transmission bursts with no word repetition
- o Serial data output for easy interface with microcomputer

Case:

8 pin dual inline plastic

Absolute maximum ratings

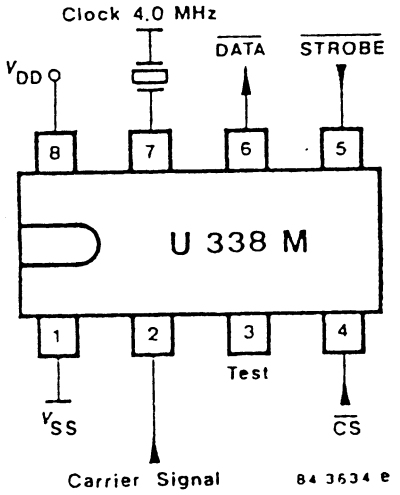
Referred to V_{SS}=ground, 0V, pin 1

Supply voltage	Pin 8	V_{DDmax}	15	V
Voltage at the other pins	Pin 2-7	V_N	$-0.3/+V_{DDmax}$	V
Output current	Pin 6	I_0	5	mA
Ambient temperature V_S = 13.2 V		T_{amb}	0 ... + 85	°C
Storage temperature		T_{stg}	-25 ... + 125	°C
Total power dissipation T_{amb} = 85 °C		P_{tot}	400	mW
Junction temperature		T_j	125	°C

Maximum thermal resistance

Junction ambient	R_{thJA}	97	K/W

Pin connection



Description

This N-MOS receiver module demodulates the command words given out by the transmitter U 327 M (IR-transmission) and from them produces the input data (12-bit serial) for a down-stream microcomputer. The serial interface allows the direct connection of the receiver to the I/O ports of microcomputers. An on-chip Ready-FF signal synchronises the orderly data flow between IR-input and $\overline{\text{DATA}}$-output.

Connections:

Pin 1 V_{SS}, ground 0 V

Pin 2 Carrier-signal input

A command word consists of 13 sequentially arranged segments of the carrier frequency F_1 = 34.64 kHz, F_2 = 37.31 kHz, or of defined pauses. The content of the command word has 13 bits and is pulse-coded, an F_1-segment representing a logic "L" and an F_2-segment a logic "H". The length of an F_1-segment at the beginning of the word and immediately after within-word transmission pauses is 13 pulses, and within the word and directly linked with an F_2-segment, 12 pulses. Correspondingly, an F_2-segment consists of 9 or 8 pulses.

Successive bits of the same value are suppressed at the transmitter and are completed by the receiver. The radiated word ends with the 13th bit, a check-bit, representing the complement of the data bit transmitted immediately before it. Frequency measurement is carrier out by pulse counting within precisely defined time-windows. A count of 10 or 6 periods identifies F_1 or F_2 respectively.

The rejection of interference from the input signal is ensured by the following criteria:

- Frequencies of the word segments
- Length of the word segments
- Sequential order of the word segment
- Position of the segments within the word (Raster)
- Position and contents of the checkbit
- Word length and a minimum following interval free from received signal of 4.3 ms.

Interference during the signal-free minimum interval prevents the the Ready-FF from being set. Thereby the last IR-command is not passed on to the MC.

Pin 3 Test (Line)

The module is switched to the Test-mode by taking $\overline{CS}$ and $\overline{STROBE}$ to a potential of typically 10 V. The circuit remains in the Test mode as long as $\overline{CS}$ is held at 10 V. Depending on an internal counter, which is counted on by pulses at the $\overline{STROBE}$ input, either various data from the frequency-recognition circuit is given out at Pin 3, or data must be input at Pin 3, to test out the word recognition (see table 1, diagram a).

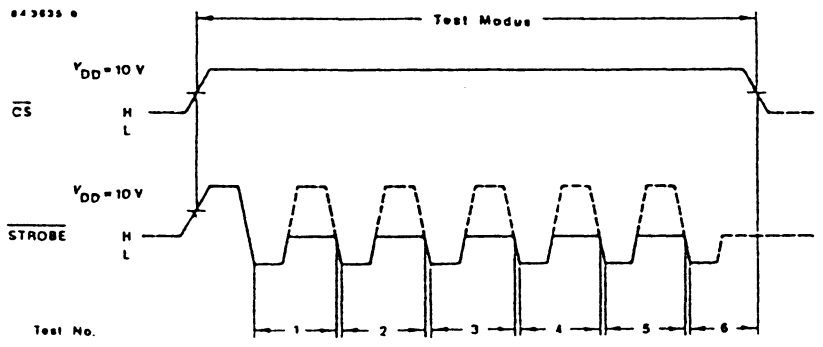
Table 1:

	INPUT		OUTPUT	
Test-No.	Function	Pin	Function	Pin
1	Frequency	2	F_1-single recognition (measurement of double period)	3
2	Frequency	2	F_2-single recognition (measurement of double period)	3
3	Frequency	2	F_1-multiple (bit) recognition (5 x F_1-single recognition)	3
4	Frequency	2	F_2-multiple (bit) recognition (3 x F_2-single recognition)	3
5	F_1-bit	3	Command word	
6	F_2-bit	3	Check of error-recognition	6

In the normal operation state, Pin 3 delivers a static line signal (active LOW) in order to switch downstream system components from Stand-by to operating state. Commands and addresses, for which the line-flip-flop is set or reset, can be randomly selected (mask-programmed). 4 terminal lines are available for the selection of addresses or address ranges. The same is true for choice of commands or command-groups.

In the basic version of the U 338 M, lines from the command groups $\overline{3+4}$ under address 1 were selected for setting the line flip-flop LOW. Resetting is likewise achieved by command 4 under address 1 (see layout in the tables for address- and command-lines).

Diagram a



Pin 4 $\overline{CS}$

The $\overline{DATA}$-output remains high-resistance for as long as $\overline{CS}$ is HIGH. When the microprocessor delivers a chip-select (active LOW), the Ready signal is first switched to the $\overline{DATA}$-output line. When Ready is set (LOW), a complete word is ready to be fetched (see diagram c).

The trailing edge of $\overline{CS}$ resets the Ready-FF (whether the $\overline{STROBE}$ was presented or not), so that the receiver is ready to accept the next IR-command. If a set-pulse for the Ready-FF arises while $\overline{CS}$ is active, this set-pulse is temporarily stored and the setting of the ready flip-flop is delayed until $\overline{CS}$ goes HIGH again (see diagram b).

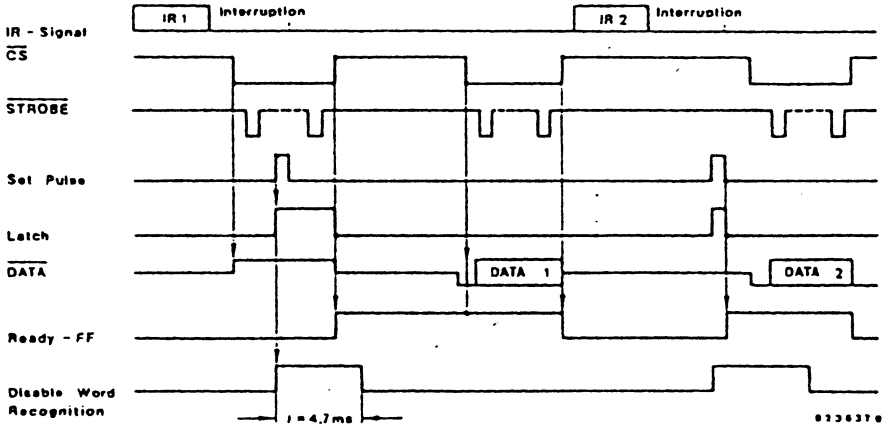
This ensures that a word coming in during the period of time when the electronics is switched off ($\overline{CS}$ = LOW) is not last. The delay is in force for a least 4.3 ms, after which the Ready-FF or the buffer store can be reset by a newly-arriving bit, irrespective of whether $\overline{CS}$ is HIGH or LOW.

Pin 5 $\overline{STROBE}$

If $\overline{CS}$ is active and Ready is set, a complete data word (12 bit) can be ready by 12 STROBES (see diagram c). If $\overline{CS}$ is active but Ready-FF not set, $\overline{STROBE}$-pulses do not prevent the formation of a new word (see diagram b).

If no new word is read, $\overline{STROBE}$ should be kept high.

Diagram b



Pin 6 $\overline{DATA}$

The switching on of $\overline{CS}$ first puts the Ready signal to the data output. With the first STROBE, data bit A appears, and with the twelvth STROBE address-bit A1 (diagram c, table 2). As long as there is an output, no command is accepted.

If there is no $\overline{CS}$ after receipt of a word, the data word and the Ready signal are retained for a least 4.3 ms, but only however until the receipt of a new word. The Ready-FF can be reset by a newly captured bit, at the earliest, after the elapse of this 4.3 ms period.

Diagram c

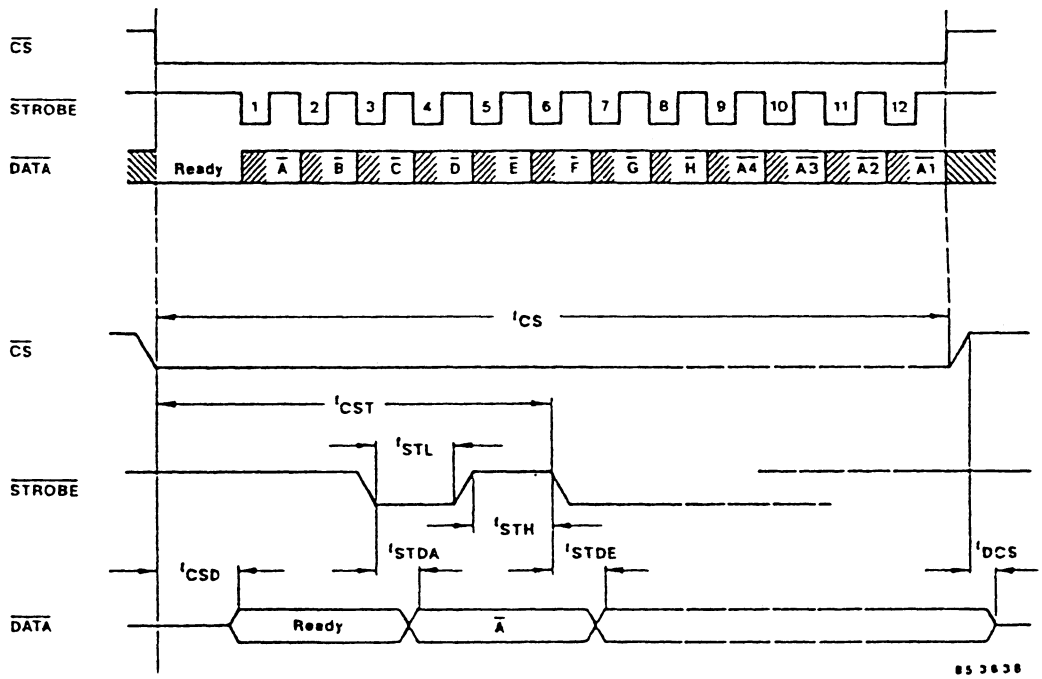


Table 2:

Coding of the data output $\overline{DATA}$:

a: Command Section

Data output F	E	D	C	B	A	Command-No.* (transmitter)	
L	L	L	L	L	L	0	
			L	L	H	1	
			L	H	L	2	
			L	H	H	3	
			H	L	L	4	**
			H	L	H	5	
			H	H	L	6	
			H	H	H	7	
L	L	H	L	L	L	8	
			L	L	H	9	
			L	H	L	10	
			L	H	H	11	
			H	L	L	12	
			H	L	H	13	
			H	H	L	14	
			H	H	H	15	
L	H	L	L	L	L	16	
			L	L	H	17	
			L	H	L	18	
			L	H	H	19	***
			H	L	L	20	
			H	L	H	21	
			H	H	L	22	
			H	H	H	23	
L	H	H	L	L	L	24	
			L	L	H	25	
			L	H	L	26	
			L	H	H	27	***
			H	L	L	28	
			H	L	H	29	
			H	H	L	30	
			H	H	H	31	

Data output F	E	D	C	B	A	Command-No.* (transmitter)
H	L	L	L	L	L	32
			L	L	H	33
			L	H	L	34
			L	H	H	35
			H	L	L	36
			H	L	H	37
			H	H	L	38
			H	H	H	39
H	L	H	L	L	L	40
			L	L	H	41
			L	H	L	42
			L	H	H	43
			H	L	L	44
			H	L	H	45
			H	H	L	46
			H	H	H	47
H	H	L	L	L	L	48
			L	L	H	49
			L	H	L	50
			L	H	H	51
			H	L	L	52
			H	L	H	53
			H	H	L	54
			H	H	H	55
H	H	H	L	L	L	56
			L	L	H	57
			L	H	L	58
			L	H	H	59
			H	L	L	60
			H	L	H	61
			H	H	L	62
			H	H	H	63

* Tne transmitter U 327 M radiates only commands No. 0 ... 39
** Command No. 4 under address 1: Line OUT (HIGH)
*** Command No. 16 - 28 under address 1: Line IN (LOW)

b: Address Section and Bits G, H

Address-No.	Data output A1	A2	A3	A4	H	G
1	H	L	L	L	H	L
2	H	L	L	H	H	L
3	H	L	H	L	H	L
4	H	L	H	H	H	L
5	L	H	L	L	L	H
6	L	H	L	H	L	H
7	L	H	H	L	L	H
8	L	H	H	H	L	H
9	H	H	L	H	X	X
10	H	H	H	L	X	X
11	L	L	L	H	X	X
12	L	L	H	L	X	X
13	H	H	H	H	X	X
14	H	H	L	L	X	X
15	L	L	L	L	X	X
16	L	L	H	H	X	X

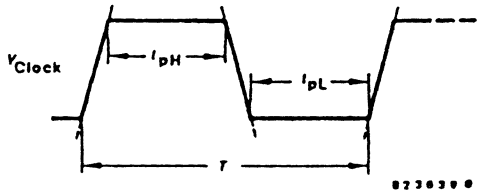
The transmitter U 327 M sends only commands under the addresses 1 ... 8. Bits G, H are determined at the transmitter end in accordance with the above table, and can be evaluated as extra check-bits. In the case of transmitter U 328 M, for the addresses 9 ... 16 bits G and H are identical with bits A2, A1.

Pin 7 Clock 4.000 MHz

Input for direct connection to a 4.000 MHz quartz crystal or for an external 4.000 MHz clock signal capacitatively coupled via C_{ext}, e.g. 0.1 nF (see diagram d). The clock-input handles a non-amplitude-modulated sine-wave, square wave or saw-tooth.

Diagram d

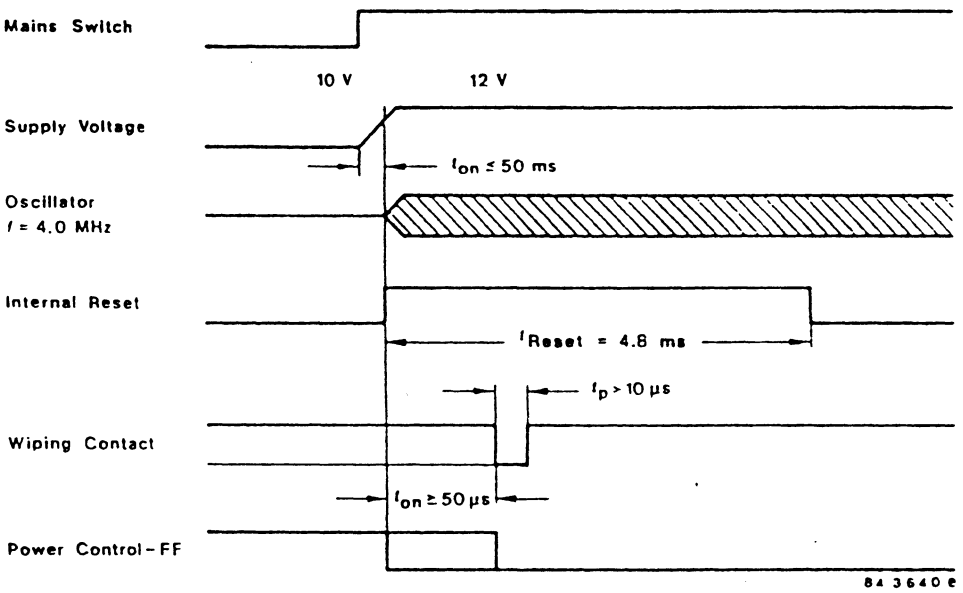
For external clock supply



Pin 8 Voltage supply V_{DD} = 12 V ± 10 %

When power is applied an internal reset-signal brings the circuit to the initial condition. Simultaneously false data is prevented from appearing at the outputs. The voltage and time conditions are clear from diagram e.

Diagram e



Electrical characteristics

Operating conditions: V_{DD} = 10.8 ... 13.2 V,
f_{cl} = 4.000 MHz, T_{amb} = 0... - 85 °C,
unless otherwise specified

		Min.	Typ.	Max.	
Pin 8 (V_{DD})					
Supply current					
V_{DD}= 13.2 V, T_{amb} = 25 °C	I_{DD}		22	40	mA
T_{amb} = 0 °C	I_{DD}			46	mA
T_{amb} = 85 °C	I_{DD}			30	mA
Pin 7 (4.000 MHz)					
Clock frequency	f_0			4.000	MHz
Clock times	t_{PH}	60			ns
	t_{PL}	60			ns
External capacitive load to ground (quartz drive)	C_M	10[+]		30	pF
Internal load	C_L			20	pF
Input leakage current V_I = 13.2 V	I_{IR}			20	µA
External clock drive (capacitive coupling)	V_{clock}	2.0		6.0	V_{pp}
direct coupling	V_{IL}			1.0	V
	V_{IH}	8.0			V
Synchron of transmitter- and receiver-clock frequencies	$G = \frac{1 + \frac{\Delta f_{0(transm.)}}{f_{0(transm.)}}}{1 + \frac{\Delta f_{0(recvr.)}}{f_{0(recvr.)}}}$	0.9995	1	1.005	

[+]) If the power-on rise time ≦ 3 ms, only.

		Min.	Typ.	Max.	
Pin 2 (IR-Signal)					
Internal capacity-coupled signal sensitivity					
Input voltage					
28.8 kHz ≦ f ≦ 43.2 kHz	V_i	0.5	0.7	1.1	V_{pp}
28.8 kHz ≧ f ≧ 43.2 kHz	V_i	0.6	0.8	1.2	V_{pp}
Input signal compatibility	V_i			V_{DD}	V_{pp}
Input leakage current V_I = 13.2 V	I_{IR}			20	µA
Pin 4,5 ($\overline{CS}$, $\overline{STROBE}$)					
Input voltages					
Normal operation:					
H-level	V_{IH}	3.2		6.5	V
L-level	V_{IL}			0.8	V
Test-mode:					
active	V_{IT}	V_{DDmin}		V_{DD}	V
Input leakage current V_I = 13.2 V	I_{IR}			10	µA
Pin 6 ($\overline{DATA}$)					
active:					
I_{QL} = 2.0 mA	V_{QL}			0.4	V
V_{QH} = 2.4 V	$-I_{QH}$	100			µA
I_{QH} = 20 µA	V_{QH}	3.5		7.0	V
I_{QH} = 200 µA	V_{QH}			5.8	V
inactive:					
V_Q = 13.2 V	I_{QR}			20	µA

		Min.	Typ.	Max.	
Pin 3 (Test, Line) (Open drain)					
Test mode:					
Input					
H-level	V_{IH}	V_{DDmin}			V
L-level	V_{IL}			0.8	V
Output					
I_{QL} = 2.0 mA	V_{QL}			0.8	V
V_Q = 13.2 V	I_{QR}			20	µA
Normal operation:					
Input with wiping contact					
Reset Line V_{IH} = 4.0 V	I^+			50	mA
Set Line V_{IL} = 0.8 V	I^+			100	µA
Output					
I_{QL} = 2.0 mA	V_{QL}			0.8	V
V_Q = 13.2 V	I_{QR}			20	µA
I^+ = Changeover current for t ≦ 10 µs					
Times Pin 4, 5, 6 ($\overline{CS}$, $\overline{STROBE}$, $\overline{DATA}$)					
C_L = 100 pF	t_{CSD}		1.5	2.5	µs
	t_{STL}	1		100	µs
	t_{STH}	1			µs
	t_{STDA}		1.5	2.5	µs
	t_{DCS}			2	µs
	t_{STDE}	0			µs
	t_{CS}	2			µs
	t_{CST}			400	µs

The times refer to an L-level of 0.8 V ($\overline{CS}$, $\overline{STROBE}$), or 0.4 V ($\overline{DATA}$) and an H-level of 3.2 V ($\overline{CS}$, $\overline{STROBE}$), or 2.4 V ($\overline{DATA}$).