

SN54166, SN54LS166A, SN74166, SN74LS166A PARALLEL-LOAD 8-BIT SHIFT REGISTERS

OCTOBER 1976 — REVISED MARCH 1988

- Synchronous Load
- Direct Overriding Clear
- Parallel to Serial Conversion

TYPE	TYPICAL MAXIMUM CLOCK FREQUENCY	TYPICAL POWER DISSIPATION
'166	35 MHz	360 mW
'LS166A	35 MHz	100 mW

description

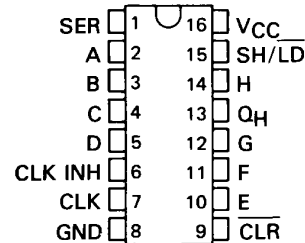
The '166 and 'LS166A 8-bit shift registers are compatible with most other TTL logic families. All '166 and 'LS166A inputs are buffered to lower the drive requirements to one Series 54/74 or Series 54LS/74LS standard load, respectively. Input clamping diodes minimize switching transients and simplify system design.

These parallel-in or serial-in, serial-out shift registers have a complexity of 77 equivalent gates on a monolithic chip. They feature gated clock inputs and an overriding clear input. The parallel-in or serial-in modes are established by the shift/load input. When high, this input enables the serial data input and couples the eight flip-flops for serial shifting with each clock pulse. When low, the parallel (broadside) data inputs are enabled and synchronous loading occurs on the next clock pulse. During parallel loading, serial data flow is inhibited. Clocking is accomplished on the low-to-high-level edge of the clock pulse through a two-input positive NOR gate permitting one input to be used as a clock-enable or clock-inhibit function. Holding either of the clock inputs high inhibits clocking; holding either low enables the other clock input. This, of course, allows the system clock to be free-running and the register can be stopped on command with the other clock input. The clock inhibit input should be changed to the high level only while the clock input is high. A buffered, direct clear input overrides all other inputs, including the clock, and sets all flip-flops to zero.

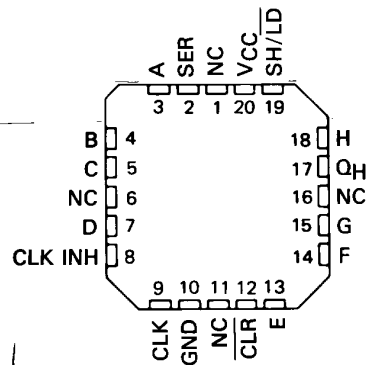
FUNCTION TABLE

CLEAR	INPUTS					INTERNAL OUTPUTS		OUTPUT Q _H
	SHIFT/ LOAD	CLOCK INHIBIT	CLOCK	SERIAL	PARALLEL A...H	Q _A	Q _B	
L	X	X	X	X	X	L	L	L
H	X	L	L	X	X	Q _{A0}	Q _{B0}	Q _{H0}
H	L	L	↑	X	a...h	a	b	h
H	H	L	↑	H	X	H	Q _{An}	Q _{Gn}
H	H	L	↑	L	X	L	Q _{An}	Q _{Gn}
H	X	H	↑	X	X	Q _{A0}	Q _{B0}	Q _{H0}

SN54166, SN54LS166A ... J OR W PACKAGE
SN74166 ... N PACKAGE
SN74LS166A ... D OR N PACKAGE
(TOP VIEW)

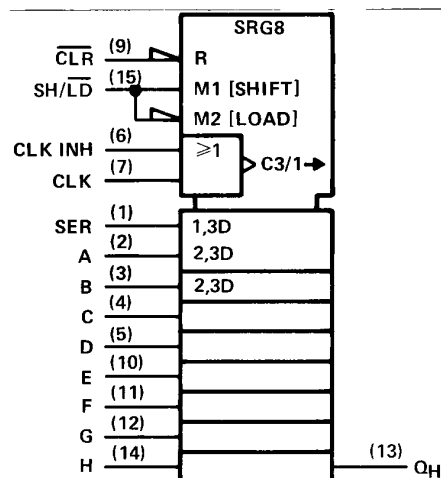


SN54LS166A ... FK PACKAGE
(TOP VIEW)



NC - No internal connection

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pin numbers shown are for D, J, N, and W packages.

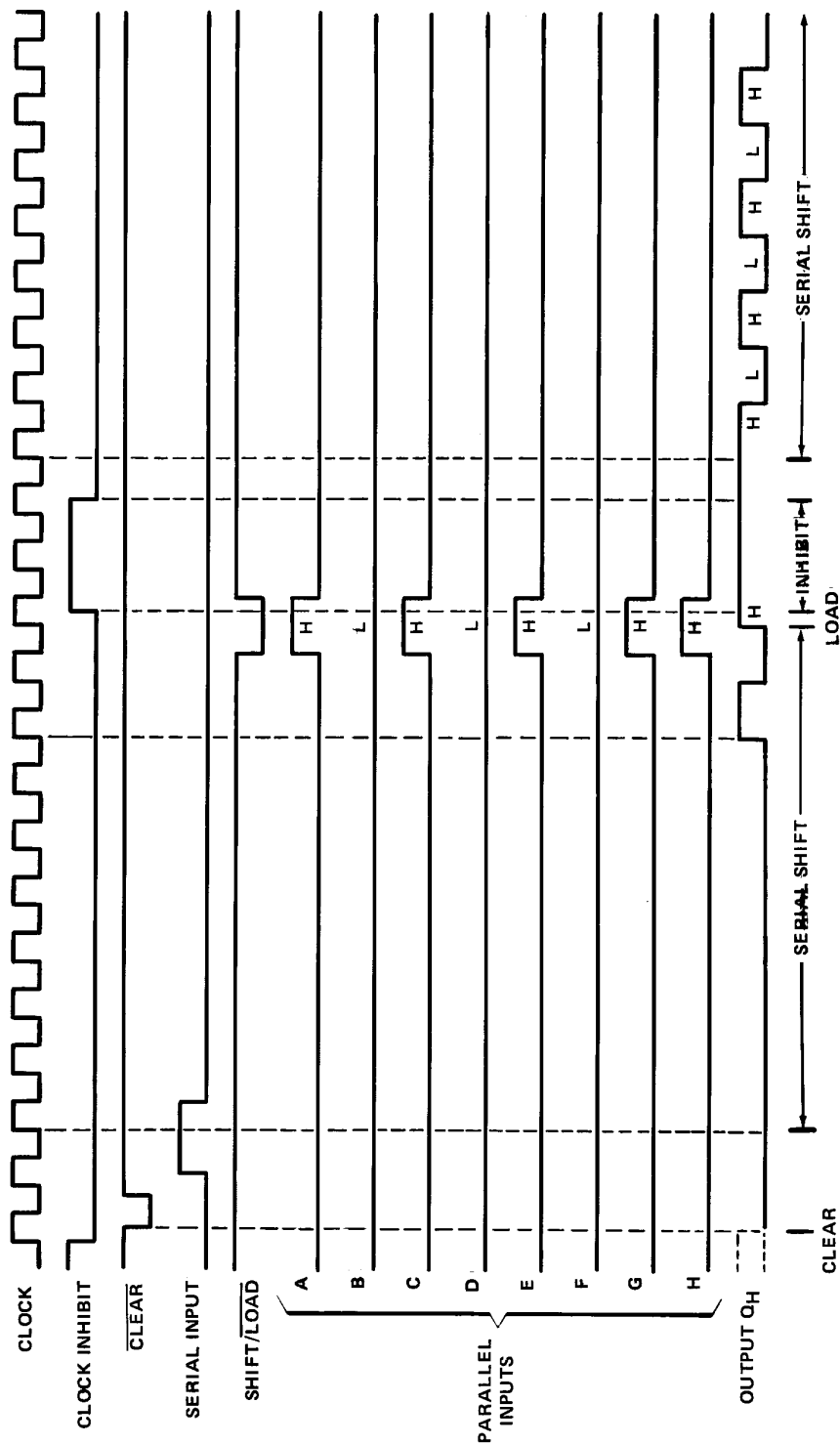
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INSTRUMENTS

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SN54166, SN54LS166A, SN74166, SN74LS166A
PARALLEL-LOAD 8-BIT SHIFT REGISTERS

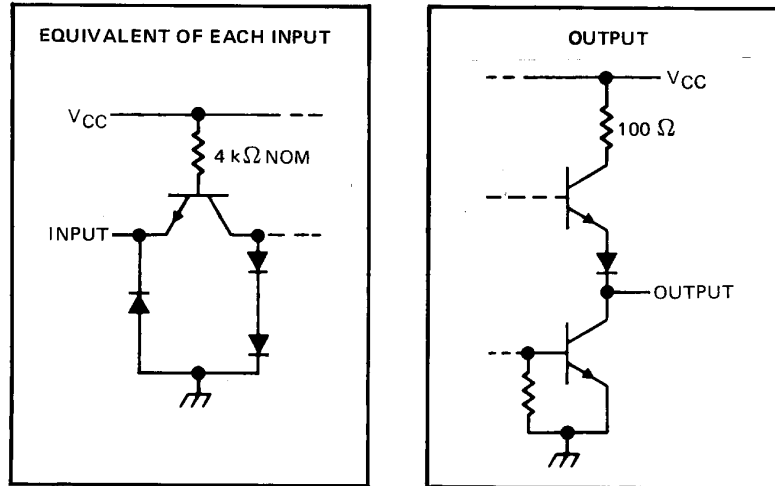
typical clear, shift, load, inhibit, and shift sequences



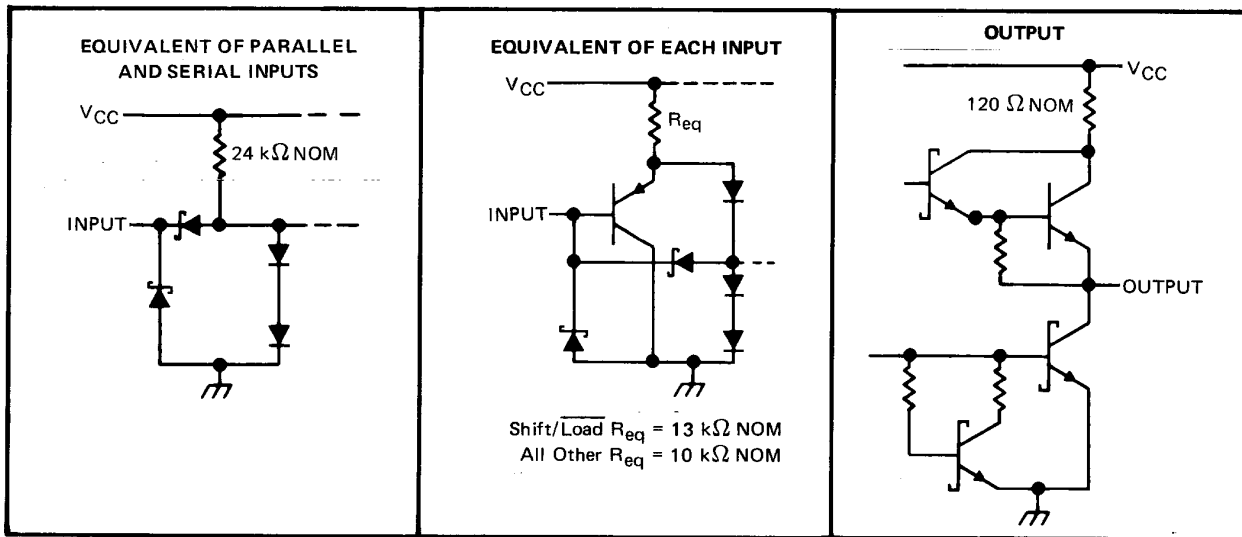
SN54166, SN54LS166A, SN74166, SN74LS166A
PARALLEL-LOAD 8-BIT SHIFT REGISTERS

schematics of inputs and outputs

'166



'LS166A

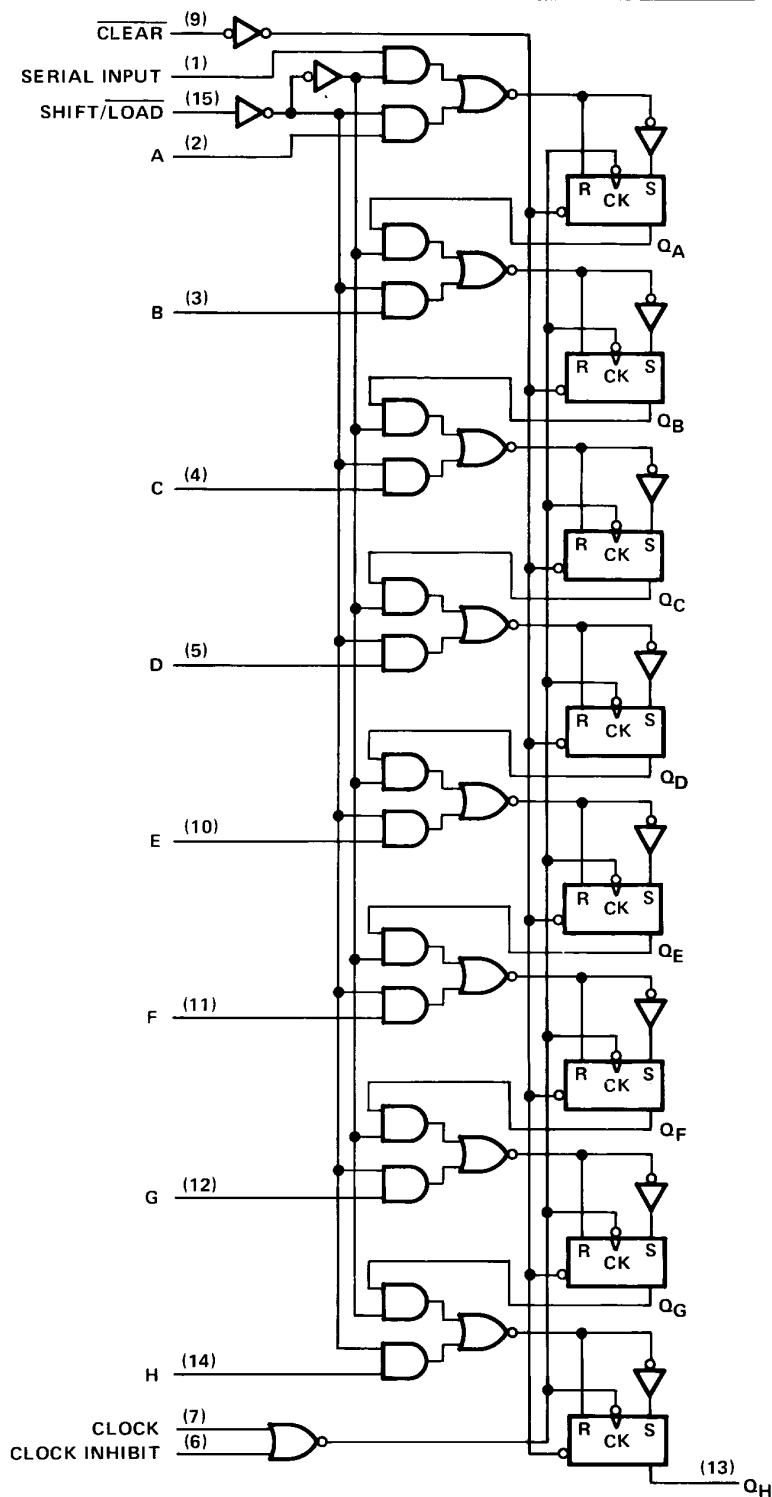


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TTL Devices

SN54166, SN54LS166A, SN74166, SN74LS166A
PARALLEL-LOAD 8-BIT SHIFT REGISTERS

logic diagram (positive logic)



Pin numbers shown are for D, J, N, and W packages.

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TTL Devices

SN54166, SN74166 PARALLEL-LOAD 8-BIT SHIFT REGISTERS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage	5.5 V
Operating free-air temperature range: SN54166 (see Note 2)	−55°C to 125°C
SN74166	0°C to 70°C
Storage temperature range	−65°C to 150°C

recommended operating conditions

	SN54166			SN74166			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			−800			−800	μA
Low-level output current, I_{OL}			16			16	mA
Clock frequency, f_{clock}	0		25	0		25	MHz
Width of clock or clear pulse, t_W (see Figure 1)	20			20			ns
Mode-control setup time, t_{su}	30			30			ns
Data setup time, t_{su} (see Figure 1)	20			20			ns
Hold time at any input, t_h (see Figure 1)	0			0			ns
Operating free-air temperature, T_A (see Note 2)	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	SN54166			SN74166			UNIT
		MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH} High-level input voltage		2			2			V
V_{IL} Low-level input voltage				0.8			0.8	V
V_{IK} Input clamp voltage	$V_{CC} = \text{MIN}, I_I = -12 \text{ mA}$			−1.5			−1.5	V
V_{OH} High-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = 0.8 \text{ V}, I_{OH} = -800 \mu\text{A}$	2.4	3.4		2.4	3.4		V
V_{OL} Low-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = 0.8 \text{ V}, I_{OL} = 16 \text{ mA}$		0.2	0.4		0.2	0.4	V
I_I Input current at maximum input voltage	$V_{CC} = \text{MAX}, V_I = 5.5 \text{ V}$			1			1	mA
I_{IH} High-level input current	$V_{CC} = \text{MAX}, V_I = 2.4 \text{ V}$			40			40	μA
I_{IL} Low-level input current	$V_{CC} = \text{MAX}, V_I = 0.4 \text{ V}$			−1.6			−1.6	mA
I_{OS} Short-circuit output current§	$V_{CC} = \text{MAX}$	−20		−57	−18		−57	mA
I_{CC} Supply current	$V_{CC} = \text{MAX}, \text{ See Note 3}$		90	127		90	127	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$.

§Not more than one output should be shorted at a time.

NOTES: 1. Voltage values are with respect to network ground terminal.

2. An SN54166 in the W package operating at free-air temperatures above 113°C requires a heat-sink that provides a thermal resistance from case to free air, $R_{\theta CA}$, of not more than 48°C/W.

3. With all outputs open, 4.5 V applied to the serial input, all other inputs except the clock grounded, I_{CC} is measured after a momentary ground, then 4.5 V, is applied to the clock.

switching characteristics, $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max} Maximum clock frequency		25	35		MHz
t_{PHL} Propagation delay time, high-to-low-level output from clear	$C_L = 15 \text{ pF}, R_L = 400 \Omega,$ See Figure 1		23	35	ns
t_{PHL} Propagation delay time, high-to-low-level output from clock			20	30	ns
t_{PLH} Propagation delay time, low-to-high-level output from clock			17	26	ns

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TTL Devices

SN54LS166A, SN74LS166A PARALLEL-LOAD 8-BIT SHIFT REGISTERS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage	7 V
Operating free-air temperature range: SN54LS166A	– 55°C to 125°C
SN74LS166A	0°C to 70°C
Storage temperature range	– 65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

		SN54LS166A			SN74LS166A			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.7			0.8	V
I_{OH}	High-level output current			– 0.4			– 0.4	mA
I_{OL}	Low-level output current			4			8	mA
f_{clock}	Clock frequency	0		25	0		25	MHz
t_w	Width of clear pulse (See Figure 1)	20			20			ns
t_w	Width of clock pulse (See Figure 1)	25			25			
t_{su}	Mode-control setup time	30			30			ns
t_{su}	Data setup time (See Figure 1)	20			20			ns
t_h	Hold time at any input (See Figure 1 and Note 4)	0			0			ns
T_A	Operating free air temperature	– 55		125	0		70	°C

NOTE 4: The hold time limit of 0 ns applies only if the rise time is less than or equal to 10 ns.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS †	SN54LS166A			SN74LS166A			UNIT
		MIN	TYP ‡	MAX	MIN	TYP ‡	MAX	
V_{IK}	$V_{CC} = \text{MIN}, I_I = -18 \text{ mA}$			– 1.5			– 1.5	V
V_{OH}	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = \text{MAX}, I_{OH} = -0.4 \text{ mA}$	2.5	3.4		2.7	3.4		V
V_{OL}	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = \text{MAX}, I_{OL} = 4 \text{ mA}$	0.25	0.4		0.25	0.4		V
	$I_{OL} = 8 \text{ mA}$				0.35	0.5		
I_I	$V_{CC} = \text{MAX}, V_I = 7 \text{ V}$			0.1			0.1	mA
I_{IH}	$V_{CC} = \text{MAX}, V_I = 2.7 \text{ V}$			20			20	µA
I_{IL}	$V_{CC} = \text{MAX}, V_I = 0.4 \text{ V}$			– 0.4			– 0.4	mA
$I_{OS} §$	$V_{CC} = \text{MAX}$	– 20		– 100	– 20		– 100	mA
I_{CC}	$V_{CC} = \text{MAX}, \text{ See Note 5}$		20	32		20	32	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$.

§Not more than one output should be shorted at a time, and duration for short-circuit should not exceed one second.

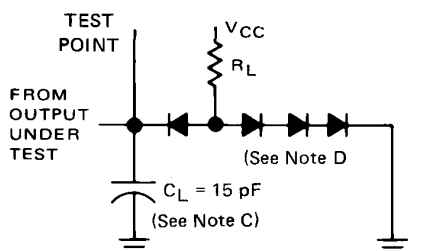
NOTE 5: With all outputs open, 4.5 V applied to the serial input and all other inputs except the clock grounded, I_{CC} is measured after a momentary ground, than 4.5 V, is applied to clock.

switching characteristics, $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max} Maximum clock frequency	$C_L = 15 \text{ pF}, R_L = 2 \text{ k}\Omega$, See Figure 1	25	35		MHz
t_{PHL} Propagation delay time, high-to-low-level output from clear			19	30	ns
t_{PHL} Propagation delay time, high-to-low-level output from clock		7	14	25	ns
t_{PLH} Propagation delay time, low-to-high-level output from clock		5	11	20	ns

SN54166, SN54LS166A, SN74166, SN74LS166A PARALLEL-LOAD 8-BIT SHIFT REGISTERS

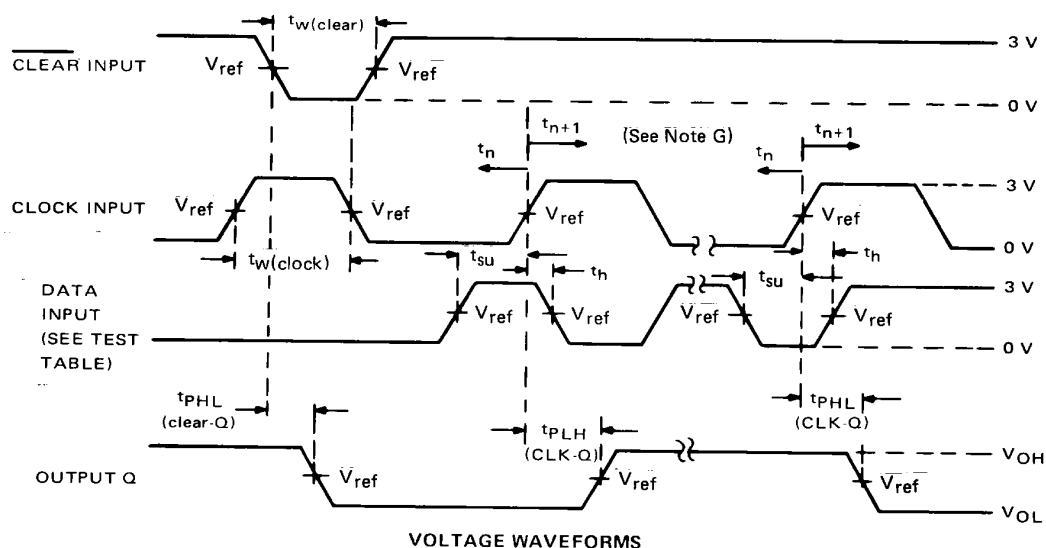
PARAMETER MEASUREMENT INFORMATION



LOAD FOR OUTPUT UNDER TEST

TEST TABLE FOR SYNCHRONOUS INPUTS

DATA INPUT FOR TEST	SHIFT/LOAD	OUTPUT TESTED (SEE NOTE F)
H	0 V	Q_H at t_{n+1}
Serial Input	4.5 V	Q_H at t_{n+8}



- NOTE: A. All pulse generators have the following characteristics: $Z_{out} \approx 50\Omega$; for '166, $t_r \leq 7$ ns and $t_f \leq 7$ ns; for 'LS166A, $t_r \leq 15$ ns and $t_f \leq 6$ ns.
- B. The clock pulse has the following characteristics: $t_w(\text{clock}) \leq 20$ ns and $\text{PRR} = 1$ MHz. The clear pulse has the following characteristics: $t_w(\text{clear}) \leq 20$ ns and $t_{\text{hold}} = 0$ ns. When testing f_{max} , vary the clock PRR.
- C. C_L includes probe and jig capacitance.
- D. All diodes are 1N3064, 1N916, or equivalent.
- E. A clear pulse is applied prior to each test.
- F. Propagation delay times (t_{PLH} and t_{PHL}) are measured at t_{n+1} . Proper shifting of data is verified at t_{n+8} with a functional test.
- G. t_n = bit time before clocking transition
 t_{n+1} = bit time after one clocking transition
 t_{n+8} = bit time after eight clocking transitions
- H. For '166 $V_{\text{ref}} = 1.5$ V; for 'LS166A $V_{\text{ref}} = 1.3$ V.

FIGURE 1

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TTL Devices

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
5962-9558301QEA	ACTIVE	CDIP	J	16	1	TBD	A42 SNPB	N / A for Pkg Type
5962-9558301QFA	ACTIVE	CFP	W	16	1	TBD	A42	N / A for Pkg Type
5962-9558301QFA	ACTIVE	CFP	W	16	1	TBD	A42	N / A for Pkg Type
8001701EA	ACTIVE	CDIP	J	16	1	TBD	A42 SNPB	N / A for Pkg Type
8001701EA	ACTIVE	CDIP	J	16	1	TBD	A42 SNPB	N / A for Pkg Type
8001701FA	ACTIVE	CFP	W	16	1	TBD	A42	N / A for Pkg Type
8001701FA	ACTIVE	CFP	W	16	1	TBD	A42	N / A for Pkg Type
JM38510/30609B2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type
JM38510/30609B2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type
JM38510/30609BEA	ACTIVE	CDIP	J	16	1	TBD	A42 SNPB	N / A for Pkg Type
JM38510/30609BEA	ACTIVE	CDIP	J	16	1	TBD	A42 SNPB	N / A for Pkg Type
JM38510/30609BFA	ACTIVE	CFP	W	16	1	TBD	A42	N / A for Pkg Type
JM38510/30609BFA	ACTIVE	CFP	W	16	1	TBD	A42	N / A for Pkg Type
SN54166J	ACTIVE	CDIP	J	16	1	TBD	A42 SNPB	N / A for Pkg Type
SN54166J	ACTIVE	CDIP	J	16	1	TBD	A42 SNPB	N / A for Pkg Type
SN54LS166AJ	ACTIVE	CDIP	J	16	1	TBD	A42 SNPB	N / A for Pkg Type
SN54LS166AJ	ACTIVE	CDIP	J	16	1	TBD	A42 SNPB	N / A for Pkg Type
SN74166N	OBSOLETE	PDIP	N	16		TBD	Call TI	Call TI
SN74166N	OBSOLETE	PDIP	N	16		TBD	Call TI	Call TI
SN74166N3	OBSOLETE	PDIP	N	16		TBD	Call TI	Call TI
SN74166N3	OBSOLETE	PDIP	N	16		TBD	Call TI	Call TI
SN74LS166AD	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS166AD	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS166ADE4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS166ADE4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS166ADR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS166ADR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS166ADRE4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS166ADRE4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS166AJ	OBSOLETE	CDIP	J	16		TBD	Call TI	Call TI
SN74LS166AJ	OBSOLETE	CDIP	J	16		TBD	Call TI	Call TI
SN74LS166AN	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74LS166AN	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74LS166AN3	OBSOLETE	PDIP	N	16		TBD	Call TI	Call TI
SN74LS166AN3	OBSOLETE	PDIP	N	16		TBD	Call TI	Call TI

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
SN74LS166ANE4	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74LS166ANE4	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74LS166ANSR	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS166ANSR	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS166ANSRE4	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS166ANSRE4	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SNJ54166J	ACTIVE	CDIP	J	16	1	TBD	A42 SNPB	N / A for Pkg Type
SNJ54166J	ACTIVE	CDIP	J	16	1	TBD	A42 SNPB	N / A for Pkg Type
SNJ54166W	ACTIVE	CFP	W	16	1	TBD	A42	N / A for Pkg Type
SNJ54166W	ACTIVE	CFP	W	16	1	TBD	A42	N / A for Pkg Type
SNJ54LS166AFK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type
SNJ54LS166AFK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type
SNJ54LS166AJ	ACTIVE	CDIP	J	16	1	TBD	A42 SNPB	N / A for Pkg Type
SNJ54LS166AJ	ACTIVE	CDIP	J	16	1	TBD	A42 SNPB	N / A for Pkg Type
SNJ54LS166AW	ACTIVE	CFP	W	16	1	TBD	A42	N / A for Pkg Type
SNJ54LS166AW	ACTIVE	CFP	W	16	1	TBD	A42	N / A for Pkg Type

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBsolete: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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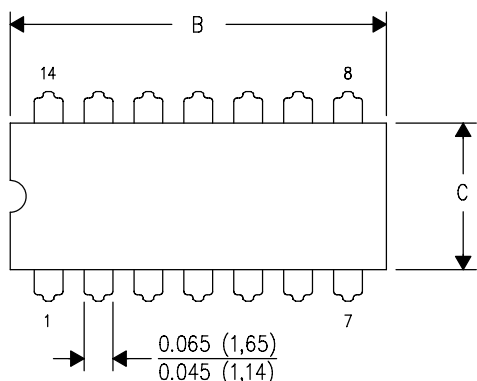
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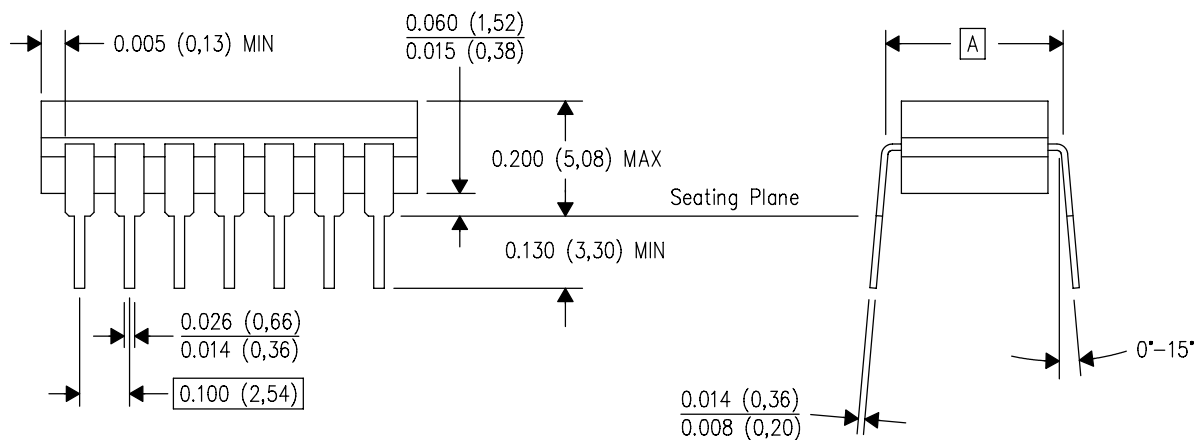
J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



PINS ** DIM	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)

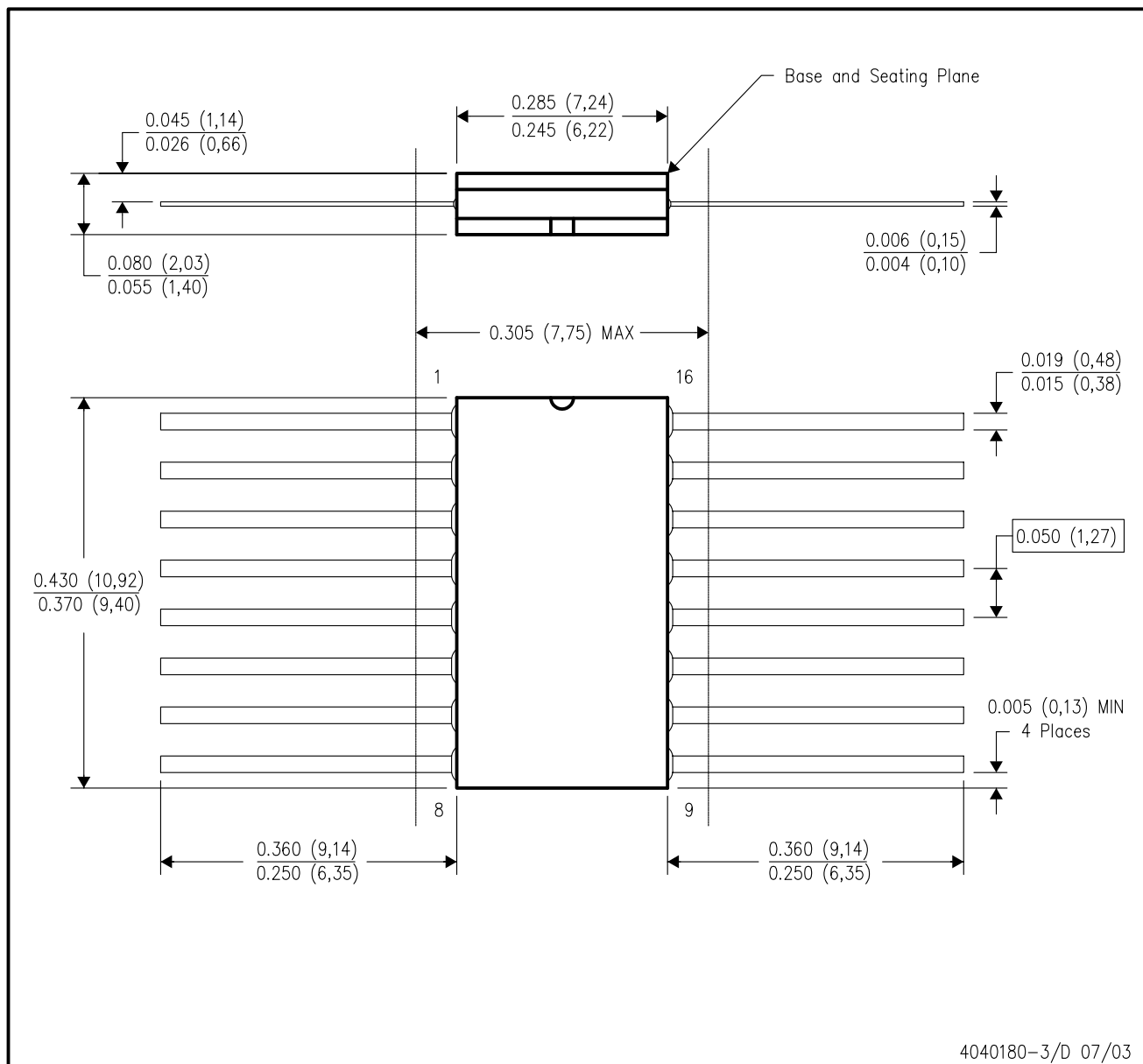


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- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package is hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
 - E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

W (R-GDFP-F16)

CERAMIC DUAL FLATPACK

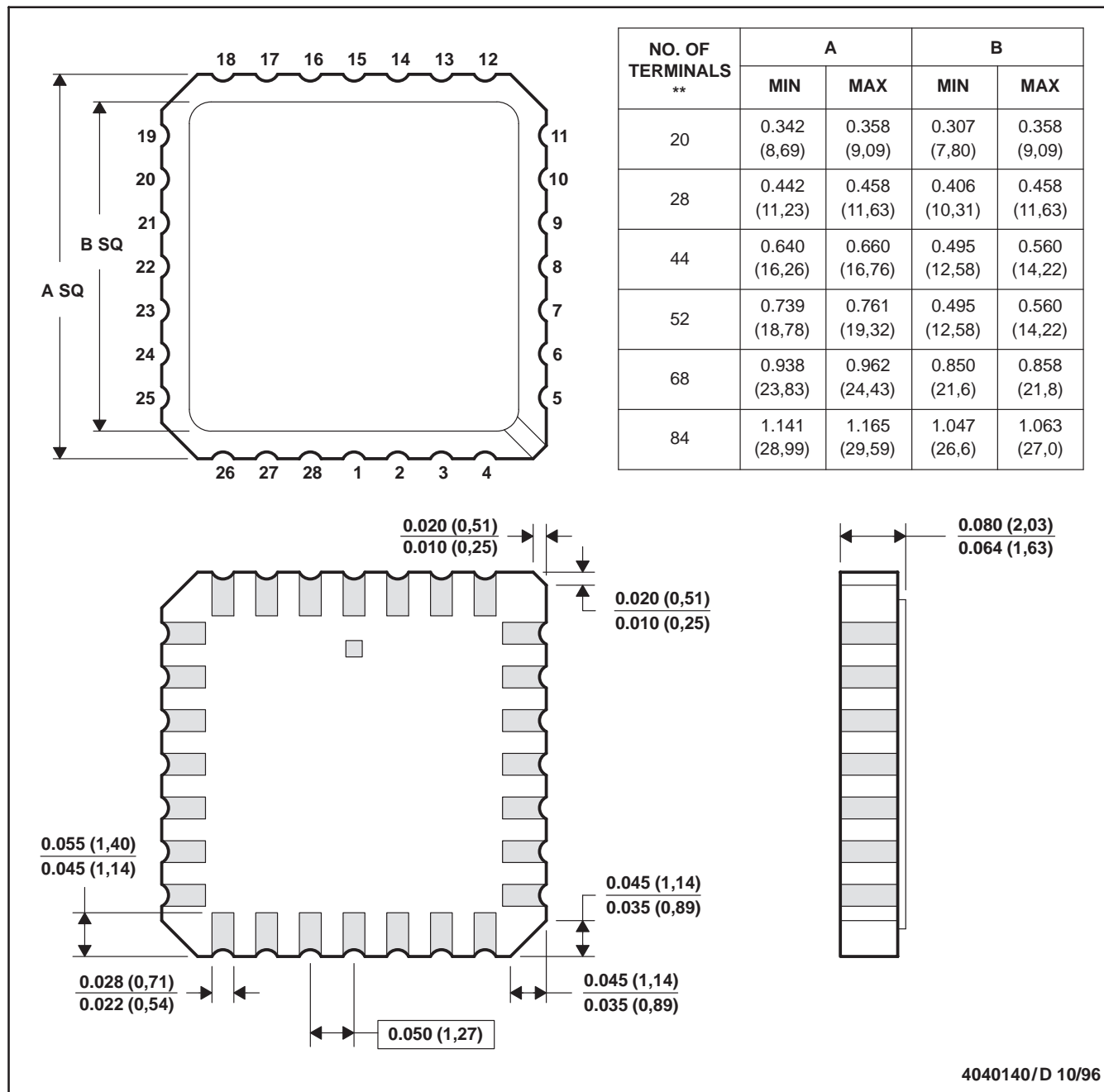


- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package can be hermetically sealed with a ceramic lid using glass frit.
 - Index point is provided on cap for terminal identification only.
 - Falls within MIL STD 1835 GDFP1-F16 and JEDEC MO-092AC

FK (S-CQCC-N**)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN

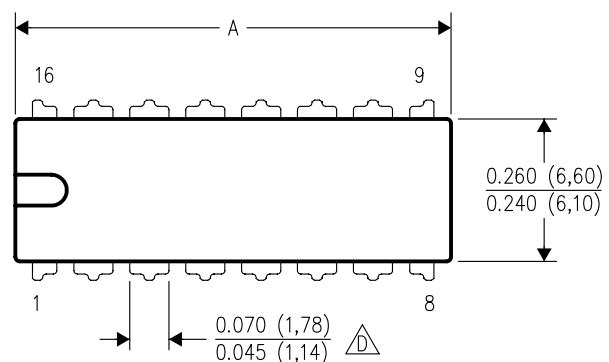


- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package can be hermetically sealed with a metal lid.
 - D. The terminals are gold plated.
 - E. Falls within JEDEC MS-004

N (R-PDIP-T**)

16 PINS SHOWN

PLASTIC DUAL-IN-LINE PACKAGE





PINS ** DIM	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS-001 VARIATION	AA	BB	AC	AD



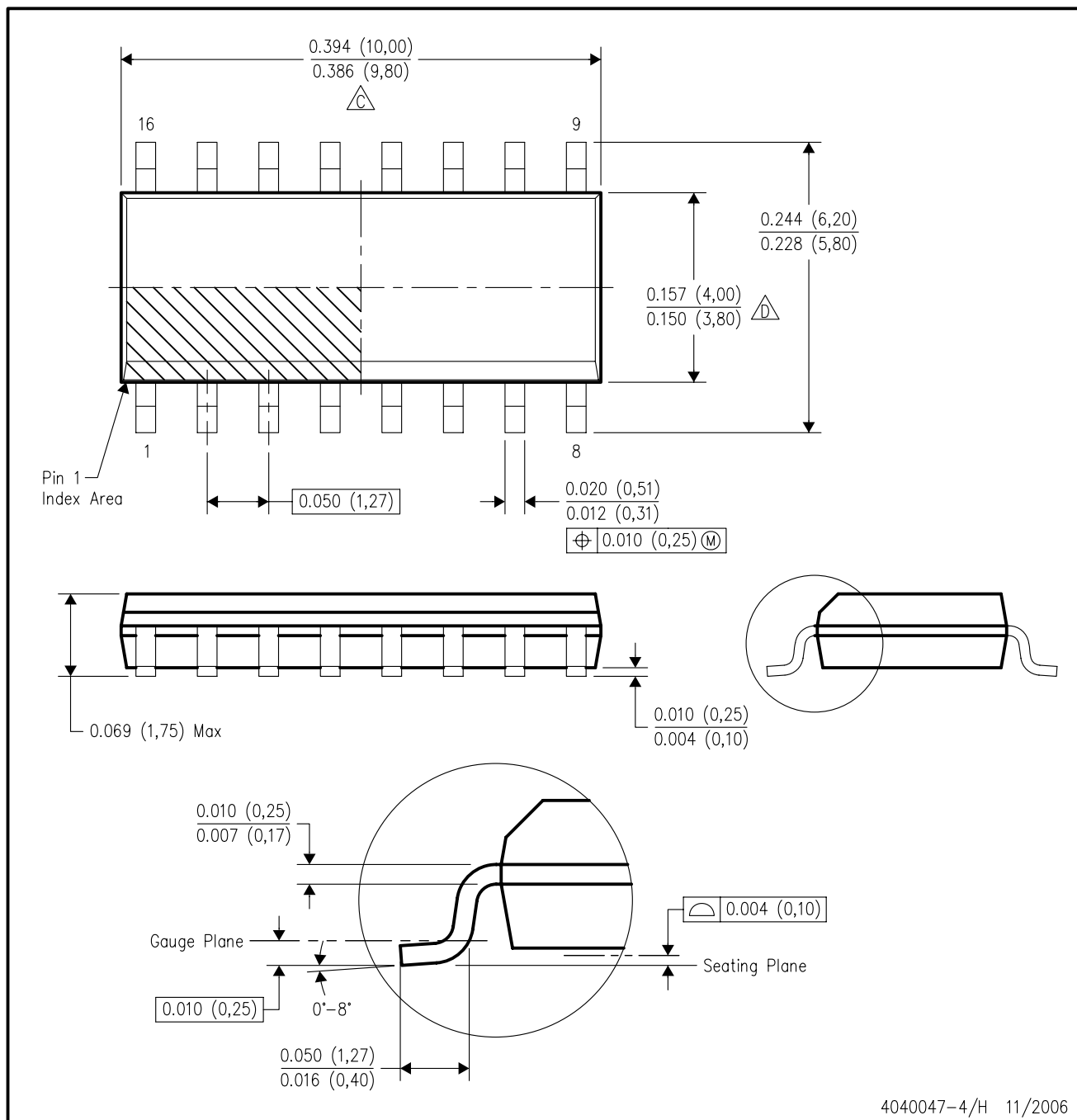
4040049/E 12/2002

NOTES:

- A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
-  Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 The 20 pin end lead shoulder width is a vendor option, either half or full width.

D (R-PDSO-G16)

PLASTIC SMALL-OUTLINE PACKAGE



4040047-4/H 11/2006

NOTES:

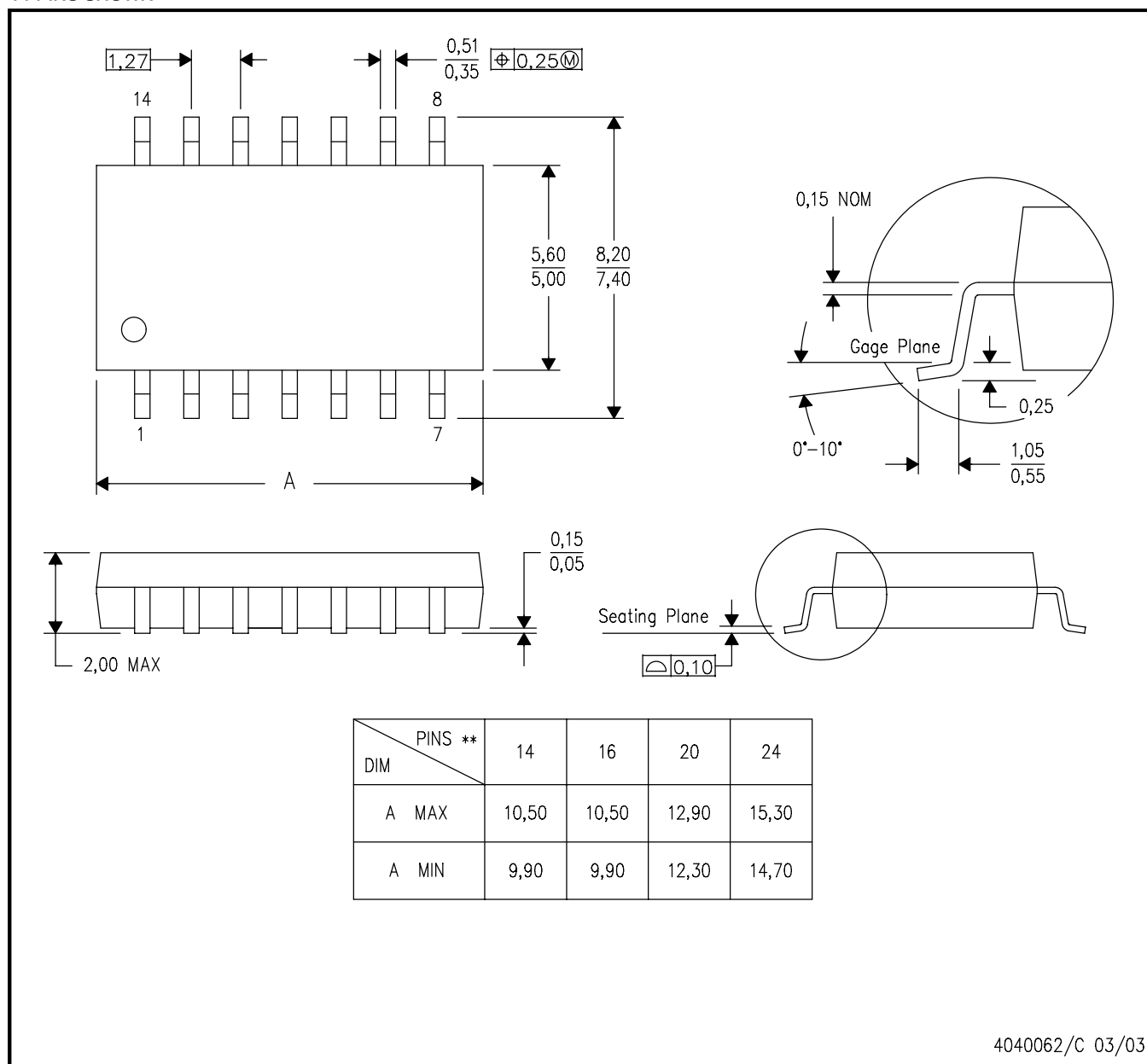
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.
- D. Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.
- E. Reference JEDEC MS-012 variation AC.

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

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