MOS
INTEGRATED CIRCUITS

SGS
Z 80-PIO
Z 80A-PIO

Product Specification

The SGS-ATES Z80 product line is a complete set of microcomputer components, development systems and support software. The Z-80 microcomputer component set includes all of the circuits necessary to build high-performance microcomputer systems with virtually no other logic and a minimum number of low cost standard memory elements.

The Z-80 Parallel I/O (PIO) Interface Controller is a programmable, two port device which provides TTL compatible interfacing between peripheral devices and the Z80-CPU. The Z80-CPU configures the Z80-PIO to interface with standard peripheral devices such as tape punches, printers, keyboards, etc.

Structure

- N-Channel Silicon Gate Depletion Load technology
- 40 Pin DIP
- Single 5 volt supply
- Single phase 5 volt clock
- Two independent 8-bit bidirectional peripheral interface ports with "handshake" data transfer control

Features

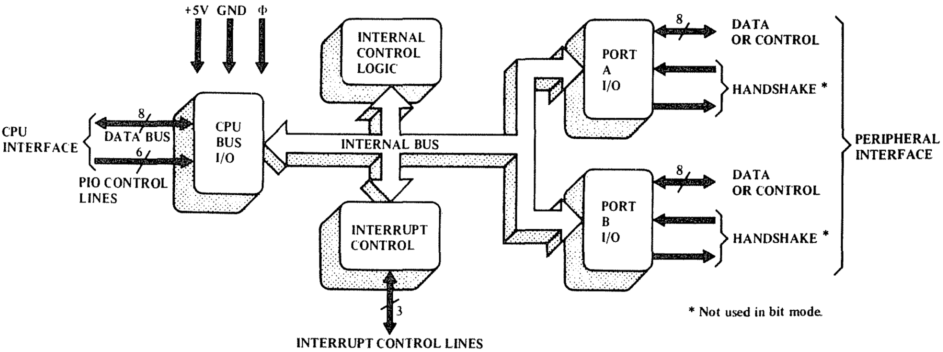
- Interrupt driven "handshake" for fast response
- Any one of the following modes of operation may be selected for either port:
    - Byte output
    - Byte input
    - Byte bidirectional bus (available on Port A only)
    - Bit Mode
- Programmable interrupts on peripheral status conditions
- Daisy chain priority interrupt logic included to provide for automatic interrupt vectoring without external logic.
- Eight outputs are capable of driving Darlington transistors.
- All inputs and outputs fully TTL compatible.

PIO Architecture

A block diagram of the Z80-PIO is shown in figure 3. The internal structure of the Z80-PIO consists of a Z80-CPU bus interface, internal control logic, Port A I/O logic, Port B I/O logic, and interrupt control logic. A typical application might use Port A as the data transfer channel and Port B for the status and control monitoring.

The Port I/O logic is composed of 6 registers with "handshake" control logic as shown in figure 4. The registers include: an 8-bit input register, an 8-bit output register, a 2-bit mode control register, an 8-bit mask register, an 8-bit input/output select register, and a 2-bit mask control register. The last three registers are used only when the port has been programmed to operate in the bit mode.

Fig. 3 - PIO BLOCK DIAGRAM



* Not used in bit mode.

Register Description

Mode Control Register–2 bits, loaded by CPU to select the operating mode: byte output, byte input, byte bidirectional bus or bit mode.

Data Output Register–8 bits, permits data to be transferred from the CPU to the peripheral.

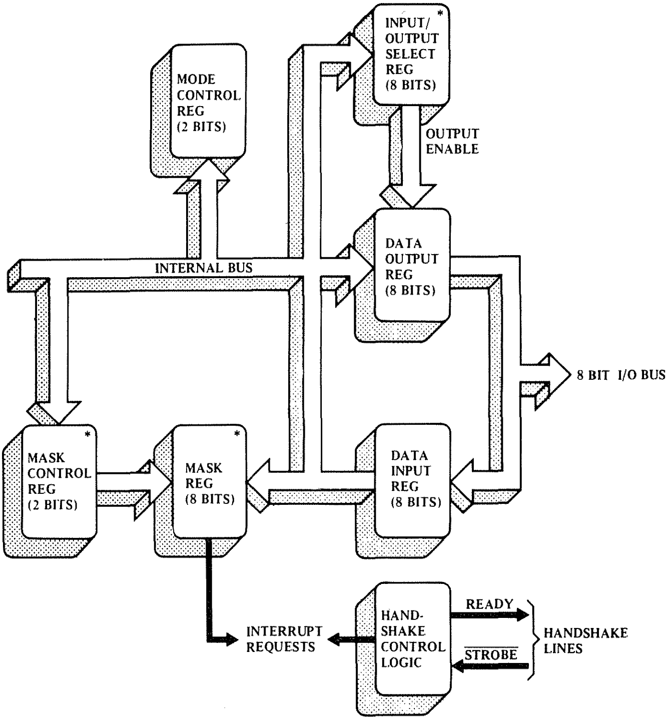
Data Input Register–8 bits, accepts data from the peripheral for transfer to the CPU.

Mask Control Register–2 bits, loaded by the CPU to specify the active state (high or low) of any peripheral device interface pins that are to be monitored and, if an interrupt should be generated when all unmasked pins are active (AND condition) or, when any unmasked pin is active (OR condition).

Mask Register–8 bits, loaded by the CPU to determine which peripheral device interface pins are to be monitored for the specified status condition.

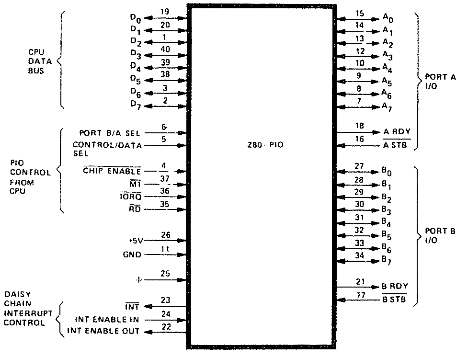
Input/Output Select Register–8 bits, loaded by the CPU to allow any pin to be an output or an input during bit mode operation.

Fig. 4 - A TYPICAL PORT I/O BLOCK DIAGRAM



* Used in the bit mode only to allow generation of an interrupt if the peripheral I/O pins go to the specified state.

Z80–PIO Pin Description

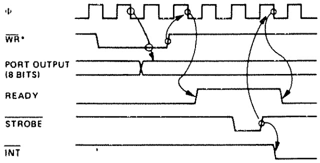


D_7-D_0	Z80-CPU Data Bus (bidirectional, tristate)
B/A Sel	Port B or A Select (input, active high)
C/D Sel	Control or Data Select (input, active high)
$\overline{\text{CE}}$	Chip Enable (input, active low)
Φ	System Clock (input)
$\overline{\text{M1}}$	Machine Cycle One Signal from CPU (input, active low)
$\overline{\text{IORQ}}$	Input/Output Request from Z80-CPU (input, active low)
$\overline{\text{RD}}$	Read Cycle Status from the Z80-CPU (input, active low)
IEI	Interrupt Enable In (input, active high)
IEO	Interrupt Enable Out (output, active high). IEI and IEO form a daisy chain connection for priority interrupt control.
$\overline{\text{INT}}$	Interrupt Request (output, open drain, active low)
A_0-A_7	Port A Bus (bidirectional, tristate)
$\overline{\text{A STB}}$	Port A Strobe Pulse from Peripheral Device (input, active low)
A RDY	Register A Ready (output, active high)
B_0-B_7	Port B Bus (bidirectional, tristate)
$\overline{\text{B STB}}$	Port B Strobe Pulse from Peripheral Device (input, active low)
B RDY	Register B Ready (output, active high)

Timing Waveforms

OUTPUT MODE

An output cycle is always started by the execution of an output instruction by the CPU. The $\overline{\text{WR}}$ pulse from the CPU latches the data from the CPU data bus into the selected port's output register. The write pulse sets the ready flag after a low going edge of Φ, indicating data is available. Ready stays active until the positive edge of the strobe line is received indicating that data was taken by the peripheral. The positive edge of the strobe pulse generates an $\overline{\text{INT}}$ if the interrupt enable flip flop has been set and if this device has the highest priority.

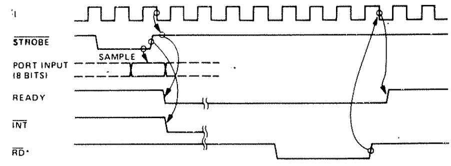


MODE 0 (OUTPUT) TIMING

WR* = $\overline{\text{RD}}$ · CE · $\overline{\text{C/D}}$ · IORQ

INPUT MODE

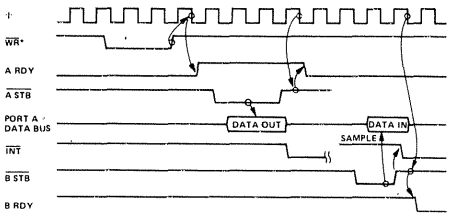
When $\overline{\text{STROBE}}$ goes low data is loaded into the selected port input register. The next rising edge of strobe activates $\overline{\text{INT}}$ if interrupt enable is set and this is the highest priority requesting device. The following falling edge of Φ resets Ready to an inactive state, indicating that the input register is full and cannot accept any more data until the CPU completes a read. When a read is complete the positive edge of $\overline{\text{RD}}$ will set Ready at the next low going transition of Φ. At this time new data can be loaded into the PIO.



RD* = RD · CE · $\overline{\text{C/D}}$ · IORQ   MODE 1 (INPUT) TIMING

BIDIRECTIONAL MODE

This is a combination of modes 0 and 1 using all four handshake lines and the 8 Port A I/O lines. Port B must be set to the Bit Mode. The Port A handshake lines are used for output control and the Port B lines are used for input control. Data is allowed out onto the Port A bus only when $\overline{\text{A STB}}$ is low. The rising edge of this strobe can be used to latch the data into the peripheral.

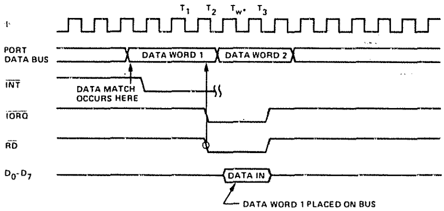


WR* = $\overline{\text{RD}}$ · CE · $\overline{\text{C/D}}$ · IORQ

BIT MODE

The bit mode does not utilize the handshake signals and a normal port write or port read can be executed at any time. When writing, the data will be latched into the output registers with the same timing as the output mode.

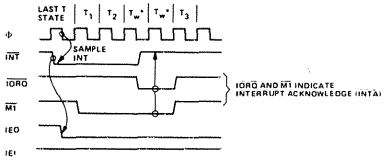
When reading the PIO, the data returned to the CPU will be composed of output register data from those port data lines assigned as outputs and input register data from those port data lines assigned as inputs. The input register will contain data which was present immediately prior to the falling edge of $\overline{\text{RD}}$. An interrupt will be generated if interrupts from the port are enabled and the data on the port data lines satisfy the logical equation defined by the 8-bit mask and 2-bit mask control registers.



* Timing Diagram Refers to Bit Mode Read

INTERRUPT ACKNOWLEDGE

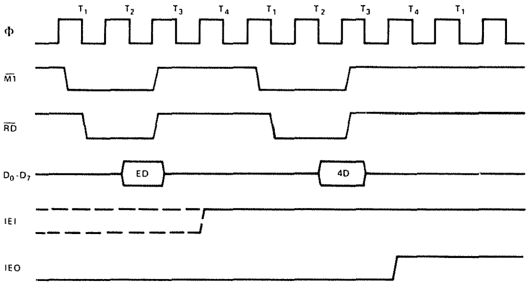
During $\overline{\text{MI}}$ time, peripheral controllers are inhibited from changing their interrupt enable status, permitting the $\overline{\text{INT}}$ Enable signal to ripple through the daisy chain. The peripheral with IEI high and IEO low during $\overline{\text{INTA}}$ will place a preprogrammed 8-bit interrupt vector on the data bus at this time. IEO is held low until a return from interrupt (RETI) instruction is executed by the CPU while IEI is high. The 2-byte RETI instruction is decoded internally by the PIO for this purpose.



RETURN FROM INTERRUPT CYCLE

If a Z80 peripheral device has no interrupt pending and is not under service, then its IEO=IEI. If it has an interrupt under service (i.e., it has already interrupted and received an interrupt acknowledge) then its IEO is always low, inhibiting lower priority chips from interrupting. If it has an interrupt pending which has not yet been acknowledged, IEO will be low unless an "ED" is decoded as the first byte of a two byte opcode. In this case, IEO will go high until the next opcode byte is decoded, whereupon it will again go low. If the second byte of the opcode was a "4D" then the opcode was an RETI instruction.

After an "ED" opcode is decoded, only the peripheral device which has interrupted and is currently under service will have its IEI high and its IEO low. This device is the highest priority device in the daisy chain which has received an interrupt acknowledge. All other peripherals have IEI=IEO. If the next opcode byte decoded is "4D", this peripheral device will reset its "interrupt under service" condition.



PIO Programming

LOAD INTERRUPT VECTOR

The Z80-CPU requires an 8-bit interrupt vector be supplied by the interrupting device. The CPU forms the address for the interrupt service routine of the port using this vector. During an interrupt acknowledge cycle the vector is placed on the Z-80 data bus by the highest priority device requesting service at that time. The desired interrupt vector is loaded into the PIO by writing a control word to the desired port of the PIO with the following format.

D7	D6	D5	D4	D3	D2	D1	D0
V7	V6	V5	V4	V3	V2	V1	0

signifies this control word is an interrupt vector

SELECTING AN OPERATING MODE

When selecting an operating mode, the 2-bit mode control register is set to one of four values. These two bits are the most significant bits of the register, bits 7 and 6; bits 5 and 4 are not used while bits 3 through 0 are all set to 1111 to indicate "set mode."

D7	D6	D5	D4	D3	D2	D1	D0
M1	M0	X	X	1	1	1	1

mode word (D7–D6)

signifies mode word to be set (D3–D0)

X=unused bit

Mode	M_1	M_0
Output	0	0
Input	0	1
Bidirectional	1	0
Bit	1	1

MODE 0 active indicates that data is to be written from the CPU to the peripheral.

MODE 1 active indicates that data is to be read from the peripheral to the CPU.

MODE 2 allows data to be written to or read from the peripheral device.

MODE 3 is intended for status and control applications. When selected, the next control word must set the I/O Register to indicate which lines are to be input and which lines are to be output.

I/O = 1 sets bit to input.
I/O = 0 sets bit to output.

D7	D6	D5	D4	D3	D2	D1	D0
I/O_7	I/O_6	I/O_5	I/O_4	I/O_3	I/O_2	I/O_1	I/O_0

INTERRUPT CONTROL

Bit 7 = 1	interrupt enable is set–allowing interrupt to be generated.
Bit 7 = 0	indicates the enable flag is reset and interrupts may not be generated.
Bits 6,5,4	are used in the bit mode interrupt operations; otherwise they are disregarded.
Bits 3,2,1,0	signify that this command word is an interrupt control word.

D7	D6	D5	D4	D3	D2	D1	D0
Enable Interrupt	AND OR	High/ Low	Mask follows	0	1	1	1

used in Mode 3 only (D6–D4)

signifies interrupt control word (D3–D0)

If the "mask follows" bit is high (D4 = 1), the next control word written to the port must be the mask.

D7	D6	D5	D4	D3	D2	D1	D0
MB_7	MB_6	MB_5	MB_4	MB_3	MB_2	MB_1	MB_0

Only those port lines whose mask bit is a 0 will be monitored for generating an interrupt

The interrupt enable flip-flop of a port may be set or reset without modifying the rest of the interrupt control word by the following command.

D7	D6	D5	D4	D3	D2	D1	D0
Int Enable	X	X	X	0	0	1	1

Z80-PIO A.C. Characteristics

TA = 0° C to 70° C, Vcc = +5 V ± 5%, unless otherwise noted

Number	Symbol	Parameter	Min	Max	Unit	Comments
1	TcC	Clock Cycle Time	250	[1]	ns	
2	TcCh	Clock Width (High)	105	2000	ns	
3	TcCL	Clock Width (Low)	105	2000	ns	
4	TfC	Clock Fall Time		30	ns	
5	TrC	Clock Rise Time		30	ns	
6	TsCS(RI)	$\overline{\text{CE}}$. B/$\overline{\text{A}}$. C/E to $\overline{\text{RD}}$. $\overline{\text{IORQ}}$ ↓ Setup Time	50		ns	[6]
7	Th	Any Hold Time for specified Setup Time	0		ns	
8	TsRI(C)	$\overline{\text{RD}}$. $\overline{\text{IORQ}}$ to Clock ↑ Setup Time	115		ns	
9	TdRI(DO)	$\overline{\text{RD}}$. $\overline{\text{IORQ}}$ ↓ to Data Out Delay		380	ns	[2]
10	TdRI(DOr)	$\overline{\text{RD}}$, $\overline{\text{IORQ}}$ ↑ to Data Out Float Delay		110	ns	
11	TsDI(C)	Data In to Clock ↑ Setup Time	50		ns	CL = 50 pF
12	TdIO(DOI)	$\overline{\text{IORQ}}$ ↓ to Data Out Delay (INTA Cycle)	250		ns	[3]
13	TsM1(Cr)	$\overline{\text{M1}}$ ↓ to Clock ↑ Setup Time	90		ns	
14	TsM1(Cf)	$\overline{\text{M1}}$ ↑ to Clock ↓ Setup Time (M1 Cycle)	0		ns	
15	TdM1(IEO)	$\overline{\text{M1}}$ ↓ to IEO ↓ Delay (interrupt		190	ns	
		immediately preceding M1)		190	ns	[5] See Note A
16	TsIEI(IO)	IEI to IORQ ↓ Setup Time (INTA Cycle)	140		ns	See Note A
17	TdIEI(IEO)	IEI ↓ to IEO ↓ Delay		130	ns	[5] CL = 50 pF
18	TdIEI(IIOr)	IEI ↑ to IEO ↑ Delay (after ED Decode)		160	ns	[5]
19	TsIO(C)	$\overline{\text{IORQ}}$ ↑ to Clock ↓ Setup Time (To Activate READY on Next Clock Cycle)	220		ns	
20	TdC(RDYr)	Clock ↓ to READY ↑ Delay	200		ns	[5] CL = 50 pF
21	TdC(RDYf)	Clock ↓ to READY ↓ Delay	150		ns	[5]
22	TwSTB	$\overline{\text{STROBE}}$ Pulse Width	150 [4]		ns	
23	TsSTB(C)	STROBE ↑ to Clock ↓ Setup Time (To Activate READY on Next Clock Cycle)	200		ns	
24	TdIO(PD)	$\overline{\text{IORQ}}$ ↑ to PORT data stable Delay (Mode 0)		180	ns	[5]
25	TsPD(STB)	PORT DATA to STROBE ↑ Setup Time (Mode 1)	230		ns	
26	TdSTB(PD)	$\overline{\text{STROBE}}$ ↓ to PORT DATA Stable (Mode 2)		210	ns	[5]
27	TdSTB(PDz)	$\overline{\text{STROBE}}$ ↑ to PORT DATA Float Delay (Mode 2)		180	ns	CL = 50 pF
28	TdPD(INT)	PORT DATA Match to INT ↓ Delay (Mode 3)		490	ns	
29	TdSTB(INT)	$\overline{\text{STROBE}}$ ↑ to $\overline{\text{INT}}$ ↓ Delay		440	ns	

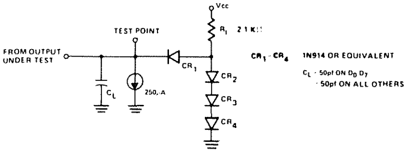
Notes A 2 5 TcC > (N-2) TdIEI (IEOG) + TdM1(IEO) + TsIEI(IO)+TTL Buffer Delay. if any
B. M1 Must be active for a minimum of 2 clock cycles to reset the PIO
[1] TcC = TwCh + TwCl + TrC + TfC
[2] Increase TdRI(DO) by 10 nsec for each 50 pF increase in loading up to 200 pF max
[3] Increase TdIO(DOT) by 10 nsec for each 60 pF increase in loading up to 200 pF max
[4] For Mode 2 TwSTB > TsPD(STB)
[5] Increase these values by 2 nsec for each 10 pF increase in loading up to 100 pF max
[6] TsCS(RI) may be reduced However the time subtracted from TsCS(RI) will be added to TdRI(DO)

Capacitance

TA = 25° C, f = 1 MHz

Symbol	Parameter	Max	Unit	Test Condition
C_Φ	Clock Capacitance	10	pF	Unmeasured Pins
C_{IN}	Input Capacitance	5	pF	Returned to Ground
C_{OUT}	Output Capacitance	10	pF	

Output Load circuit



Z80A-PIO A.C. Characteristics

TA = 0° C to 70° C, Vcc = +5 V ± 5%, unless otherwise noted

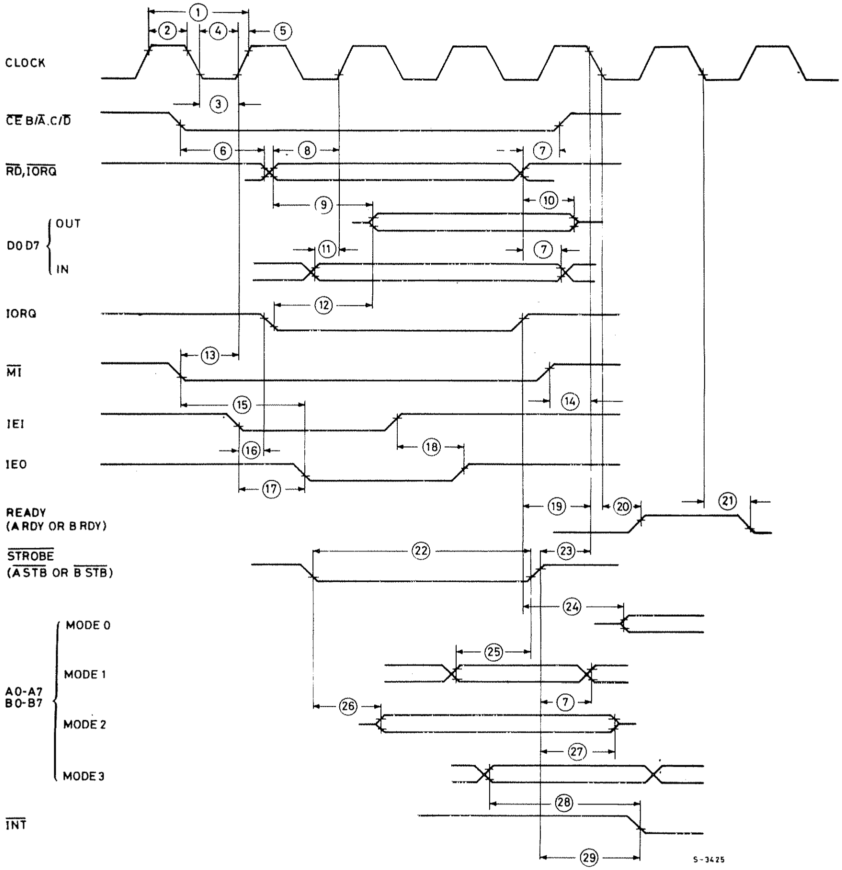
Number	Symbol	Parameter	Min	Max	Unit	Comments
1	TcC	Clock Cycle Time	400	[1]	ns	
2	TcCh	Clock Width (High)	170	2000	ns	
3	TcCL	Clock Width (Low)	170	2000	ns	
4	TfC	Clock Fall Time		30	ns	
5	TrC	Clock Rise Time		30	ns	
6	TsCS(RI)	$\overline{CE}$, B/$\overline{A}$, C/E to $\overline{RD}$, $\overline{IORQ}$ ↓ Setup Time	50		ns	[6]
7	Th	Any Hold Time for specified Setup Time	0		ns	
8	TsRI(C)	$\overline{RD}$, $\overline{IORQ}$ to Clock ↑ Setup Time	115		ns	
9	TdRI(DO)	$\overline{RD}$, $\overline{IORQ}$ ↓ to Data Out Delay		430	ns	[2]
10	TdRI(DOr)	$\overline{RD}$, $\overline{IORQ}$ ↑ to Data Out Float Delay		160	ns	
11	TsDI(C)	Data In to Clock ↑ Setup Time	50		ns	CL = 50 pF
12	TdIO(DOI)	$\overline{IORQ}$ ↓ to Data Out Delay (INTA Cycle)	340		ns	[3]
13	TsM1(Cr)	$\overline{M1}$ ↓ to Clock ↑ Setup Time	210		ns	
14	TsM1(Cf)	$\overline{M1}$ ↑ to Clock ↓ Setup Time ($\overline{M1}$ Cycle)	0		ns	
15	TdM1(IEO)	$\overline{M1}$ ↓ to IEO ↓ Delay (interrupt immediately preceding $\overline{M1}$ ↓)		300	ns	[5] See Note A
16	TsIEI(IO)	IEI to IORQ ↓ Setup Time (INTA Cycle)	140		ns	See Note A
17	TdIEI(IEO)	IEI ↓ to IEO ↓ Delay		190	ns	[5] CL = 50 pF
18	TdIEI(IIOr)	IEI ↑ to IEO ↑ Delay (after ED Decode)		210	ns	[5]
19	TsIO(C)	$\overline{IORQ}$ ↑ to Clock ↓ Setup Time (To Activate READY on Next Clock Cycle)	220		ns	
20	TdC(RDYr)	Clock ↓ to READY ↑ Delay	200		ns	[5] CL = 50 pF
21	TdC(RDYf)	Clock ↓ to READY ↓ Delay	150		ns	[5]
22	TwSTB	STROBE Pulse Width	150 [4]		ns	
23	TsSTB(C)	STROBE ↑ to Clock ↓ Setup Time (To Activate READY on Next Clock Cycle)	220		ns	
24	TdIO(PD)	$\overline{IORQ}$ ↑ to PORT data stable Delay (Mode 0)		200	ns	[5]
25	TsPD(STB)	PORT DATA to STROBE ↑ Setup Time (Mode 1)	260		ns	
26	TdSTB(PD)	STROBE ↓ to PORT DATA Stable (Mode 2)		230	ns	[5]
27	TdSTB(PDz)	STROBE ↑ to PORT DATA Float Delay (Mode 2)		200	ns	CL = 50 pF
28	TdPD(INT)	PORT DATA Match to INT ↓ Delay (Mode 3)		540	ns	
29	TdSTB(INT)	STROBE ↑ to INT ↓ Delay		490	ns	

Notes
A 2 5 TcC > (N-2) TdIEI (IEOG) + TdM1(IEO) + TsIEI(IO) + TTL Buffer Delay, if any
B M1 Must be active for a minimum of 2 clock cycles to reset the PIO
[1] TcC = TwCh + TwCl + TrC + TfC
[2] Increase TdRI(DO) by 10 nsec for each 50 pF increase in loading up to 200 pF max
[3] Increase TdIO(DOT) by 10 nsec for each 60 pF increase in loading up to 200 pF max
[4] For Mode 2 TwSTB > TsPD(STB)
[5] Increase these values by 2 nsec for each 10 pF increase in loading up to 100 pF max
[6] TsCS(RI) may be reduced However the time subtracted from TsCS(RI) will be added to TdRI(DO)

A.C. Timing Diagram

Timing measurements are made at the following voltages, unless otherwise specified:

	"1"	"0"
CLOCK	V_{CC}-0.6V	0.45V
OUTPUT	2 V	0.8V
INPUT	2 V	0.8V
FLOAT	ΔV	±0.5V



Absolute Maximum Ratings

Temperature Under Bias	Specified operating range
Storage Temperature	-65°C to +150°C
Voltage On Any Pin with Respect to Ground	-0.3V to +7V
Power Dissipation	0.6W

Note: All AC and DC characteristics remain the same for the military grade parts except I_{cc}.
I_{cc}= 130 mA

* Comment
Stresses above those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

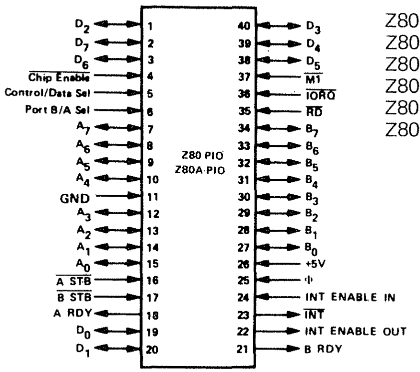
Z80-PIO and Z80A-PIO D.C. Characteristics

T_A= 0°C to 70°C, V_{cc}= +5V ± 5%, unless otherwise noted

Symbol	Parameter	Min.	Max.	Unit	Test Condition
V_{ILC}	Clock Input Low Voltage	-0.3	0.45	V	
V_{IHC}	Clock Input High Voltage	V_{cc}-0.6	V_{cc}+0.3	V	
V_{IL}	Input Low Voltage	-0.3	0.8	V	
V_{IH}	Input High Voltage	2	Vcc	V	
V_{OL}	Output Low Voltage		0.4	V	I_{OL} = 2.0 mA
V_{OH}	Output High Voltage	2.4		V	I_{OH} · 250 µA
I_{CC}	Power Supply Current		70	mA	
I_{LI}	Input Leakage Current		10	µA	V_{IN} = 0 to Vcc
I_{LOH}	Tri-State Output Leakage Current in Float		10	µA	V_{OUT} = 2.4 to Vcc
I_{LOL}	Tri-State Output Leakage Current in Float		-10	µA	V_{OUT} = 0.4 V
I_{LD}	Data Bus Leakage Current in Input Mode		±10	µA	$0 \leqslant V_{IN} \leqslant Vcc$
I_{OHD}	Darlington Drive Current	-1.5		mA	V_{OH} = 1.5 V Port B Only

Z 80-PIO
Z 80A-PIO

PIN CONNECTIONS

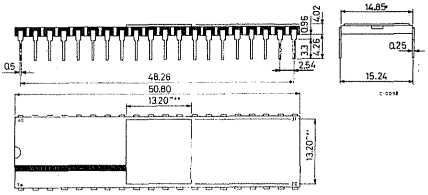


ORDERING NUMBERS:

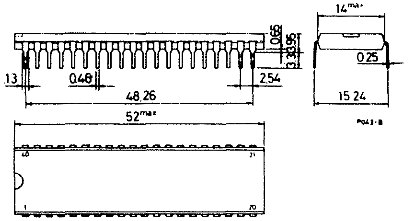
Z80PIO	D1	for dual in-line ceramic package (metal-seal)
Z80PIO	B1	for dual in-line plastic package
Z80APIO	D1	for dual in-line ceramic package (metal-seal)
Z80APIO	B1	for dual in-line plastic package
Z80PIO	F1	for dual in-line ceramic package (frit-seal)
Z80APIO	F1	for dual in-line ceramic package (frit-seal)

MECHANICAL DATA (dimension in mm)

40-PIN CERAMIC DUAL IN-LINE PACKAGE (METAL-SEAL)



40-PIN PLASTIC DUAL IN-LINE PACKAGE



40-PIN CERAMIC DUAL IN-LINE PACKAGE (FRIT-SEAL)