1. General Description

This EPROM-Based 8-bit micro-controller uses a fully static CMOS design technology to achieve high speed, small size, low power and high noise immunity.

On chip memory includes 1K words EPROM and80 bytes static RAM.

Four comparator inputs with external Vref (not for 18 pin package) are also provided.

2. Features

- ◆ Fully CMOS static design
- ◆ 8-bit data bus
- ◆ On chip EPROM size : 1 K words
- ◆ Internal RAM size : 80 bytes (72 general purpose registers, 8 special registers)
- ◆ 36 single word instructions
- ◆ 14-bit instructions
- ◆ 2-level stacks
- ◆ Operating voltage : 2.3V ~ 6.0 V
- ◆ Operating frequency : 0 ~ 20 MHz
- ◆ The most fast execution time is 200 ns under 20 MHz in all single cycle instructions except the branch instruction
- ◆ Addressing modes include direct, indirect and relative addressing modes
- ◆ Power-on Reset (POR), only available while PED is Disable
- ◆ 4 Channel comparator
- ◆ Power edge-detector Reset
- ◆ Sleep Mode for power saving
- ◆ 8-bit real time clock/counter(RTCC) with 8-bit programmable prescaler
- ◆ 4 types of oscillator can be selected by programming option:
  RC—Low cost RC oscillator
  LFXT—Low frequency crystal oscillator
  XTAL—Standard crystal oscillator
  HFXT—High frequency crystal oscillator
- ◆ 4 oscillator start-up time can be selected by programming option:
  150 μs, 20 ms, 40 ms, 80 ms
- ◆ On-chip RC oscillator based Watchdog Timer(WDT) can be operated freely
- ◆ 12 I/O(for 18 pins package),14 I/O(for 20 pins package),16 I/O(for 22/24 pins package) pins with their own independent direction control

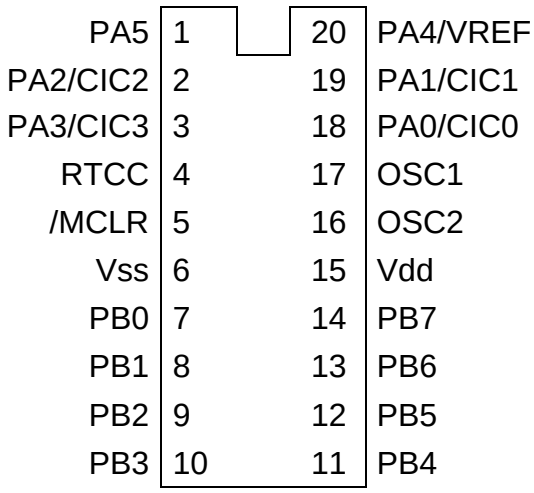
3. Applications

The application areas of this MDT10P22 range from appliance motor control and high speed automotive to low power remote transmitters/receivers, pointing devices, and telecommunications processors, such as Remote controller, small instruments, chargers, toy, automobile and PC peripheral … etc

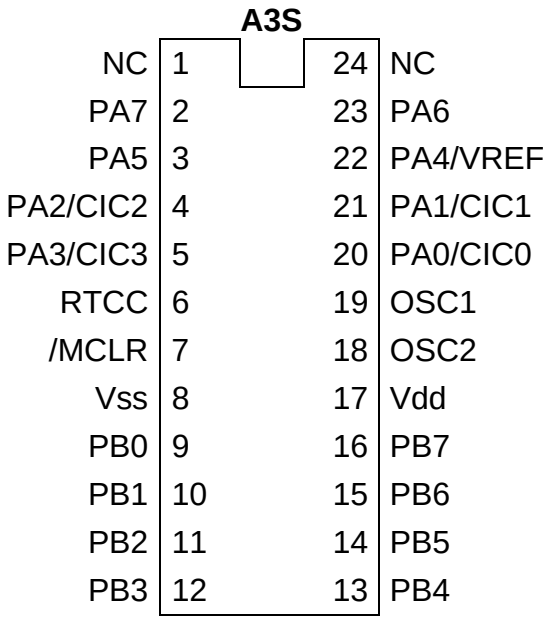
4. Pin Assignment

※ A1 ：20PINS, A2 ：22PINS,
A3 ：24PINS, A5 :18 PINS
※P －PDIP,S －SOP, K －SKINNY

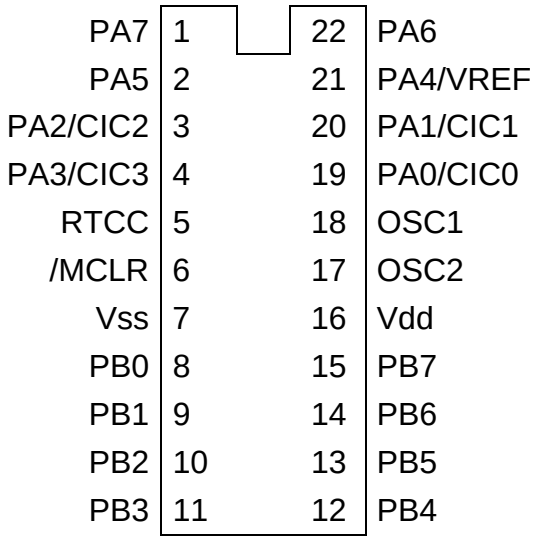
A1P,A1S



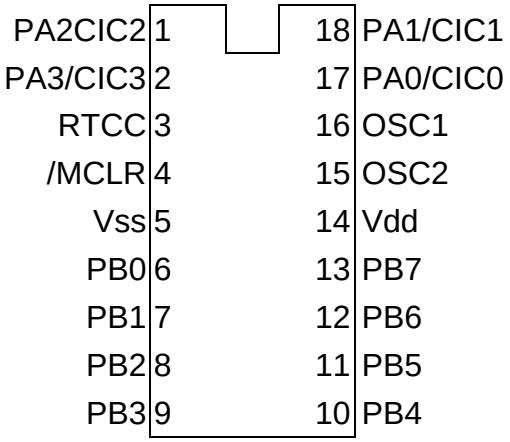
A3S



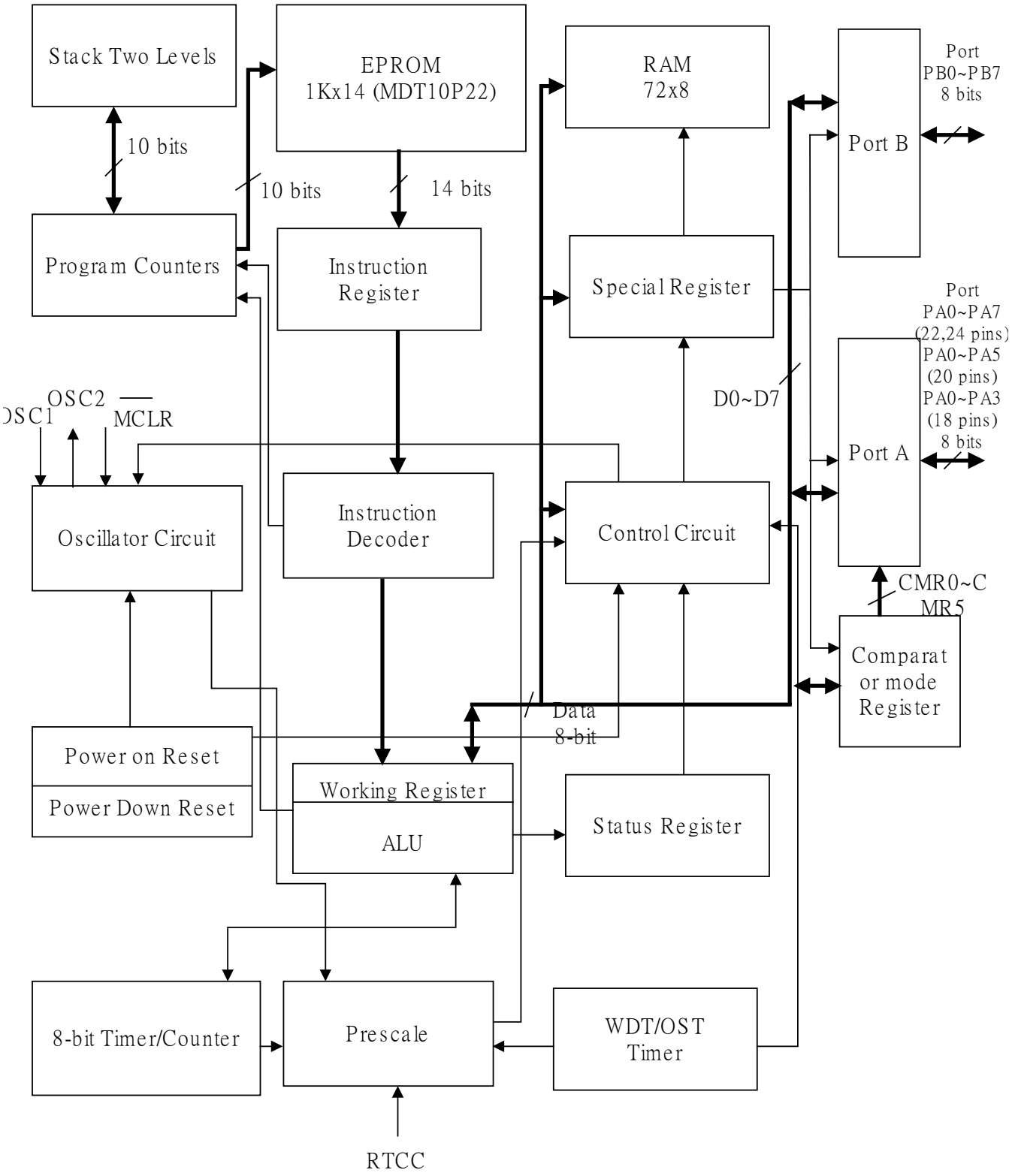
A2K



A5P,A5S



5. Block Diagram



6. Pin Function Description

Pin Name	I/O	Function Description
PA0~PA7	I/O	PA0~PA3 : TTL input level or comparator input PA4 : TTL input level or comparator VREF input PA5~PA7 : TTL input level
PB0~PB7	I/O	Port B, TTL input level
RTCC	I	Real Time Clock/Counter, Schmitt Trigger input levels
/MCLR	I	Master Clear, Schmitt Trigger input levels
OSC1	I	Oscillator Input
OSC2	O	Oscillator Output
Vdd		Power supply
Vss		Ground
NC		Unused ,do not connect

7. Memory Map

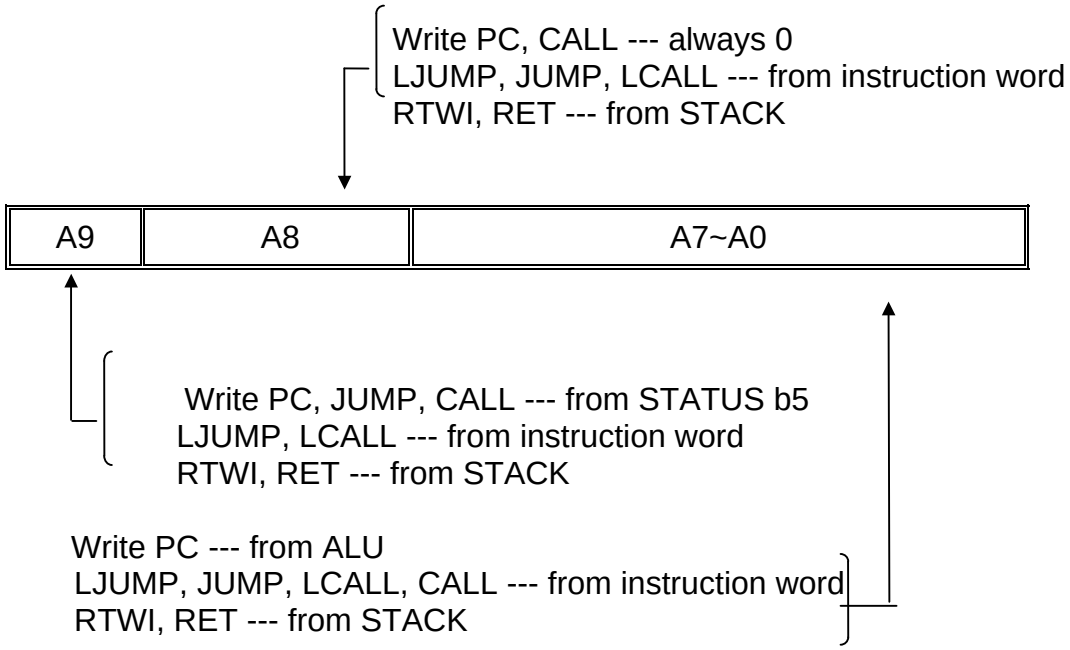
(A) Register Map

Address	Description
00	Indirect Addressing Register
01	RTCC
02	PC
03	STATUS
04	MSR
05	Port A
06	Port B
07	Control register for comparator
08~0F	Internal RAM, General Purpose Register
10~1F	Internal RAM, Memory bank 0
30~3F	Internal RAM, Memory bank 1
50~5F	Internal RAM, Memory bank 2
70~7F	Internal RAM, memory bank 3

(1) IAR (Indirect Address Register) : R0

(2) RTCC (Real Time Counter/Counter Register) : R1

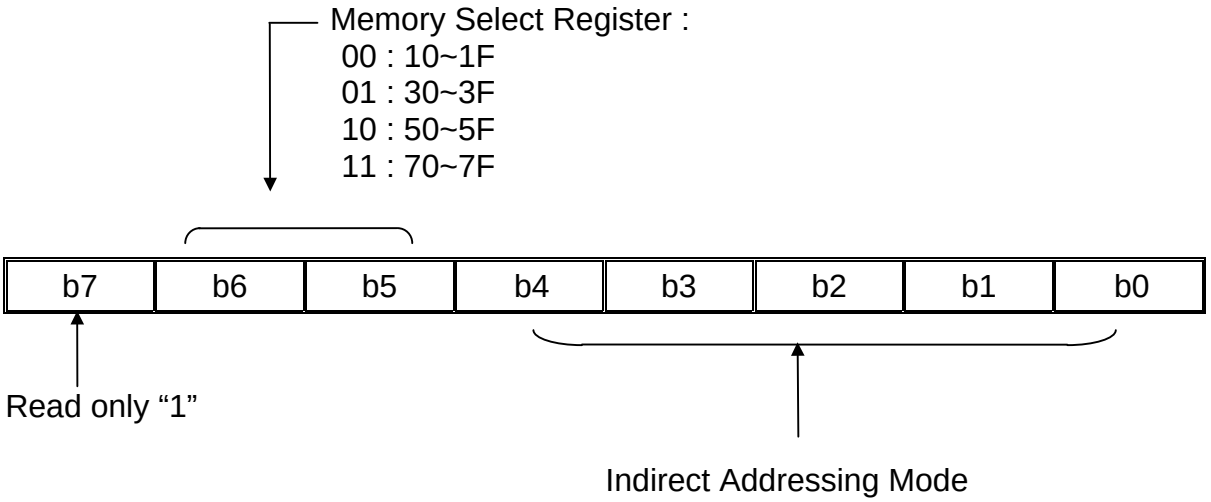
(3) PC (Program Counter) : R2



(4) STATUS (Status register) : R3

Bit	Symbol	Function
0	C	Carry bit
1	HC	Half Carry bit
2	Z	Zero bit
3	PF	Power loss Flag bit
4	TF	Time overflow Flag bit
5	page	ROM Page select bit : 00 : 000H --- 1FFH 01 : 200H --- 3FFH
7	——	General purpose bit

(5) MSR (Memory Select Register) : R4



(6) PORT A : R5

PA7~PA0, I/O Register for 22, 24 pins
PA5~PA0, I/O Register for 20 pins
PA3~PA0, I/O Register for 18 pins

(7) PORT B : R6

PB7~PB0, I/O Register

(8) CMR(Comparator Mode Register) : R7

Bit	Function
0	0: Define PA0 as TTL input
	1: Define PA0 as comparator input
1	0: Define PA1 as TTL input
	1: Define PA1 as comparator input
2	0: Define PA2 as TTL input
	1: Define PA2 as comparator input
3	0: Define PA3 as TTL input
	1: Define PA3 as comparator input
5:4	Reference Voltage select
	00: 1/4 VDD
	01: 1/2 VDD
	10: 3/4 VDD
	11: VREF (External pin and PA4 must be set to inpu
_7:6	Register bits

(9) TMR (Time Mode Register)

Bit	Symbol	Function		
		Prescaler Value	RTCC rate	WDT rate
2—0	PS2—0	0 0 0	1 : 2	1 : 1
		0 0 1	1 : 4	1 : 2
		0 1 0	1 : 8	1 : 4
		0 1 1	1 : 16	1 : 8
		1 0 0	1 : 32	1 : 16
		1 0 1	1 : 64	1 : 32
		1 1 0	1 : 128	1 : 64
		1 1 1	1 : 256	1 : 128
3	PSC	Prescaler assignment bit : 0 — RTCC 1 — Watchdog Timer		
4	TCE	RTCC signal Edge : 0 — Increment on low-to-high transition on RTCC pin 1 — Increment on high-to-low transition on RTCC pin		
5	TCS	RTCC signal set : 0 — Internal instruction cycle clock 1 — Transition on RTCC pin		

(10) CPIO A, CPIO B (Control Port I/O Mode Register)

The CPIO register is “write-only”

＝“0”, I/O pin in output mode;

＝“1”, I/O pin in input mode.

(11) EPROM Option by writer programming :

A. FIRST WORD

Oscillator Type	Oscillator Start-up Time
RC Oscillator	150 μs
LFXT Oscillator	20 ms
XTAL Oscillator	40 ms
HFXT Oscillator	80 ms

Watchdog Timer control
Watchdog timer disable all the time
Watchdog timer enable all the time

Power Edge Detect
PED Disable
PED Enable

Security bit
Security Disable
Security Enable

(B) Program Memory

Address	Description
000- 3FF	Program memory
3FF	The starting address of the power on, external reset or WDT

8. Reset Condition for all Registers

Register	Address	Power-On Reset	/MCLR Reset	WDT Reset
CPIO A	— —	1111 1111	1111 1111	1111 1111
CPIO B	— —	1111 1111	1111 1111	1111 1111
TMR	— —	--11 1111	--11 1111	--11 1111
IAR	00h	—	—	—
RTCC	01h	xxxx xxxx	uuuu uuuu	uuuu uuuu
PC	02h	1111 1111	1111 1111	1111 1111
STATUS	03h	0001 1xxx	000# #uuu	000# #uuu
MSR	04h	100x xxxx	100u uuuu	1uuu uuuu
PORT A	05h	xxxx xxxx	uuuuuuuu	uuuu uuuu
PORT B	06h	xxxx xxxx	uuuu uuuu	uuuu uuuu
CMR	07h	0000 0000	uuuu uuuu	uuuu uuuu

Note : u＝unchanged, x＝unknown, - ＝unimplemented, read as “0”
#＝value depends on the condition of the following table

Condition	Status: bit 4	Status: bit 3
/MCLR reset (not during SLEEP)	U	u
/MCLR reset during SLEEP	1	0
WDT reset (not during SLEEP)	0	1
WDT reset during SLEEP	0	0

9. Instruction Set

Instruction Code	Mnemonic Operands	Function	Operating	Status
010000 00000000	NOP	No operation	None	
010000 00000001	CLRWT	Clear Watchdog timer	0→WT	TF, PF
010000 00000010	SLEEP	Sleep mode	0→WT, stop OSC	TF, PF
010000 00000011	TMODE	Load W to TMODE register	W→TMODE	None
010000 00000100	RET	Return	Stack→PC	None
010000 00000rrr	CPIO R	Control I/O port register	W→CPIO r	None
010001 1rrrrrrr	STWR R	Store W to register	W→R	None
011000 trrrrrrr	LDR R, t	Load register	R→t	Z
111010 iiiiiiii	LDWI I	Load immediate to W	I→W	None
010111 trrrrrrr	SWAPR R, t	Swap halves register	[R(0~3)↔R(4~7)] →t	None
011001 trrrrrrr	INCR R, t	Increment register	R + 1→t	Z
011010 trrrrrrr	INCRSZ R, t	Increment register, skip if zero	R + 1→t	None
011011 trrrrrrr	ADDWR R, t	Add W and register	W + R→t	C, HC, Z
011100 trrrrrrr	SUBWR R, t	Subtract W from register	R – W→t (R+/W+1→t)	C, HC, Z
011101 trrrrrrr	DECR R, t	Decrement register	R – 1→t	Z
011110 trrrrrrr	DECRSZ R, t	Decrement register, skip if zero	R – 1→t	None
010010 trrrrrrr	ANDWR R, t	AND W and register	R ∩ W→t	Z
110100 iiiiiiii	ANDWI i	AND W and immediate	i ∩ W→W	Z
010011 trrrrrrr	IORWR R, t	Inclu. OR W and register	R ∪ W→t	Z
110101 iiiiiiii	IORWI i	Inclu. OR W and immediate	i ∪ W→W	Z
010100 trrrrrrr	XORWR R, t	Exclu. OR W and register	R ⊕ W→t	Z
110110 iiiiiiii	XORWI i	Exclu. OR W and immediate	i ⊕ W→W	Z
011111 trrrrrrr	COMR R, t	Complement register	/R→t	Z
010110 trrrrrrr	RRR R, t	Rotate right register	R(n) →R(n-1), C →R(7), R(0)→C	C
010101 trrrrrrr	RLR R, t	Rotate left register	R(n)→r(n+1), C→R(0), R(7)→C	C
010000 1xxxxxxx	CLRW	Clear working register	0→W	Z
010001 0rrrrrrr	CLRR R	Clear register	0→R	Z
0000bb brrrrrrr	BCR R, b	Bit clear	0→R(b)	None

Instruction Code	Mnemonic Operands	Function	Operating	Status
0010bb brrrrrrr	BSR R, b	Bit set	1→R(b)	None
0001bb brrrrrrr	BTSC R, b	Bit Test, skip if clear	Skip if R(b)=0	None
0011bb brrrrrrr	BTSS R, b	Bit Test, skip if set	Skip if R(b)=1	None
100nnn nnnnnnnn	LCALL n	Long CALL subroutine	n→PC, PC+1→ Stack	None
101nnn nnnnnnnn	LJUMP n	Long JUMP to address	n→PC	None
110000 nnnnnnnn	CALL n	Call subroutine	n→PC, PC+1→ Stack	None
110001 iiiiiiii	RTWI i	Return, place immediate to W	Stack→PC,i→W	None
11001n nnnnnnnn	JUMP n	JUMP to address	n→PC	None

Note :

W	:	Working register	b	:	Bit position
WT	:	Watchdog timer	t	:	Target
TMODE	:	TMODE mode register		0	: Working register
CPIO	:	Control I/O port register		1	: General register
TF	:	Timer overflow flag	R	:	General register address
PF	:	Power loss flag	C	:	Carry flag
PC	:	Program Counter	HC	:	Half carry
OSC	:	Oscillator	Z	:	Zero flag
Inclu.	:	Inclusive ‘∪’	/	:	Complement
Exclu.	:	Exclusive ‘⊕’	x	:	Don’t care
AND	:	Logic AND ‘∩’	i	:	Immediate data (8 bits)
			n	:	Immediate address

10. Electrical Characteristics

(Operating temperature at 25℃).

Sym	Description	Condition	Min	Typ	Max	Unit
Vdd	Operating voltage		2.3		6.0	V
V_{IL}	Input Low Voltage					
	PA, PB	Vdd=5V	-0.6		1.0	V
	RTCC, /MCLR	Vdd=5V	-0.6		1.0	V
V_{IH}	Input high Voltage					
	PA, PB	Vdd=5V	2.0		Vdd	V
	RTCC, /MCLR	Vdd=5V	3.3		Vdd	V
I_{IL}	Input leakage current	Vdd=5V			+/-1	μA
V_{OL}	Output Low Voltage					
	PA, PB	Vdd=5V, I_{OL}=20mA		0.5		V
		Vdd=5V, I_{OL}=5mA		0.1		V

Sym	Description	Condition	Min	Typ	Max	Unit
V_{OH}	Output High Voltage PA, PB	 Vdd=5V, I_{OH}= -20mA Vdd=5V, I_{OH}= -5mA		 3.8 4.5		 V V
I_{slp}	Sleep current (WDT disable)	V_{dd} = 2.3 ~ 6.0 V		0.1	1.0	μA
I_{slp}	Sleep current (WDT enable)	V_{dd} = 2.3 V V_{dd} = 3.0 V V_{dd} = 4.0 V V_{dd} = 5.0 V V_{dd} = 6.0 V		1 3 6 11 17		μA μA μA μA μA
V_{pr}	Power Edge-detector Reset Voltage		1.1		1.3	V
Twdt	The basic WDT time-out cycle time	V_{dd} = 2.3 V V_{dd} = 3.0 V V_{dd} = 4.0 V V_{dd} = 5.0 V V_{dd} = 6.0 V		25.2 22.4 20.4 18.8 18.0		mS mS mS mS mS
T_{FLT}	/MCLR filter	V_{dd} = 5.0 V		600		nS
Icc	Comparator Supply current (one comparator)	Vdd=5.0v		15		μA
Vref	Input reference voltage	Vdd=2.5v ~6.0v			Vdd-0.8 v	V
 --- 	Comparator Response time V-=Vdd/4, V+=V- ± 0.2v V-=Vdd/2, V+=V- ± 0.2v V-=Vdd3/4, V+=V- ± 0.2v V-=VDD-0.8,V+=V± 0.2v	Vdd=5.0v , V- = Vref V+ = (PA0~PA3)		 8 8 8 8		 μS μS μS μS

11. Operating Current

Temperature＝25 ℃, the typical value as followings :

11.1 OSC Type＝RC ; WDT－Enable; @ V_{dd}＝5.0 V ; PED=Disable

Cext. (F)	Rext. (Ohm)	Frequency (Hz)	Current (A)
3P	4.7 K	11.2 M	1.2 mA
	10.0 K	5.95 M	655 μA
	47.0 K	1.40M	235 μA
	100.0 K	658 K	165 μA
	300.0 K	225 K	140 μA
	470.0 K	141 K	120 μA
20P	4.7 K	5.45 M	620 μA
	10.0 K	2.75 M	370 μA
	47.0 K	625 K	172 μA
	100.0 K	295 K	140 μA
	300.0 K	100 K	125 μA
	470.0 K	64 K	120 μA
100P	4.7 K	1.77 M	290 μA
	10.0 K	885 K	210 μA
	47.0 K	195 K	145 μA
	100.0 K	92 K	135 μA
	300.0 K	31 K	130 μA
	470.0 K	20 K	125 μA
300P	4.7 K	685 K	190 μA
	10.0 K	337 K	158 μA
	47.0 K	75 K	135 μA
	100.0 K	35 K	130 μA
	300.0 K	12 K	126 μA
	470.0 K	7 K	125 μA

11.2 OSC Type＝LF (OSC1&OSC2 External Cap about 10P);　WDT－Disable ;
PED=Disable

Voltage/Frequency	32 K (EXT100P)	455 K (EXT50P)	1 M	Sleep
2.3 V	7.0μA	2.6V@25.0 μA	40μA	＜1.0 μA
3.0 V	15.0μA	55μA	70μA	＜1.0 μA
4.0 V	35.0μA	90μA	120μA	＜1.0 μA
5.0 V	73.0μA	145μA	185μA	＜1.0 μA
6.0 V	132.0μA	220μA	265μA	＜1.0 μA

11.3 OSC Type＝XT (OSC1&OSC2 EXternal Cap about 10P);　WDT－Enable ；
PED=Disable

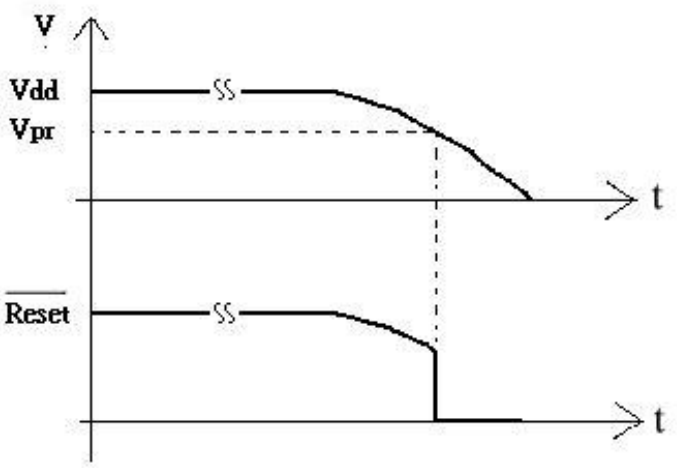
Voltage/Frequency	1 M	4 M	10 M	Sleep
2.1 V	50μA	120μA	290μA	＜1.0 μA
3.0 V	105μA	235μA	500μA	3 μA
4.0 V	215μA	405μA	650μA	6 μA
5.0 V	380μA	600μA	1.3mA	11 μA
6.0 V	650μA	855μA	1.7mA	17 μA

11.4 OSC Type＝HF (OSC1&OSC2 External Cap about 10P);　WDT－Enable ；
PED=Disable

Voltage/Frequency	4 M	10 M	20 M	Sleep
2.1 V	150μA	320μA	X	＜1.0 μA
3.0 V	290μA	550μA	930μA	3 μA
4.0 V	510μA	910μA	1.5mA	6 μA
5.0 V	800μA	1.5mA	2.4mA	11 μA
6.0 V	1.4mA	2.0mA	3.3mA	17 μA

11.5 Power Edge-detector Reset Voltage (Not in Sleep Mode), @ V_{dd}＝5.0 V (PED : Enable)

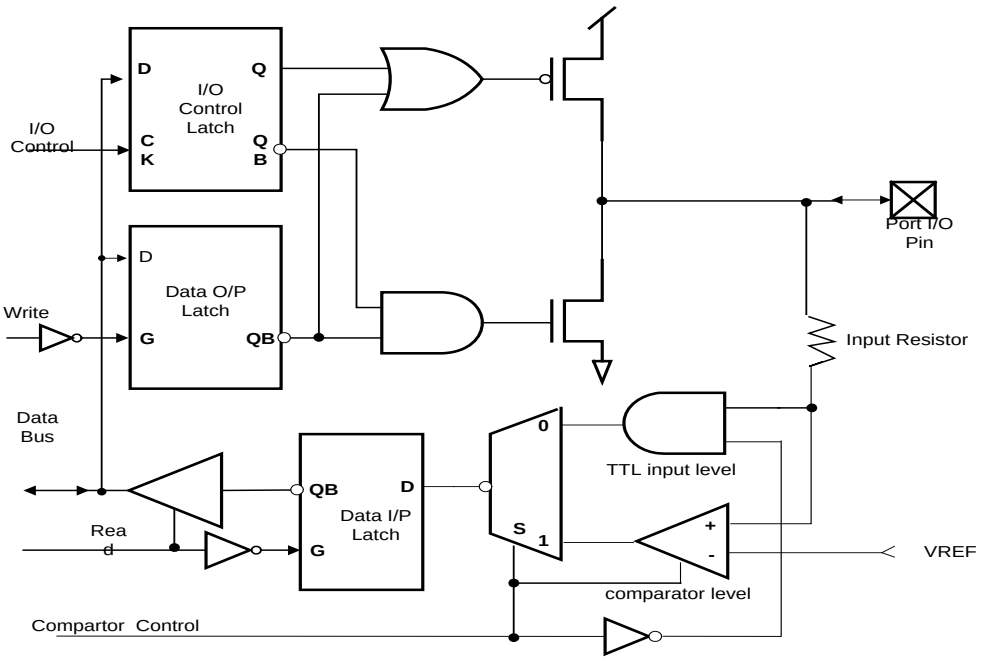
V_{pr}≦1.6~1.8 V　　V_{pr} ： V_{dd} (Power Supply)



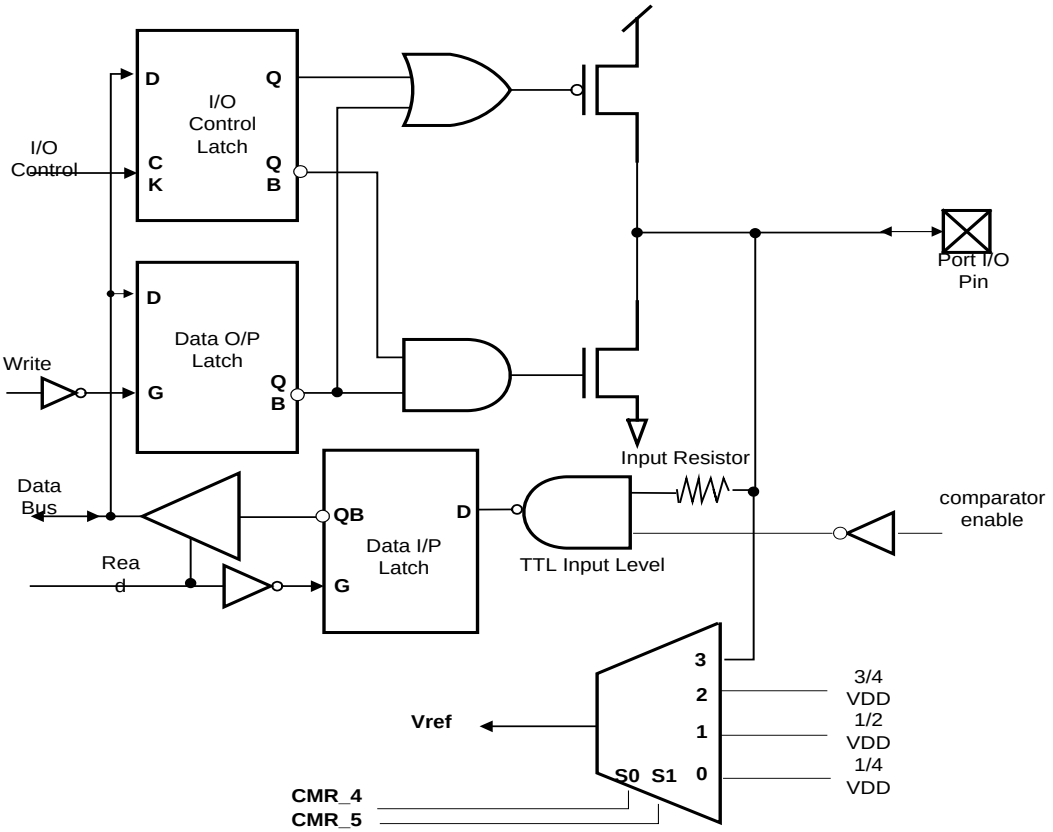
PS. If PED_Enable then Internal Power_on_reset will be off

12. Port A　Equivalent Circuit

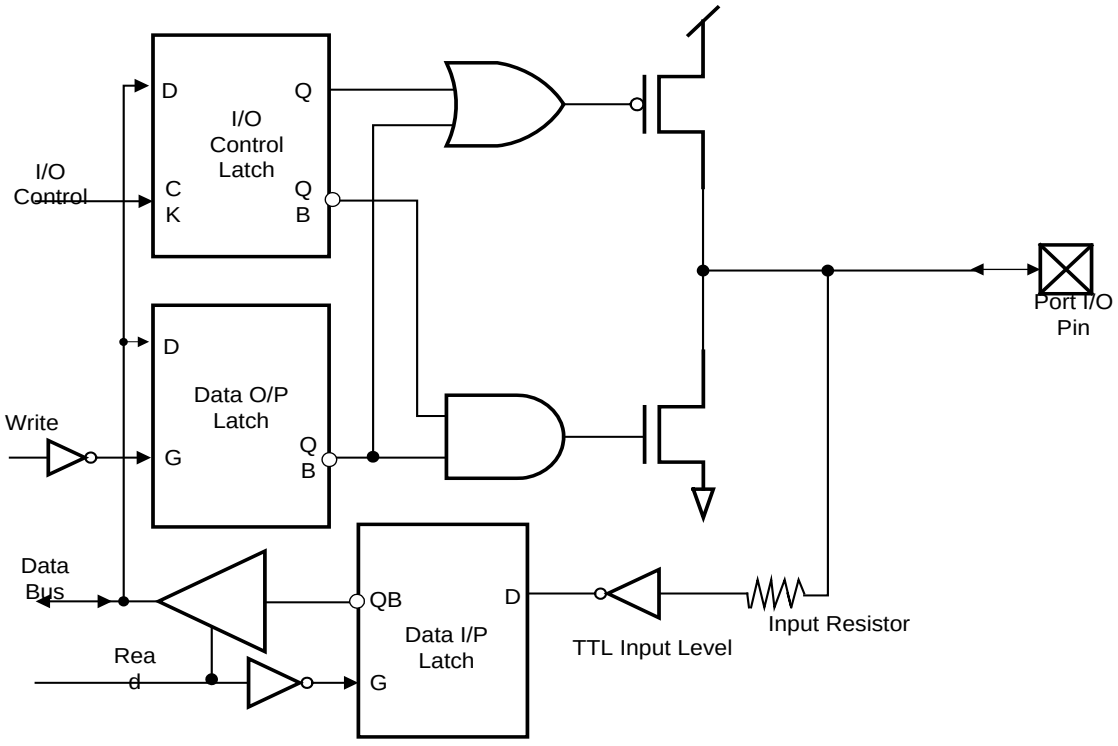
PA0-PA3



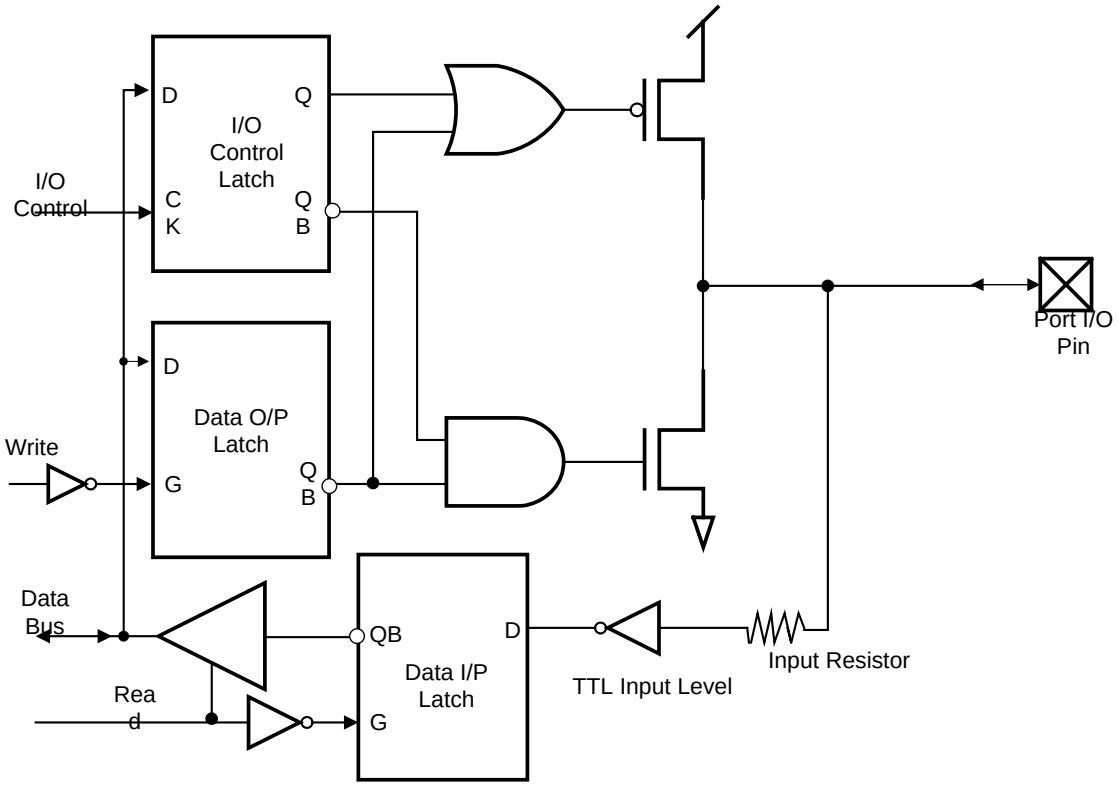
PA4


D
Q
I/O Control Latch
C K
Q B
I/O Control
Port I/O Pin
D
Data O/P Latch
G
Q B
Write
Input Resistor
Data Bus
QB
D
Data I/P Latch
G
Rea d
TTL Input Level
comparator enable
3
2
1
S0 S1
0
Vref
3/4 VDD
1/2 VDD
1/4 VDD
CMR_4
CMR_5

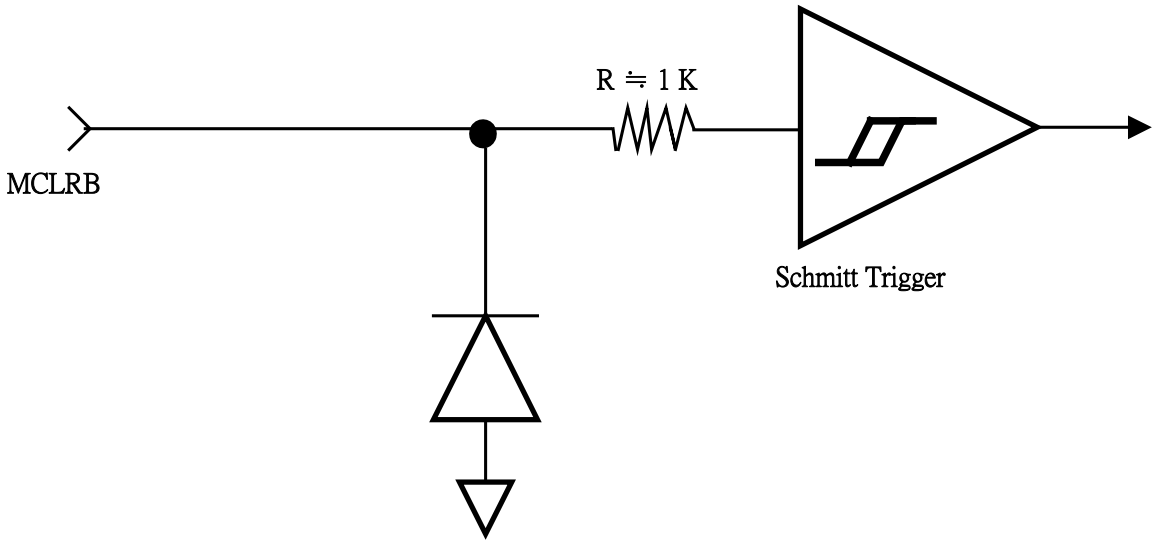
PA5-PA7

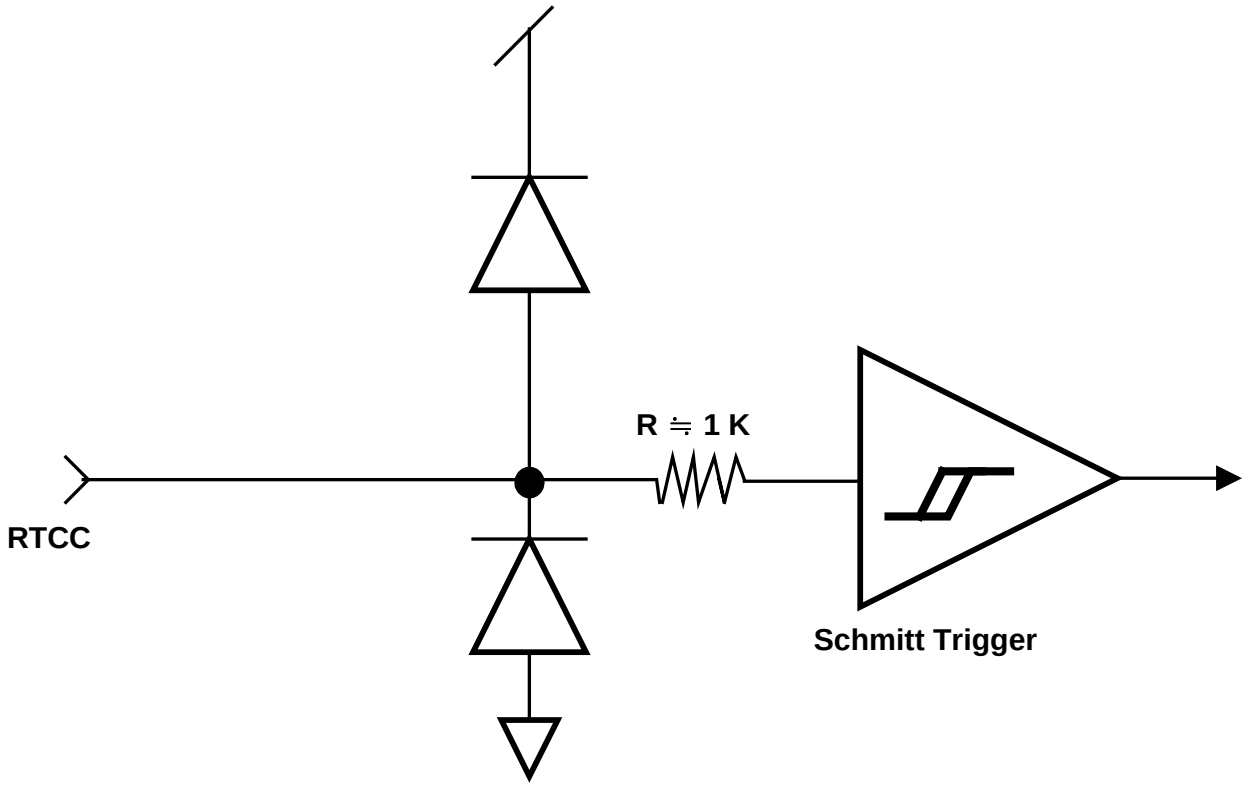

D
Q
I/O Control Latch
C K
Q B
I/O Control
Port I/O Pin
D
Data O/P Latch
G
Q B
Write
Data Bus
QB
D
Data I/P Latch
G
Rea d
TTL Input Level
Input Resistor

Port B Equivalent Circuit



13. MCLRB and RTCC Input Equivalent Circuit

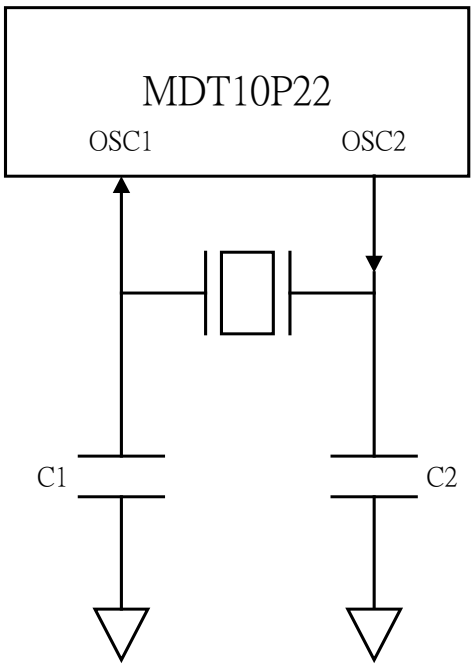




14. External Capacitor Selection For Crystal Oscillator

@ V_{dd} = 5.0 V

Osc. Type	Resonator Freq.	Capacity Range
HF	20 MHz	10 pF ~ 50 pF
	10 MHz	20 pF ~ 50 pF
	4 MHz	10 pF ~ 30 pF
XT	10 MHz	10 pF ~ 50 pF
	4 MHz	10 pF ~ 50 pF
	1 MHz	20 pF ~50 pF
LF	1 MHz	20 pF ~ 30 pF
	455 K	20 pF ~30 pF
	32 K	20 pF ~30 pF



To increase the stability of oscillator and the ability of anti-noise, the above values of the external capacitor are for reference only, but the higher capacitance also increases the start-up time.