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MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

MC33120

Subscriber Loop Interface Circuit

SUBSCRIBER LOOP INTERFACE CIRCUIT (SLIC)

THIN FILM SILICON MONOLITHIC INTEGRATED CIRCUIT

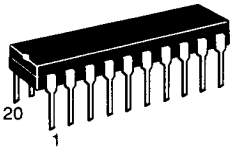
The MC33120 is designed to provide the interface between the 4-wire side of a central office, or PBX, and the 2-wire subscriber line. Interface functions include battery feed, proper loop termination AC impedance, hookswitch detection, adjustable transmit, receive, and transhybrid gains, and single/double fault indication. Additionally the MC33120 provides a minimum of 58 dB of longitudinal balance (4-wire and 2-wire).

The transmit and receive signals are referenced to analog ground, while digital signals are referenced to digital ground, easing the interface to codecs, filters, etc. The 2 status outputs (hookswitch and faults) and the Power Down Input are TTL/CMOS compatible. The Power Down Input permits local shutdown of the circuit.

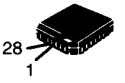
Internal drivers allow the external loop current pass transistors to be standard bipolar transistors (non-Darlington).

The MC33120 is available in a 20 pin DIP and a 28 pin PLCC surface mount package.

- 58 dB Longitudinal Balance Guaranteed; 4-wire and 2-wire
- Transmit, Receive, and Transhybrid Gains Externally Adjustable
- Return Loss Externally Adjustable
- Proper Hookswitch Detection With 30 kΩ Leakage
- Single/Double Fault Indication With Shutdown for Thermal Protection
- Critical Sense Resistors Included Internally
- Standard Power Supplies: – 42 V to – 58 V, and +5.0 V, ±10%
- On-Hook Transmission
- Power Down Input (TTL and CMOS Compatible)
- Operating Ambient Temperature: – 40°C to +85°C
- Available in a 20 Pin DIP and 28 Pin PLCC Package



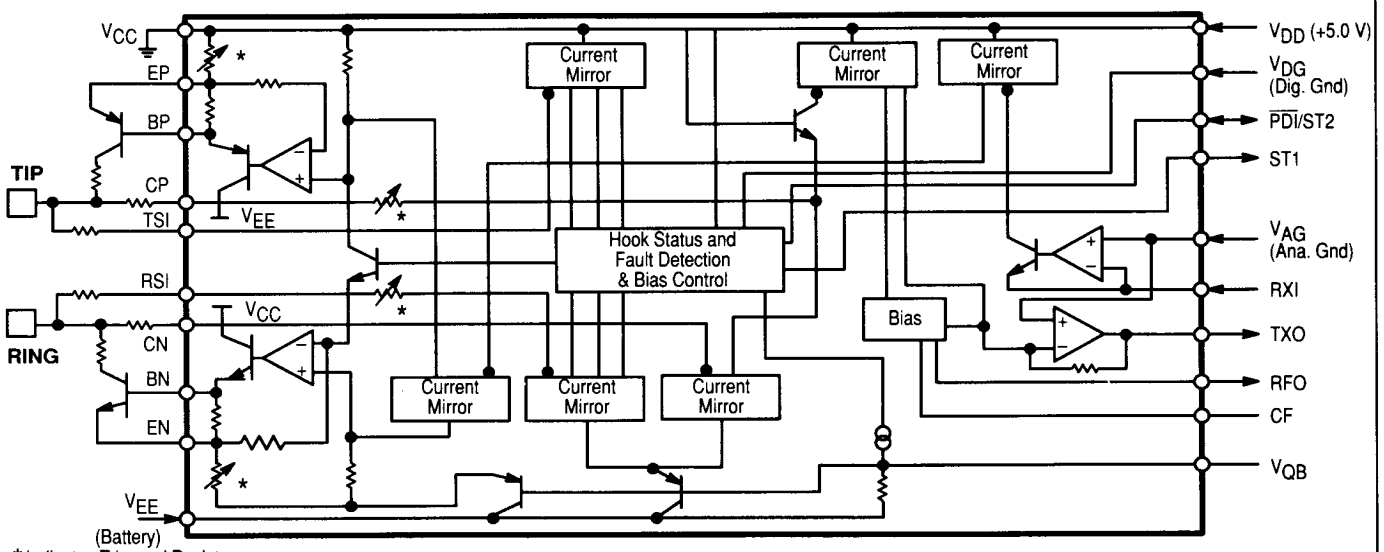
P SUFFIX
PLASTIC PACKAGE
CASE 738



FN SUFFIX
PLCC
CASE 776

ORDERING INFORMATION		
Device	**Temperature Range**	**Package**
MC33120P	– 40° to +85°C	Plastic DIP
MC33120FN		PLCC

SIMPLIFIED BLOCK DIAGRAM



* Indicates Trimmed Resistor

ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	Value	Unit
Supply Voltage with respect to V_{CC} with respect to V_{DG}	 V_{EE} V_{DD}	 – 60, +0.5 – 0.5, +7.0	Vdc
Input Voltage @ PDI, with respect to V_{DG} @ Pins 1–5, 16–20	V_{in}	 – 0.5, +7.0 V_{EE} to V_{CC}	Vdc
Storage Temperature Range	T_{stg}	– 65 to +150	°C
Junction Temperature	T_J	150	°C

Devices should not be operated at these values. The "Recommended Operating Conditions" table provides conditions for actual device operation.

RECOMMENDED OPERATING CONDITIONS

Characteristic	Symbol	Min	Typ	Max	Unit
Supply Voltage (with respect to V_{CC}) (with respect to V_{DG})	 V_{EE} V_{DD}	 – 58 +4.5	 – 48 +5.0	 – 42 +5.5	Vdc
(with respect to V_{CC}) (with respect to V_{CC}) (with respect to V_{AG})	V_{AG} V_{DG}	– 3.0 – 3.0 – 3.0	0 0 0	+10 +7.0 +10	Vdc
(with respect to V_{EE}) (with respect to V_{CC} and V_{AG})	V_{DD}	— +3.5	— —	+63.5 —	Vdc
Loop Current	I_{LOOP}	15	—	50	mA
PDI Input Voltage	V_{PDI}	0	—	V_{DD}	Vdc
Sink Current ST1 ST2	 I_{ST1L} I_{ST2L}	 0 0	 — —	 1.0 1.0	mA
Transmit Signal Level at Tip & Ring Receive Signal Level at V_{RX}	S_{TX} S_{RX}	– 48 – 48	— —	+3.0 +3.0	dBm
Loop Resistance	R_L	0	—	2.0	kΩ
External Transistor Beta	H_{FE}	40	—	500	A/A
Operating Ambient Temperature (See text for derating)	T_A	– 40	—	+85	°C

All limits are not necessarily functional concurrently.

ELECTRICAL CHARACTERISTICS (V_{EE} = – 48 V, V_{DD} = +5.0 V, unless otherwise noted, V_{CC} = V_{AG} = V_{DG} = 0 V, T_A = 25°C, see Figure 1, unless otherwised noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
POWER SUPPLIES					
V_{EE} Current On Hook (R_L > 10 MΩ, V_{EE} = – 58 V) Off Hook (R_L = 0 Ω, V_{EE} = – 58 V)* V_{DD} Current On Hook (R_L > 10 MΩ, V_{DD} = +5.5 V) Off Hook (R_L = 0 Ω, V_{DD} = +5.5 V)	 I_{EEN} I_{EEF} I_{DDN} I_{DDF}	 – 2.7 – 75 — 5.5	 – 1.2 – 58 1.4 9.0	 — – 45 2.7 15	mA
V_{EE} Ripple Rejection f = 1.0 kHz, at V_{TX} (4-wire) f = 1.0 kHz, at Tip/Ring (2-wire) V_{DD} Ripple Rejection f = 1.0 kHz, at V_{TX} (4-wire) f = 1.0 kHz, at Tip/Ring (2-wire)	PSRR 	 40 40 37 37	 62 52 52 48	 — — — —	dB

*Includes loop current.

ELECTRICAL CHARACTERISTICS (V_{EE} = – 48 V, V_{DD} = +5.0 V, unless otherwise noted, V_{CC} = V_{AG} = V_{DG}, T_A = 25°C, see Figure 1)

Characteristic	Symbol	Min	Typ	Max	Unit
LOOP FUNCTIONS					
Loop Current					mA
Maximum (RRF = 4.7 k, R_L = 10 Ω)	I_{LMAX}	41	43	53	
Nominal (RRF = 4.7 k, R_L = 600 Ω)	I_{LOOP}	37	40	48	
Minimum (RRF = 4.7 k, R_L = 1800 Ω)	I_{LMN}	19	21	—	
Battery Feed Resistance (RRF = 4.7 k, R_L = 1800 Ω)*	R_{BF}	475	508	675	Ω
Hookswitch Threshold					kΩ
On-to-Off Hook	R_{NF}	2.0	3.1	—	
Off-to-On Hook	R_{FN}	—	7.0	10	
Fault Detection Threshold					Ω
Ring-to-Ground (R_L = 600 Ω)	R_{RG}	600	660	—	
Tip-to-Battery (R_L = 600 Ω)	R_{TB}	600	660	—	

*Calculated from [(48/I_{LMN}) – 1800]

GAIN LEVELS

Transmit Voltage Gain (CP, CN to TXO)	G_{TX1}	—	0.328	—	V/V
Transmit Voltage Gain (V_{TX}/V_L)					dB
V_L = 0 dBm, f = 1.0 kHz	G_{TX2}	– 0.3	0.0	+0.3	
V_L = 0 dBm, f = 3.4 kHz, with respect to G_{TX2}		– 0.1	0.0	+0.1	
V_L = +3.0 dBm, f = 1.0 kHz, with respect to G_{TX2}		– 0.15	0.0	+0.15	
V_L = – 48 dBm, f = 1.0 kHz, with respect to G_{TX2}		—	±0.1	—	
Transmit Distortion (at Pin 11)	THD_T				%
(f = 300 Hz to 4.0 kHz, – 40 dBm ≤ V_{T-R} ≤ +5.0 dBm)		—	0.05	—	
Receive Current Gain (I_{EP}/I_{RXI})	G_{RX1}	94	102	110	mA/mA
Receive Voltage Gain (V_L/V_{RXI}) (R_L = 600 Ω)					dB
V_{RXI} = 0 dBm, f = 1.0 kHz	G_{RX2}	– 0.3	0.0	+0.3	
V_{RXI} = 0 dBm, f = 3.4 kHz, with respect to G_{RX2}		– 0.1	0.0	+0.1	
V_{RXI} = +3.0 dBm, f = 1.0 kHz, with respect to G_{RX2}		– 0.15	0.0	+0.15	
V_{RXI} = – 48 dBm, f = 1.0 kHz, with respect to G_{RX2}		—	±0.1	—	
Receive Distortion	THD_R	—	0.05	—	%
(f = 300 Hz to 4.0 kHz, – 40 dBm ≤ V_{RXI} ≤ +5.0 dBm)					
Return Loss (Reference = 600 Ω resistive, f = 1.0 kHz)	RL	30	>40	—	dB
Transhybrid Rejection (R_L = 600 Ω, f = 1.0 kHz, Figure 4)	THR	—	44	—	dB

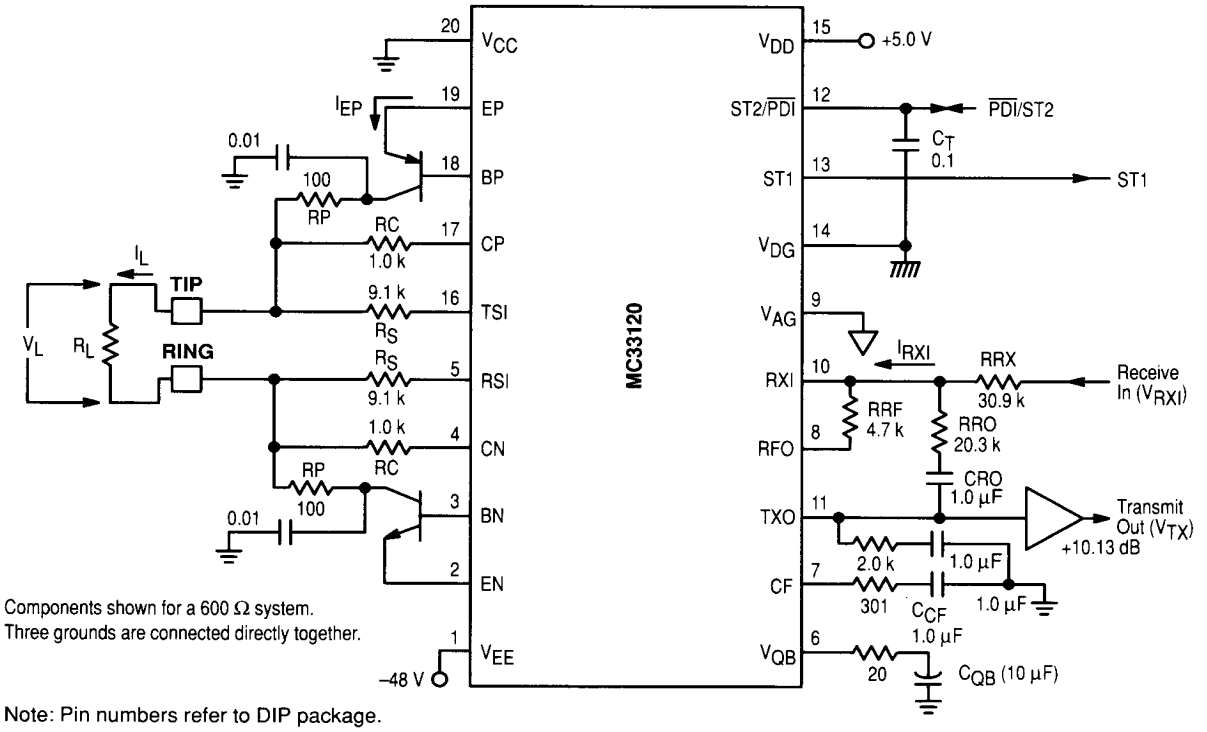
LONGITUDINAL SIGNALS (V_{CM} = 5.12 Vrms, see Figures 1 and 2)

2-Wire Balance, f = 1.0 kHz, Z_{ac} = 600 Ω (@ Tip/Ring)	LB	58	64	—	dB
4-Wire Balance, f = 1.0 kHz, Z_{ac} = 600 Ω (@ V_{TX})		58	64	—	
2-Wire Balance, f = 330 Hz, Z_{ac} = 600 Ω (@ Tip/Ring)		58	64	—	
4-Wire Balance, f = 330 Hz, Z_{ac} = 600 Ω (@ V_{TX})		58	64	—	
2-Wire Balance, f = 3.3 kHz, Z_{ac} = 600 Ω (@ Tip/Ring)		53	60	—	
4-Wire Balance, f = 3.3 kHz, Z_{ac} = 600 Ω (@ V_{TX})		53	60	—	
2-Wire Balance, f = 1.0 kHz, Z_{ac} = 900 Ω (@ Tip/Ring)		—	62	—	
4-Wire Balance, f = 1.0 kHz, Z_{ac} = 900 Ω (@ V_{TX})		—	62	—	
Signal Balance, f = 1.0 kHz (Figure 3)		40	55	—	
Longitudinal Impedance, RS = 9100 Ω	Z_{LONG}	150	180	210	Ω
Maximum Longitudinal Current per side	I_{LM}				mA
f = 1.0 kHz, I_{LOOP} = I_{LMN}, C_T = 0.1 μF		8.5	16	—	

ELECTRICAL CHARACTERISTICS (V_{EE} = – 48 V, V_{DD} = +5.0 V, unless otherwise noted, V_{CC} = V_{AG} = V_{DG}, T_A = 25°C, see Figure 1)

Characteristic	Symbol	Min	Typ	Max	Unit
LOGIC INTERFACE					
ST1 Output Voltage					Vdc
Low (I_{ST1} = 1.0 mA, V_{DD} = 5.5 V)	V_{OL}	V_{DG}	0.17	0.4	
High (I_{ST1} = – 100 µA, V_{DD} = 4.5 V)	V_{OH}	2.4	3.2	—	
ST2 Output Voltage					
Low (I_{ST2} = 1.0 mA, V_{DD} = 5.5 V)	V_{OL}	V_{DG}	0.17	0.4	
High (I_{ST2} = – 100 µA, V_{DD} = 4.5 V)	V_{OH}	2.4	4.3	—	
Time Delay					µs
Hookswitch Closure to ST1 Change	t_{ST11}	—	10	—	
Hookswitch Opening to ST1 Change	t_{ST12}	—	200	—	
Hookswitch Closure to 90% of Loop Current (C_T = 0.1 µF)	t_{HS}	—	19	—	ms
PDI Taken High-to-Low to 10% of Loop Current	t_{ST21}	—	18	—	ms
PDI Taken Low-to-High to 90% of Loop Current	t_{ST22}	—	10	—	µs
PDI Input Current	I_{IH}				µA
V_{PDI} = 3.0 V, R_L = 600 Ω, V_{DD} = 5.0 V		– 1250	– 800	– 300	
V_{PDI} = 0 V, R_L = 600 Ω, V_{DD} = 5.5 V		—	– 800	—	
PDI Input Voltage					V
Low	V_{IL}	V_{DG}	—	0.8	
High	V_{IH}	2.0	—	V_{DD}	
MISCELLANEOUS					
V_{QB} Voltage (V_{QB} – V_{EE})	V_{QB}				Vdc
@ I_L = 20 mA		—	0.82	—	
@ I_L = 40 mA		—	0.95	—	
TXO Offset Voltage (V_{TXO} – V_{AG}) @ R_L = 600 Ω	V_{TXO}	– 400	+30	+400	mVdc
TXO Output Current	I_{TXO}	±275	±800	—	µA pk
RXI Offset Voltage (V_{RXI} – V_{AG}) @ R_L = 600 Ω	V_{RXOS}	—	0.8	—	mVdc
V_{AG} Input Current @ R_L = 600 Ω	I_{VAG}	—	0.2	—	µA
Idle Channel Noise (with C-message filter, R_L = 600 Ω)					dBrnc
@ TXO (Pin 11)	N_{IC4}	—	– 10	—	
@ Tip/Ring	N_{IC2}	—	– 5.0	—	
Thermal Resistance — Junction to Ambient	θ_{JA}				°C/W
(Either package, in still air, soldered to a PC board) (@ T_A = +25°C)		—	62	—	
(@ T_A = +85°C)		—	36	—	

FIGURE 1 — TEST CIRCUIT



Note: Pin numbers refer to DIP package.

FIGURE 2 — LONGITUDINAL BALANCE TEST

(Per IEEE-455)

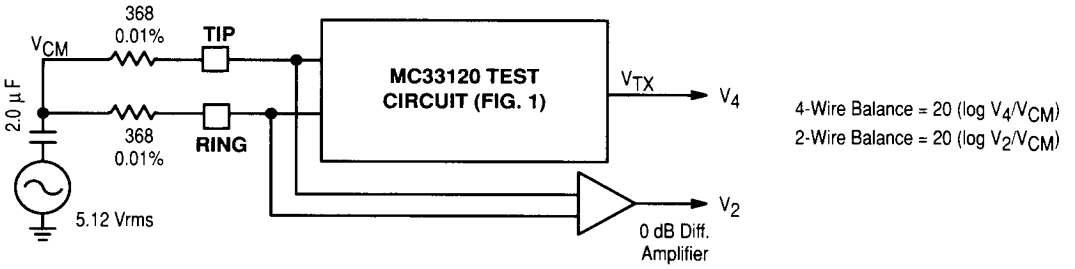


FIGURE 3 — SIGNAL BALANCE TEST

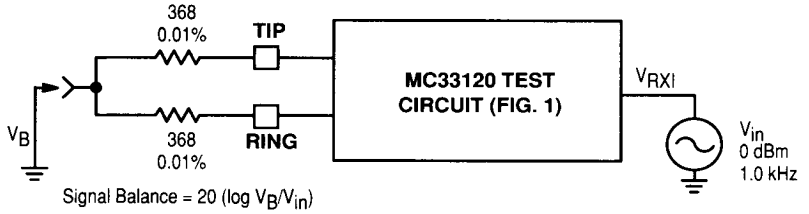
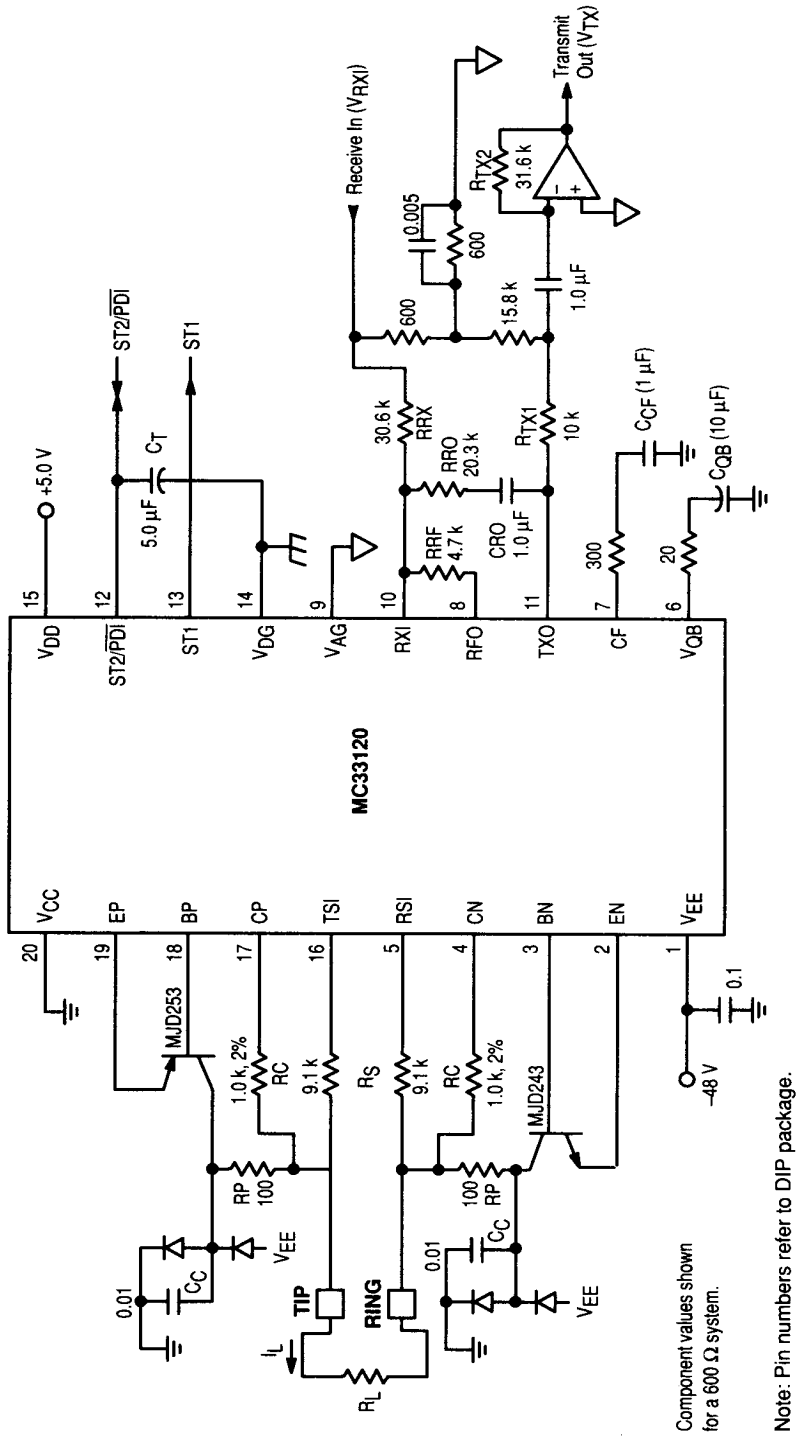


FIGURE 4 — APPLICATION CIRCUIT



Note: Pin numbers refer to DIP package.

PIN DESCRIPTION

Name	Pin		Description
	DIP	PLCC	
V_{CC}	20	28	Connect to noise-free Battery ground. Carries loop current and some bias currents.
EP	19	27	Connect to the emitter of the PNP pass transistor.
BP	18	26	Connect to the base of the PNP pass transistor.
CP	17	24	Connect to TIP through a current limiting protection resistor (R_C). CP is the noninverting input to the internal transmit amplifier (Figure 28). Input impedance is 31 kΩ.
TSI	16	23	Sense input. Connect to TIP through a current limiting protection resistor (R_S) which also sets the longitudinal impedance. Input impedance is ≈100 Ω to V_{CC}.
V_{DD}	15	22	Connect to a +5.0 V, ±10% supply, referenced to digital ground. Powers logic section and provides some bias currents for the loop current drivers.
V_{DG}	14	20	Digital Ground. Reference for ST1, ST2 and V_{DD}. Connect to system digital ground.
ST1	13	18	Status Output (TTL/CMOS). Indicates hook switch status — High when on-hook, low when off-hook, and pulse dialing information. Used with ST2 to indicate fault conditions.
ST2/PDI	12	17	Status output **and** an input (TTL/CMOS). As an output, ST2 can indicate hook status — Low when on-hook, high when off-hook. Used with ST1 to indicate fault conditions. As an input, it can be taken low (when off-hook) to deny subscriber loop current.
TXO	11	16	Transmit voltage output. Amplitude is ≈1/3 that across CP and CN. Nominally capable of 800 μA output current. DC referenced to V_{AG}.
RXI	10	14	Receive current input. Current at this pin is multiplied by 102 at EP and EN to generate loop current. RXI is a virtual ground at V_{AG} level. Current flow is **out** of this pin.
V_{AG}	9	13	Analog ground, reference for TXO and RXI. Connect to system analog ground.
RFO	8	12	A resistor between this pin and RXI sets the maximum loop current and DC feed resistance. Minimum resistor value is 3.3 k (see Figures 5–7).
CF	7	10	A low leakage capacitor between this pin and V_{AG} provides DC and AC signal separation. A series resistor is required for battery supply turn-on/off transient protection (Figure 4).
V_{QB}	6	8	Quiet Battery. A capacitor between V_{QB} and V_{CC} filters noise and ripple from V_{EE}, providing a quiet battery source for the speech amplifiers. A series resistor is required for battery supply turn-on/off transient protection (Figure 4).
RSI	5	7	Sense input. Connect to RING through a current limiting protection resistor which also sets the longitudinal impedance. Input impedance is ≈100 Ω to V_{QB}.
CN	4	6	Connect to RING through a current limiting protection resistor. CN is the inverting input to the internal transmit amplifier (Figure 28). Input impedance is 31 kΩ.
BN	3	4	Connect to the base of the NPN pass transistor.
EN	2	3	Connect to the emitter of the NPN pass transistor.
V_{EE}	1	2	Connect to battery voltage. Nominally – 48 V, it can range from – 42 to – 58 V.

(Pins 1, 5, 9, 11, 15, 19, 21, and 25 are not internally connected on the PLCC package).

FIGURE 5 — LOOP CURRENT versus LOOP RESISTANCE AND RRF

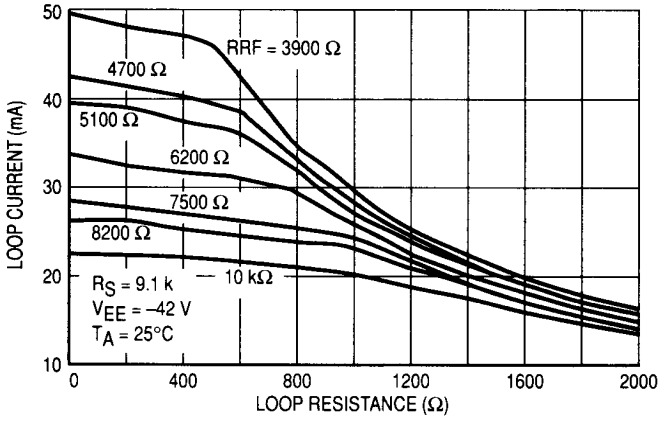


FIGURE 6 — LOOP CURRENT versus LOOP RESISTANCE AND RRF

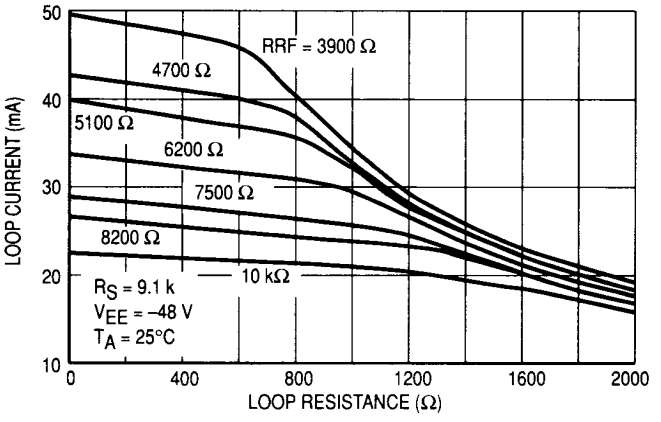


FIGURE 7 — LOOP CURRENT versus LOOP RESISTANCE AND RRF

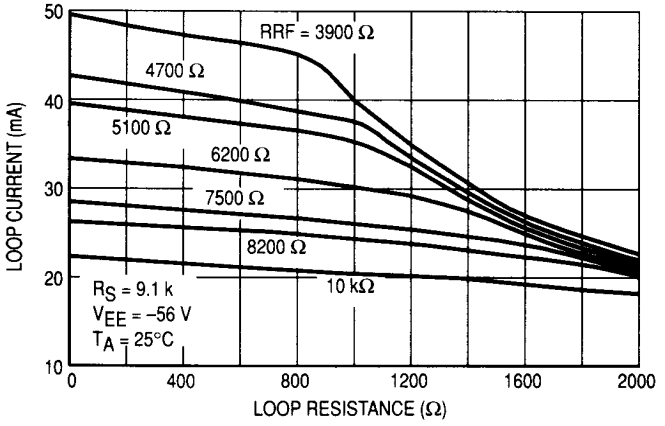


FIGURE 8 — OFF-HOOK TO ON-HOOK THRESHOLD versus RRF

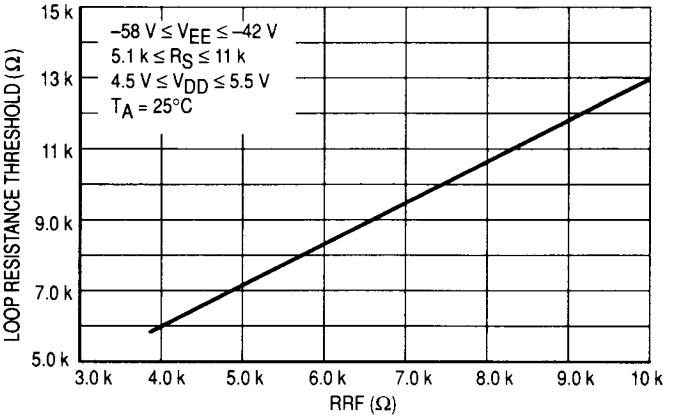


FIGURE 9 — ON-HOOK TO OFF-HOOK THRESHOLD versus R_S

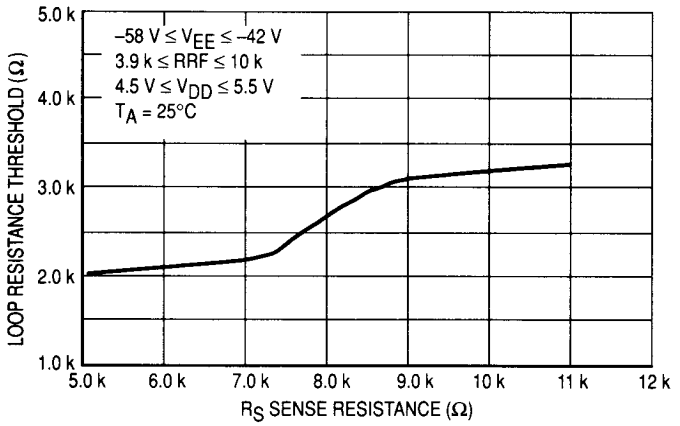


FIGURE 10 — I_{DD} versus LOOP CURRENT

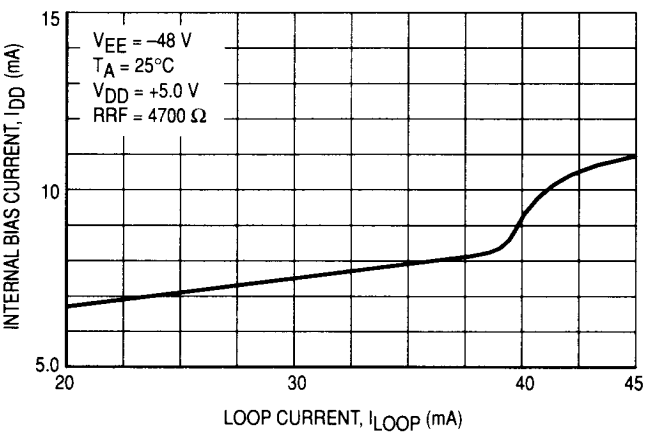


FIGURE 11 — FAULT THRESHOLD (ON-HOOK) versus R_S

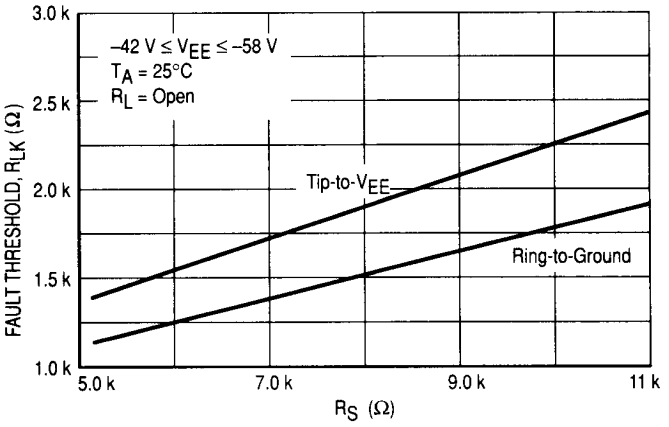


FIGURE 12 — FAULT THRESHOLD (OFF-HOOK) versus LOOP RESISTANCE

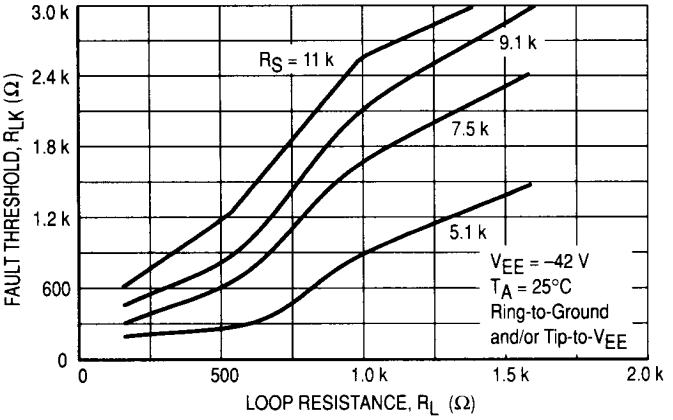


FIGURE 13 — FAULT THRESHOLD (OFF-HOOK) versus LOOP RESISTANCE

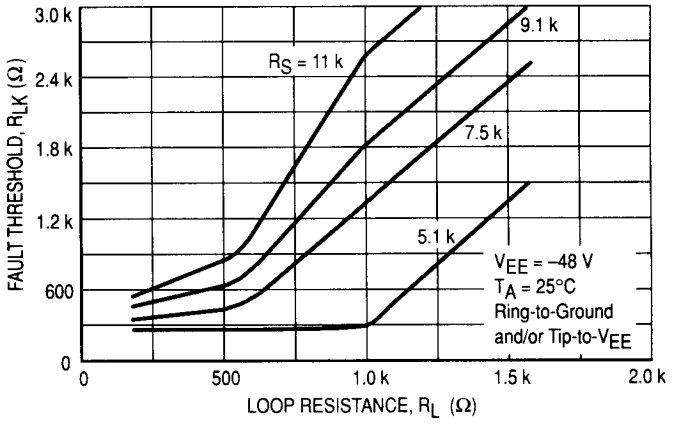


FIGURE 14 — FAULT THRESHOLD (OFF-HOOK) versus LOOP RESISTANCE

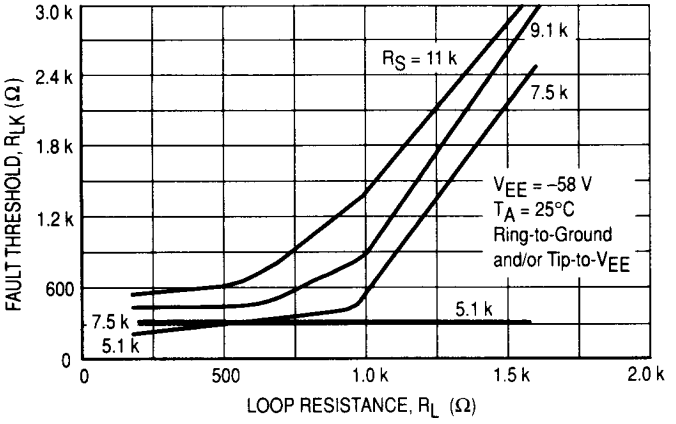


FIGURE 15 — FAULT THRESHOLD (OFF-HOOK) versus R_S

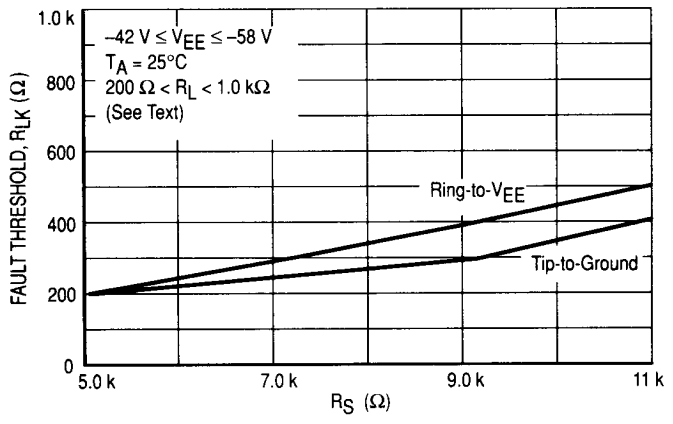


FIGURE 16 — V_{DD} RIPPLE REJECTION versus FREQUENCY

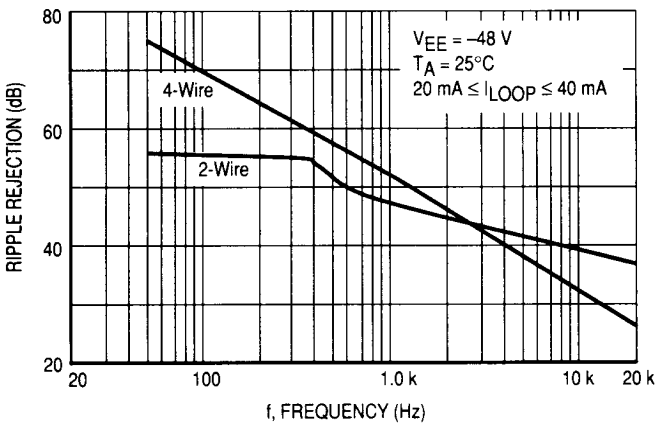


FIGURE 17 — V_{EE} RIPPLE REJECTION versus FREQUENCY

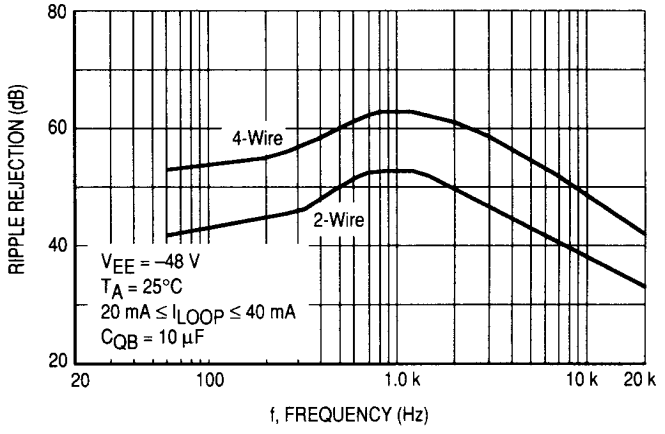


FIGURE 18 — V_{EE} RIPPLE REJECTION versus FREQUENCY AND C_{QB}

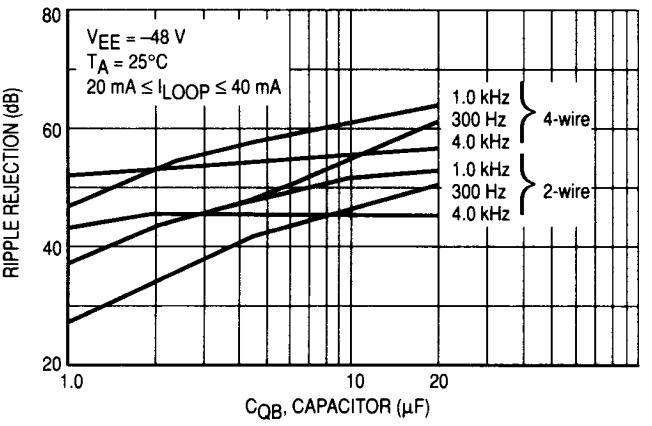


FIGURE 19 — ST1, V_{OL} versus I_{OL}

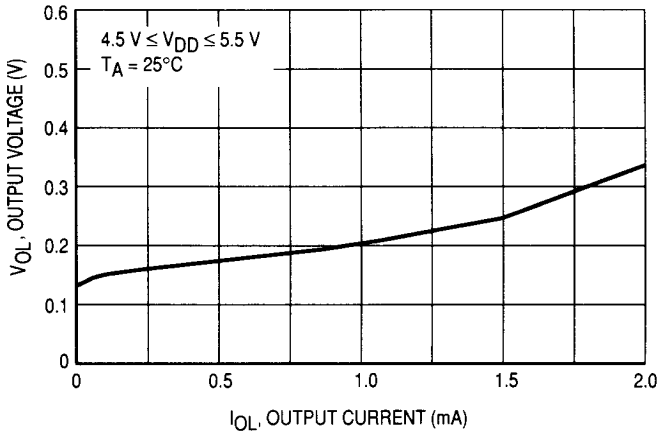


FIGURE 20 — ST1, V_{OH} versus I_{OH}

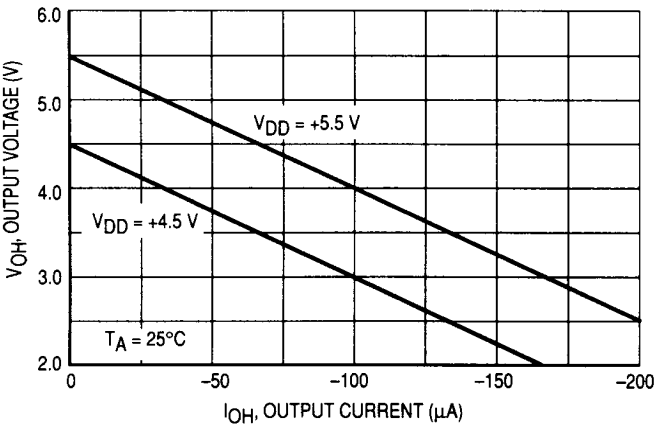


FIGURE 21 — ST2, V_{OL} versus I_{OL}

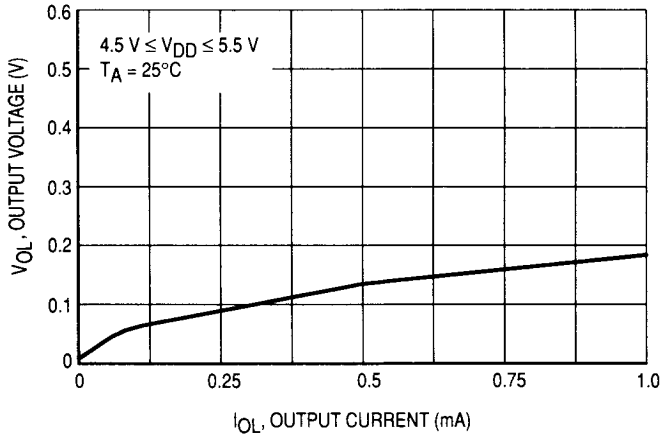


FIGURE 22 — ST2, V_{OH} versus I_{OH}

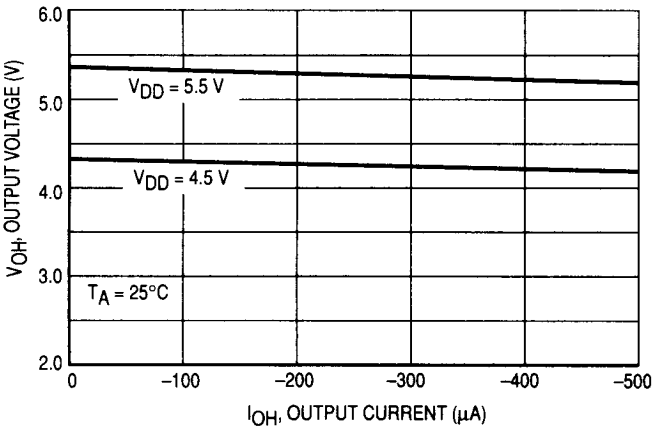


FIGURE 23 — IC POWER DISSIPATION versus LOOP RESISTANCE AND V_{EE}

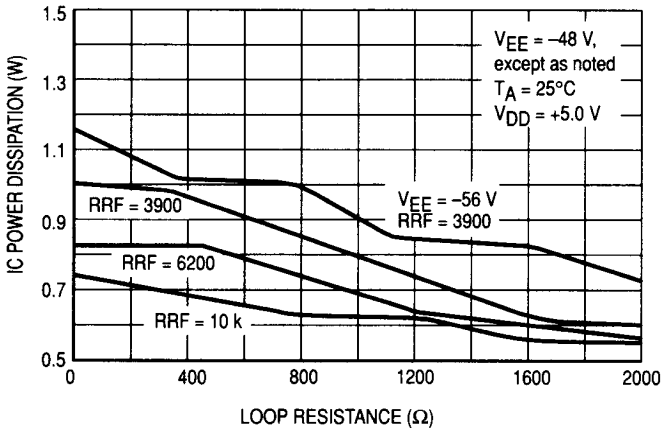


FIGURE 24 — TRANSISTOR POWER DISSIPATION versus LOOP RESISTANCE AND RRF

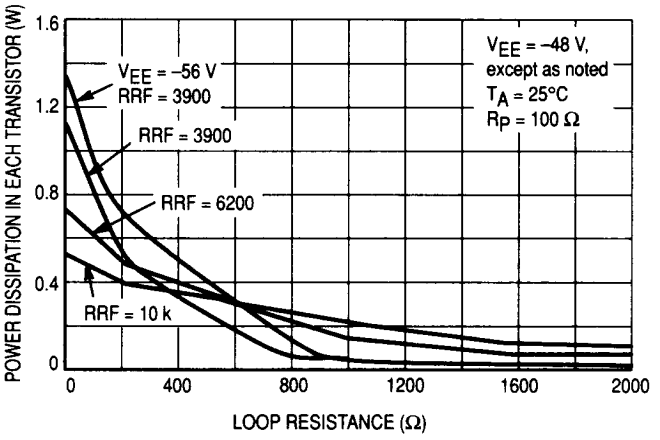


FIGURE 25 — MAXIMUM LONGITUDINAL CURRENT versus LOOP CURRENT

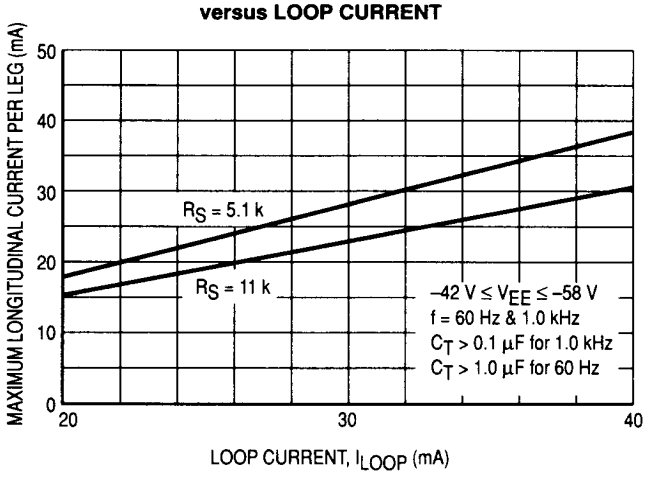
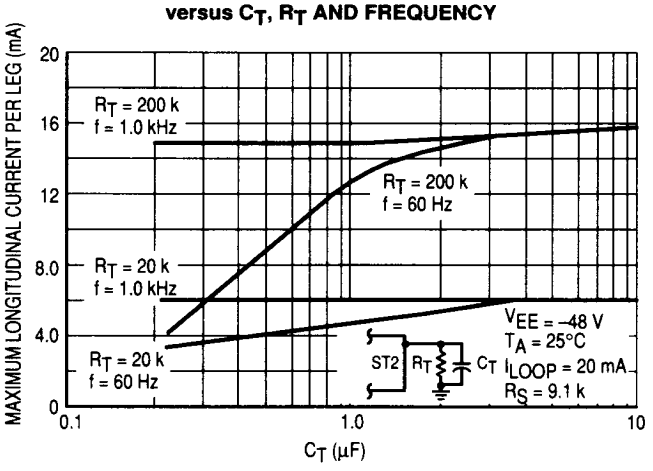


FIGURE 26 — MAXIMUM LONGITUDINAL CURRENT versus C_T, R_T AND FREQUENCY



FUNCTIONAL DESCRIPTION

Introduction

The MC33120 is a solid state SLIC (Subscriber Line Interface Circuit) which provides the interface between the two wire telephone line and the four wire side of a Central Office or PBX. Most of the BORSCHT functions are provided, specifically:

— **B**attery feed of the loop current to the line, with programmable maximum current for short lines and battery feed resistance for long lines.
— **O**vervoltage protection through internal clamp diodes and external resistors and diodes.
— **S**upervision, in that hook status is indicated in the presence of ≥30 kΩ leakage, and regardless of whether or not the circuit is powered down intentionally by the Central Office or PBX. Fault conditions are detected and indicated to the system. Dialing (pulse and DTMF) information is passed through the MC33120 to the 4-wire side.
— **H**ybrid function, in that the MC33120 is a 2-to-4 wire converter. Transmit, receive, return loss, and transhybrid gains are independently adjustable.

The MC33120 does not provide ring insertion, ring trip, digital coding/decoding of the speech signals, nor test functions. These must be provided external to this device.

The MC33120 controls two external transistors (one NPN and one PNP) through which the loop current flows. By appropriate circuit design, the power dissipation (which can exceed 3.0 watts under certain worst case conditions) is approximately equally distributed among the two transistors and the IC, thereby lowering junction temperatures and increasing long term reliability. In most situations, heatsinks will not be required.

The MC33120 incorporates critical sense resistors internally, which are trimmed for optimum performance. With this technique, the external resistors on the two wire side, which generally must be high wattage for transient protection reasons, can be non-precision.

Longitudinal balance is tested to a minimum of 58 dB @ 1.0 kHz (refer to Electrical Characteristics and Figure 1) for both the two wire and four wire side, and typically measures in the mid-60s. The longitudinal current capability is tested to a minimum of 8.5 mArms per side (refer to Electrical Characteristics and Figure 1) at a loop current of 20 mA.

Following is a description of the individual sections. Figure 4 is the reference schematic.

DC Loop Current

The DC loop current is determined by the battery voltage (V_{EE}), the load resistance across Tip and Ring, and the resistor at RFO. Varying the 4 resistors R_S and RC will influence the loop current a small amount (<5%). The curves of Figures 5–7 indicate the loop current versus loop resistance, different values of RRF, and for various values of V_{EE}. The graphs represent performance at T_A = 25°C and after the IC had reached a steady state temperature (>5 minutes).

FIGURE 27 — DC LOOP CURRENT PATH

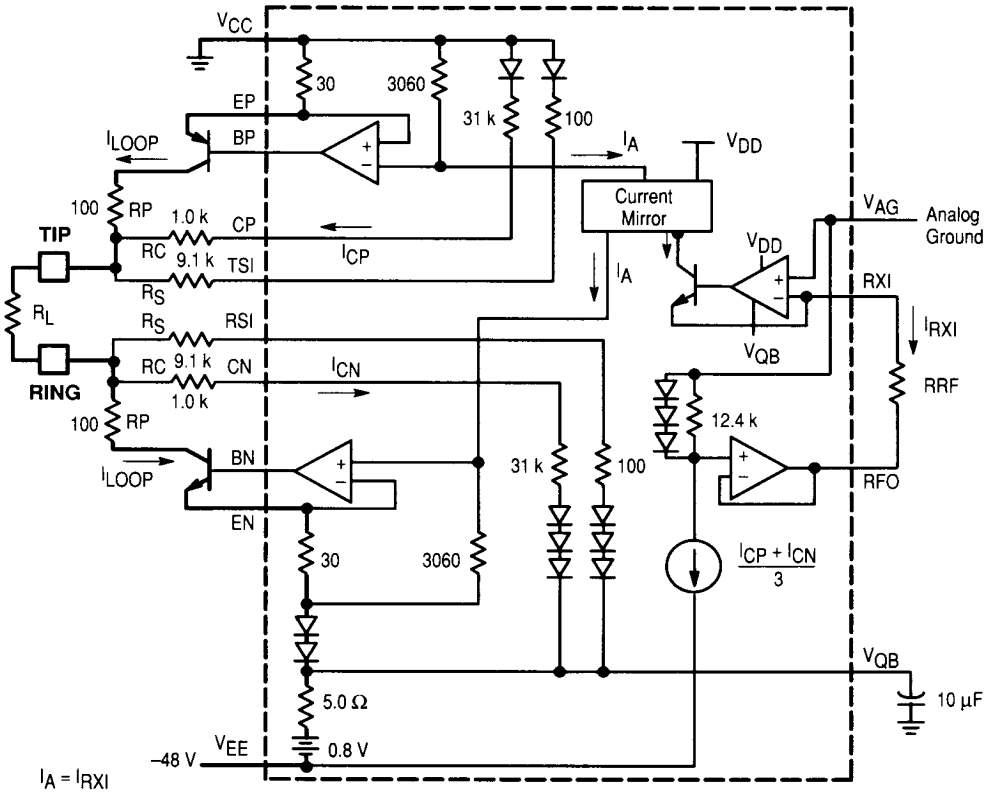


Figure 27 is representative of the DC loop current path (bold lines). On a long line (R_L > 1.0 kΩ), the loop current can be determined from the following equation:

$$I_{LOOP} = \frac{(|V_{EE}| - 3.6\ V) \bullet 13}{RRF + \{(R_L + 5) \bullet 13\}} \qquad \text{(Equation 1)}$$

On short lines (R_L < 1.0 kΩ), the three diodes across the 12.4 k resistor clamp the voltage at RFO, thereby preventing the RXI current from increasing as the load resistance is decreased. The maximum loop current is:

$$I_{LOOP\ (MAX)} = \frac{1.85\ V \bullet 102}{RRF} \ (T_A = 25°C) \qquad \text{(Equation 2)}$$

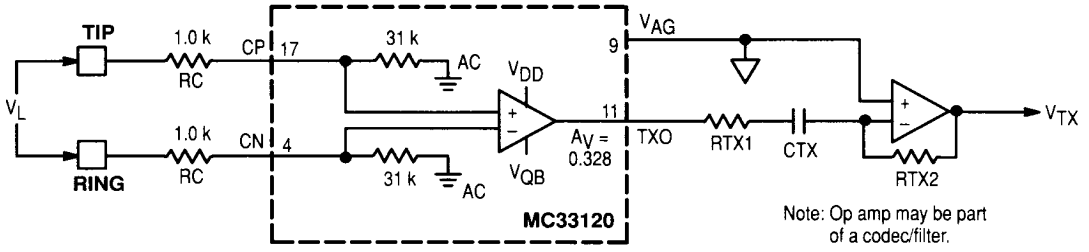
Due to the temperature dependence of a diode's forward voltage, the maximum loop current will change with temperature by ≈ –0.3%/°C.

The battery feed resistance ($\Delta V_{TIP}/\Delta I_L$) is ≈400 Ω, but depends on the loop current, V_{EE}, RRF, and is a valid parameter only on long lines where the current limit is not in effect. On short lines, the feed resistance is high since the loop current is clamped at a constant level. The AC impedance (Return Loss) however, is not determined nor affected by the DC parameters. See the Applications Section for Return Loss information.

Transmit Path

The transmit path, shown in Figure 28, consists of an internal amplifier which has inputs at CP and CN, and its output at TXO. The gain is internally fixed at 0.328 V/V (–9.7 dB). The output is in phase with the signal at CP (normally the same as TIP), and is out of phase with the signal at CN. The signal at TXO is also out of phase with that at V_{RX}, the receive signal input, described in another section.

FIGURE 28 — TRANSMIT PATH



The TXO output can swing ≈3.0 Vp-p, with a nominal current capability of ±800 µA peak (±275 µA minimum). The load on TXO is the parallel combination of RTX1 and the RRO network (described later). TXO is nominally internally biased at the V_{AG} DC level, but has an offset which varies with loop current.

In normal applications, the signal at CP/CN is reduced slightly from that at Tip/Ring by the voltage divider composed of the external RC resistors, and the internal 31 k resistors. The value of the RC resistors depends on the transient protection needed, described in another section, with 1.0 kΩ resistors being suitable for most applications. The resulting signal at TXO needs to be gained up to obtain 0 dB from Tip/Ring to V_{TX} (the 4-wire output). The common method involves an external op amp, as shown in Figure 28, with a gain of RTX2/RTX1. The gain from V_L to V_{TX} is:

$$\frac{V_{TX}}{V_L} = \frac{RTX2 \bullet 31\ k \bullet 0.328}{RTX1 \bullet (RC + 31\ k)} \qquad \text{(Equation 3)}$$

If a codec/filter is used, many of which include an internal op amp, a separate op amp is not needed. CTX is primarily for DC blocking (of the TXO offset), and is usually large (1.0 µF) so as to not affect the gain.

Receive Path

The receive path, shown in Figure 29, consists of the input at RXI, the transistor driver amplifiers, the external transistors, and the load at Tip/Ring.

RXI is a virtual ground (DC level = V_{AG}) and is a current input. Current flow is **out** of the pin. The RXI current is mirrored to the two transistor drivers which provide a gain of 102. The two external transistors are then two current sources, in series, operating at the same value. An additional internal circuit (not shown) balances the two current sources to maintain operation in their linear region.

The load current (through R_L) is slightly different from the transistor current due to the sense resistors RC and RS. The sense resistors add to the DC loop current, but subtract from the AC load current.

In normal operation, the current at RXI is composed of a DC current (from RFO), an AC current (from V_{RX}) which is the receive signal, and an AC current from TXO, which is the feedback signal to set the return loss (setting the return loss is discussed in the section on AC Terminating Impedance). The resulting AC signal at Tip is inverted from that at V_{RX}, while the signal at Ring is in phase with V_{RX}.

The resistors RP are for transient protection, and their value (defined in another section) depends on the amount of protection required. A nominal value of 100 Ω is suitable for most applications.

The system receive gain, from V_{RX} to Tip/Ring, is not described in this section since in normal applications, it involves the feedback which sets the AC terminating impedance. The Applications Section discusses these in detail.

Logic Interface (Hook status, pulse dialing, faults)

The logic interface section provides hookswitch status, fault information, and pulse dialing information to the 4-wire side of the system at the ST1 and ST2 outputs. Figure 30 is a representative diagram.

FIGURE 29 — RECEIVE PATH

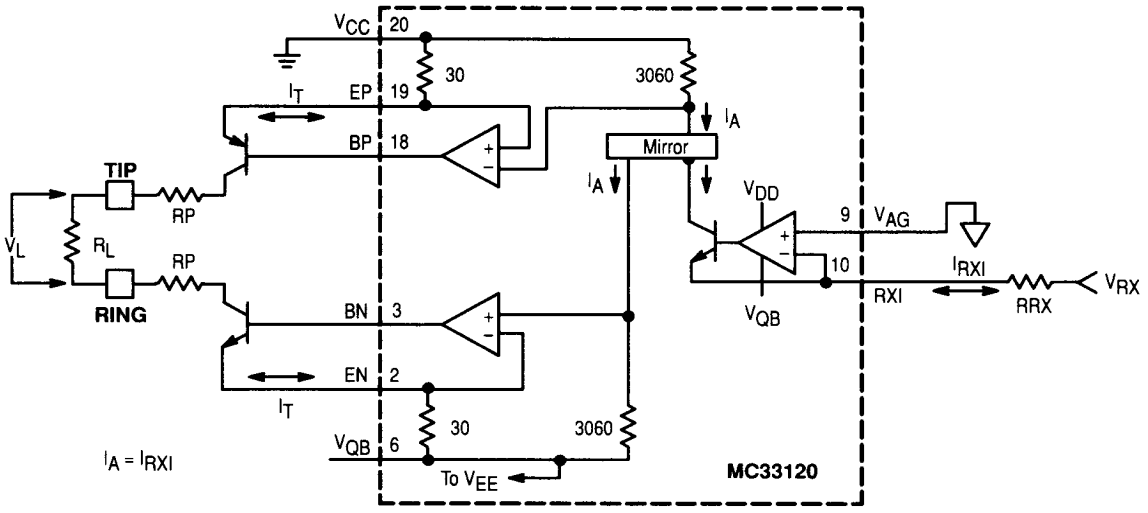
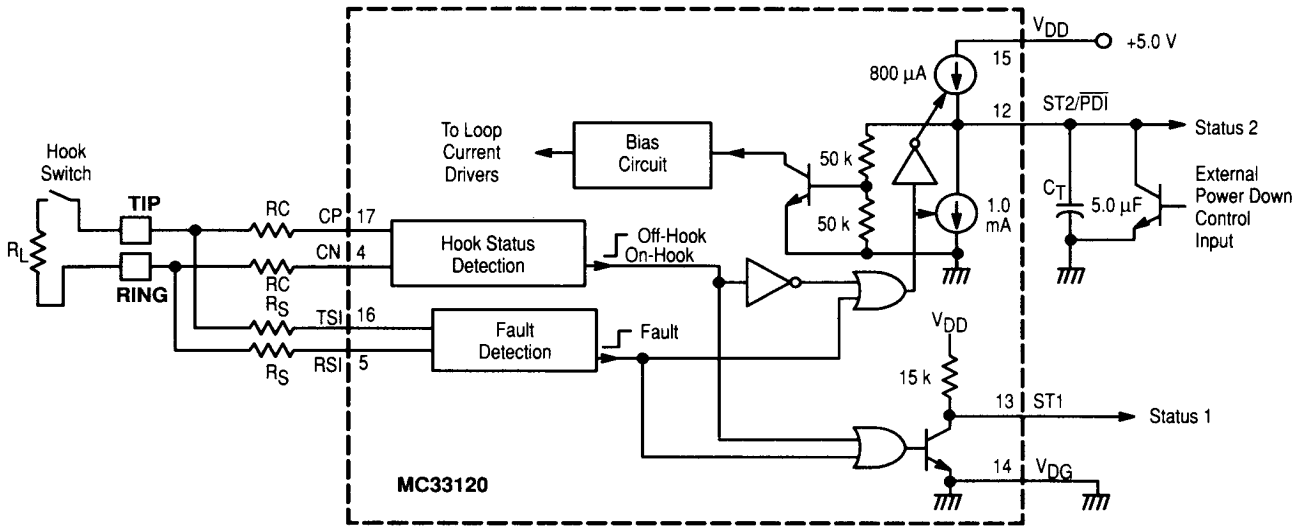


FIGURE 30 — LOGIC INTERFACE



The logic outputs operate according to the truth table in Table 1:

TABLE 1 — STATUS OUTPUT TRUTH TABLE

Hook Status	Fault Detection	Outputs		Circuit Condition
		ST1	ST2	
On Hook	No Fault	Hi	Lo	Internally powered down
Off Hook	No Fault	Lo	Hi	Powered up
On Hook	Fault	Lo	Lo	Internally powered down
Off Hook	Fault	Lo	Lo	Internally powered down

Referring to Figure 30, ST1 is configured as an active NPN pulldown with a 15 kΩ pullup resistor. ST2 has a 800 µA current source pullup, and a 1.0 mA current source for a pulldown. Current limiting this output controls the discharge from the external capacitor when ST2 switches low.

The condition where both ST1 and ST2 are high is not valid, but may occur momentarily during an off-hook to on-hook transition. The condition where both ST1 and ST2 are low may occur momentarily during an on-hook to off-hook transition — this should not be interpreted as a fault condition. ST1 and ST2 are TTL/CMOS compatible and are powered by the +5.0 V supply (V_{DD}). Refer to the Applications Section for more details.

Power Supplies, Grounds

The MC33120 requires 2 power supplies: battery voltage between – 42 V and – 58 V (V_{EE}), and an auxiliary voltage between +4.5 V and +5.5 V (V_{DD}).

V_{EE} is nominally – 48 V, with a typical range of – 42 V to – 58 V, and must be referenced to V_{CC} (battery ground). A 0.1 µF bypass capacitor should be provided between V_{CC} and V_{EE}. The V_{EE} current (I_{EE}) is nominally 1.2 mA when on-hook, 10 to 14 mA more than the loop current when off-hook, and ≈8.0 mA when off-hook but powered down by using the PDI pin. Ripple and noise rejection from V_{EE} is a minimum of 40 dB (with a 10 µF capacitor at V_{QB}), and

is dependent on the size and quality of the V_{QB} capacitor (C_{QB}) since V_{QB} is the actual internal supply voltage for the speech amplifiers. The absolute maximum for V_{EE} is – 60 V, and should not be exceeded by the combination of the battery voltage, its tolerance, and its ripple.

V_{DD} is normally supplied from the line card's digital +5.0 V supply, and is referenced to V_{DG} (digital ground). A 0.1 μF capacitor should be provided between V_{DD} and V_{DG}. The V_{DD} current (I_{DD}) is nominally 1.7 mA when on-hook and between 6.0 and 11 mA when off-hook (see Figure 10). When the MC33120 is intentionally powered down using the PDI pin, I_{DD} changes by <1.0 mA from the normal off-hook value.

V_{AG} is the analog ground for the MC33120, and is the reference for the speech signals (RXI and TXO). Current flow is **into** the pin, and is typically <0.5 μA.

Normally, V_{CC}, V_{DG} and V_{AG} are to be at the same DC level. However, if strong transients are expected at Tip and Ring, as in a Central Office application, V_{CC} should not be connected directly to V_{DG} and V_{AG} in order to prevent possible damage to the +5.0 V system. The MC33120 is designed to tolerate as much as ±30 V between V_{CC} and the other two grounds **on a transient basis only.** This feature permits V_{CC} and the other grounds to be kept separate (on an AC basis) on the line card by transient suppressors, or to be connected together farther into the system (at the power supplies). See the Applications Section on ground arrangements and transient protection for further information on connecting the MC33120 to the system supplies.

For operation of the MC33120 at supply voltages other than – 42 to – 58 V (such as – 24 V or – 28 V), contact your local Motorola sales office.

APPLICATIONS INFORMATION

This section contains information on the following topics:

Design Procedure

This section describes the step-by-step sequence for designing in the MC33120 SLIC into a typical line card application for either a PBX or Central Office. The sequence is important so that each new component value which is calculated does not affect components previously determined. Figure 4 (Typical Application Circuit) is the reference circuit for most of this discussion. The recommended sequence (detailed below), consists of establishing the DC aspects first, and then the AC aspects:

1) Determine the maximum loop current for the shortest line, select RRF. Power dissipation must be considered here.
2) Select the main protection resistors (RP), and diodes, based on the expected transient voltages. Transient protection configuration must also be considered here.
3) Select RC based on the expected transient voltages.
4) Select RS based on the desired longitudinal impedance at Tip and Ring. Transient voltages are also a factor here.
5) Calculate RRO based on the desired AC terminating impedance (return loss).
6) Calculate RRX based on the desired receive gain.
7) Calculate RTX2 and RTX1 based on the desired transmit gain.
8) Calculate the balance resistor (RB), or network, as appropriate for desired transhybrid rejection.
9) Logic Interface

Preliminary

There is a primary AC feedback loop which has its main sense points at CP and CN (see Figure 34). The loop extends from there to TXO, through RRO to RXI, through the internal amplifiers to the transistor drivers, through RP to Tip and Ring, and through the RCs to CP and CN. Components within this loop, such as RP, RC, the transistors, and the compensation capacitors need not be tightly matched to each other in order to maintain good longitudinal balance. The tolerance requirements on these components, and others, are described in subsequent sections. Any components, however, which are placed **outside** the loop for additional line card functions, such as test relay contacts, fuses, resistors in series with Tip and Ring, etc. will affect longitudinal balance, signal balance, and gains if their values and mismatch is not carefully considered. The MC33120 cannot compensate for mismatch among components outside the loop.

The compensation capacitors (0.01 μF) shown at the transistor collectors (Figure 4) compensate the transistor driver amplifiers, providing the required loop stability. The required tolerance on these capacitors can be determined from the following guidelines:

A 10% mismatch (±5% tolerance) will degrade the longitudinal balance by ≈1.0 dB on a 60 dB device, and by ≈3.0 dB on a 70 dB device.

A 20% mismatch (±10% tolerance) will degrade the longitudinal balance by ≈3.0 dB on a 60 dB device, and by ≈6.0 dB on a 70 dB device.

High quality ceramic capacitors are recommended since they serve the secondary function of providing a bleedoff path for RF signals picked up on the phone line. These capacitors should be connected to a good quality RF ground.

The capacitors used at C_{QB} and C_F must be low leakage to obtain proper performance. Leakage at the C_{QB} capacitor will affect the DC loop current characteristics, while leakage at the C_F capacitor will affect the AC gain parameters.

1) Maximum Loop Current and Battery Feed Resistance

The maximum loop current (at R_L = 0) is determined by the RRF resistor between RFO and RXI. The current limit is accomplished by three internal series diodes (see Figure 27) which clamp the voltage across RRF as the loop resistance decreases, thereby limiting the current at RXI. Since the loop current is 102 x I_{RXI}, the loop current is therefore

clamped. The graphs of Figures 5–7 indicate the maximum loop current at an ambient temperature of +25°C, and after the IC has reached thermal equilibrium (approx. 10 minutes).

Although the maximum loop current is primarily a function of the RRF resistor, it is also affected by ambient temperature, and slightly by V_{EE}. The ambient temperature effects are due to the temperature dependence of the diodes' forward voltage drop, causing the maximum loop current to change by ≈ – 0.3%/°C. Changing V_{EE} affects the maximum current in that the power dissipation is changed, thereby changing the die temperature, which affects the diodes' voltage.

The maximum loop current is affected slightly (<5%) by the choice of the RS and RC resistors, since the sense currents through those resistors add to the current supplied by the transistors.

The battery feed resistance is determined by RRF, and is not adjustable independently of the current limit. Defined as $\Delta V_{TIP}/\Delta I_L$, it is ≈400 Ω, and is a valid parameter only on long lines where the current limit is not in effect. On short lines, the feed resistance is high since the loop current is clamped at a near constant level. The AC impedance (return loss) however, is not determined nor affected by these DC parameters. Return loss is discussed in another section.

If the application requires that the current limit value have a low temperature dependence, refer to the section following this design sequence which describes an alternate configuration.

2) Main Protection Resistors (RP) and Transient Currents

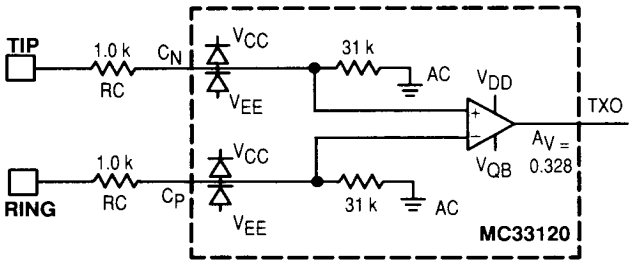
The purpose of the protection resistors (RP), along with the 4 clamp diodes shown in Figure 4, is to absorb the bulk of the transient energy when transient voltages come in from the phone line. The resistor value must be selected to limit the transient current to a value which can be tolerated by the diodes, while dissipating the energy. The recommended value shown (100 Ω) will limit the current from a 1500 V transient to 15 A, which can be carried by 1N4002 diodes under surge conditions. The resistors must be of a type which can tolerate the high instantaneous energy associated with transients. Resistor manufacturers should be consulted for this information.

Referring to Figure 4, a positive transient on either Tip or Ring, or both, will cause the transient current to be delivered to Ground. A negative transient will cause the transient current to come from the V_{EE} supply line. Therefore, the PC board track supplying V_{CC} and V_{EE} to the MC33120 must be designed to carry the transient currents as well as the normal operating currents. Additionally, since a negative transient will cause a current flow **out** of the power supply's negative output, which is opposite to the normal flow of current, provisions must be made for this reverse current flow. One suggested method is to place a zener transient suppressor (1N6290A) across the battery supply pins (V_{CC} to V_{EE}) **physically adjacent to the MC33120.** The inductance associated with PC board tracks and wiring will result in insufficient protection for the MC33120 if the suppressor is located at the opposite end of the line card, or at the power supplies.

Transient currents can be reduced by increasing the value of RP, with an upper limit determined by the DC conditions on the longest line (highest loop resistance) and minimum V_{EE} supply voltage. These conditions determine the minimum DC voltage across the transistors, which must be sufficient to handle the largest AC (transmit and receive) signals. If too large a value is selected for RP, the AC signals will be clipped. It is recommended that each transistor have no less than one volt (DC) across their collector to emitter. System AC specifications may require more than this.

Since the RP resistors are within the loop, their tolerance can be ±5% with no substantial degradation of longitudinal balance. A ±10% tolerance (20% mismatch) will degrade balance by ≈4.0 dB on a 65 dB device.

FIGURE 32 — RC PROTECTION RESISTORS



3) Selecting the RC Resistors

The primary purpose of the RC resistors is to protect the CP and CN pins from transient voltages and destructive currents. Internally, these pins have clamp diodes to V_{CC} and V_{EE} rated for a maximum of 1.0 A under surge conditions only (Figure 32). The 1.0 kΩ resistors shown in the figures, for example, will provide protection against surges up to 1.0 kV. Resistor manufacturers must be consulted for the proper type of resistor for this environment.

The RC resistors are in series with internal 31 kΩ resistors, and therefore form a voltage divider to the inputs of the transmit amplifier, as shown in Figure 32. This will affect the transmit gain, receive gain, return loss, and transhybrid rejection (described in subsequent sections). The tolerance of the RC resistors depends on the value selected for them, since any mismatch between them will create a differential voltage at CP and CN when longitudinal voltages are present on Tip and Ring. To ensure a minimum of 58 dB of longitudinal balance, the resistors' absolute value must not differ by more than 39 Ω. With a nominal value of 1.0 kΩ, their tolerance must be ±2%, or less. If their nominal value is 390 Ω or less, their tolerance can be ±5%.

4) Longitudinal Impedance (Z_{LONG}) — Selecting the RS Resistors

The longitudinal impedance is determined by the RS resistors at the TSI and RSI pins according to the following equation:

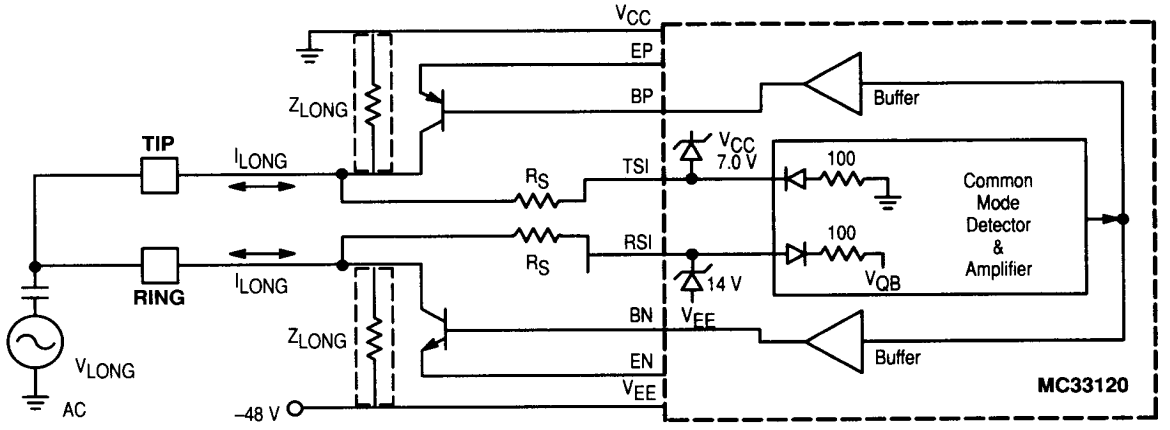
$$Z_{LONG} = \frac{RS + 100}{51} \qquad \text{(Equation 4)}$$

Z_{LONG} is defined as V_{LONG}/I_{LONG} as shown in Figure 33; for RS = 9.1 kΩ, Z_{LONG} = 180 Ω. The calculated value of Z_{LONG} includes the fact that the RS resistors are in parallel with the synthesized impedance. The tolerance of the RS resistors therefore depends on how much mismatch can be tolerated between the longitudinal impedances at Tip and at Ring. Calculations indicate the two RS resistors

can have a ±5% tolerance, and still comfortably provide a minimum of 58 dB longitudinal balance.

The resistors must be able to withstand transient voltages expected at Tip and Ring. The TSI and RSI pins have internal clamp diodes rated for a maximum of 1.0 A under surge conditions only (Figure 33). Resistor manufacturers must be consulted for the proper type of resistor for this environment.

FIGURE 33 — LONGITUDINAL IMPEDANCE

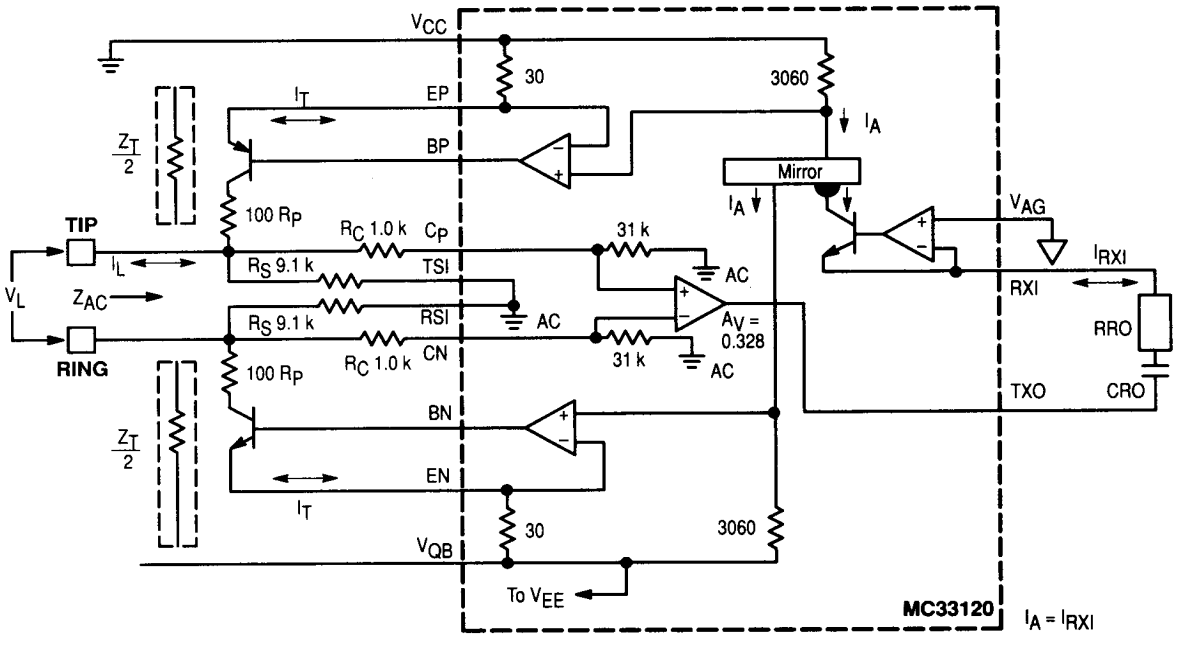


5) AC Terminating Impedance and Source Impedance (Z_{ac}) — Return Loss

The return loss measurement is a measure of how closely the AC impedance of the SLIC circuit matches the characteristic impedance of the phone line, or a reference impedance. The reference impedance can be, in some cases, a pure resistance (commonly 600 Ω or 900 Ω), a series resistor and capacitor (900 Ω + 2.16 μF), or a more complex network. To achieve proper return loss with the MC33120, the RRO impedance shown in Figure 34 is to have the same configuration as the reference impedance, but with values scaled according to the equations mentioned below.

CRO, used primarily for DC blocking, is generally a large value (1.0 μF) so as to not affect the impedance of RRO. However, it can be included in the RRO network if a complex network is required.

FIGURE 34 — AC TERMINATING IMPEDANCE



Z_{ac} is the impedance looking into the circuit from Tip and Ring (set by RRO), and is defined as V_L/I_L. Half of Z_{ac} is from Tip to V_{CC}, and the other half is from Ring to V_{QB} (an AC ground). Each half is made up of a synthesized impedance ($Z_T/2$) in parallel with R_S and (RC + 31 k).

Therefore Z_{ac} is equal to:

$$Z_{ac} = [Z_T/2 \,//R_S//(RC + 31\ k)] \bullet 2 \qquad \text{(Equation 5)}$$

$$\text{and } \frac{Z_T}{2} = \frac{\{R_S//(RC + 31\ k)\} \bullet (Z_{ac}/2)}{\{R_S//(RC + 31\ k)\} - (Z_{ac}/2)} \qquad \text{(Equation 6)}$$

The synthesized impedance Z_T is created as follows:

An incoming signal V_L produces a differential voltage at CP and CN, and therefore at TXO equal to:

$$V_{TXO} = \frac{V_L \bullet 31\ k \bullet 0.328}{(RC + 31\ k)} \qquad \text{(Equation 7)}$$

The signal at TXO creates an AC current I_{RXI} through RRO. RXI is a virtual ground, and CRO is insignificant for first order calculations.

I_{RXI} is gained up by a factor of 102 to produce the current I_T through the transistors.

Z_T is therefore V_L/I_T. The relationship between Z_T and RRO is:

$$RRO = \frac{Z_T \bullet 1.037 \bullet 10^6}{(31\ k + RC)} \qquad \text{(Equation 8)}$$

While equation 8 gives the exact value for RRO, a first order approximation is $Z_{ac} \bullet 33.5$.

a) Resistive Loads (with RC = 1.0 k, R_S = 9.1 k):

For a 600 Ω resistive system, Z_T calculates to 626 Ω, and RRO calculates to 20.3 kΩ.

For a 900 Ω resistive system, Z_T calculates to 961 Ω, and RRO calculates to 31.14 kΩ.

b) Complex Loads

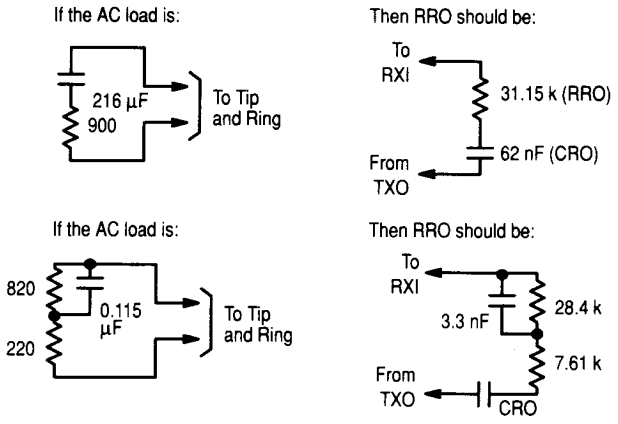
For complex (non-resistive) loads, the MC33120 must be made to look like a termination impedance equal to that complex load. This is accomplished by configuring RRO the same as the complex load, but with all impedance values increased according to the scaling factor of Equation 9.

$$SF = \frac{[(RC + 31\ k)//RS] \bullet 1.037 \bullet 10^6}{(RC + 31\ k) \bullet [(RC + 31\ k)//R_S - (Z_{ac}/2)]} \qquad \text{(Equation 9)}$$

Z_{ac} is computed at a nominal frequency of interest. A first order approximation of Equation 9 is:

$$SF = 1.037 \bullet 10^6/(RC + 31\ k) \qquad \text{(Equation 9a)}$$

For example:

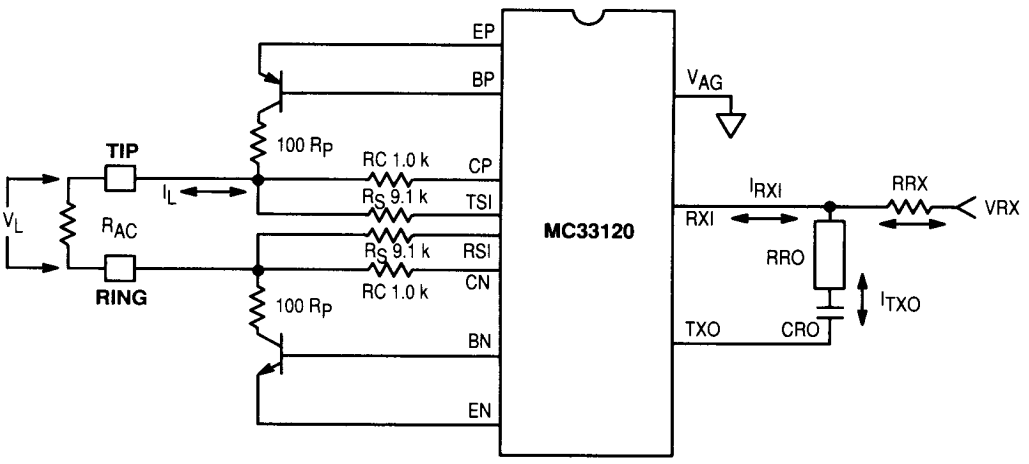


CRO must remain in series with the network to provide DC blocking. If the load network does not include a series capacitor (as in the second example above), CRO should be large (1.0 µF) so its impedance does not affect the RRO network. The above procedure will yield a return loss measurement which is constant with respect to frequency. The RRO resistor, or network, must have a tolerance equal to or better than the required system tolerance for return loss and receive gain.

6) Receive Gain (G_{RX})

The receive gain involves the same circuit as Figure 34, but with the addition of the RRX resistor (or network) which sets the receive gain. See Figure 35.

FIGURE 35 — RECEIVE GAIN



The receive gain (G_{RX}), defined as the voltage gain from V_{RX} to V_L, is calculated as follows:

RXI is a virtual ground, and R_{ac} is the AC impedance of the load (phone line).

The AC current generated in the transistors is 102 • I_{RXI}, which is equal to 102 • ($I_R - I_{TXO}$).

$I_R = V_{RX}/RRX$, and

$$I_{TXO} = \frac{V_{TXO}}{RRO} = \frac{V_L \bullet 31\ k \bullet 0.328}{RRO \bullet (31\ k + RC)} \qquad \text{(Equation 10)}$$

Using equations 5 and 8, involving Z_{ac}, RS and RC, and the above equations yields:

$$\frac{V_L}{V_{RX}} = G_{RX} = \frac{102 \bullet (R_{ac}//Z_{ac})}{RRX} \qquad \text{(Equation 11)}$$

$$\text{Therefore, } RRX = \frac{102 \bullet (R_{ac}//Z_{ac})}{G_{RX}} \qquad \text{(Equation 12)}$$

Equation 12 applies **only** for the case where R_{ac} and Z_{ac} have the same configuration. If they also have the same magnitude, then set RRX = 51 • R_{ac} to set a receive gain of 0 dB. The AC source impedance of the above circuit to Tip and Ring is Z_{ac}. For the case where $R_{ac} \neq Z_{ac}$, use the following equation:

$$\frac{V_L}{V_{RX}} = \frac{102}{RRX \bullet \left[\frac{1}{Z_L} + \frac{1.037 \bullet 10^6}{(31k + RC) \bullet RRO}\right]} \qquad \text{(Equation 13)}$$

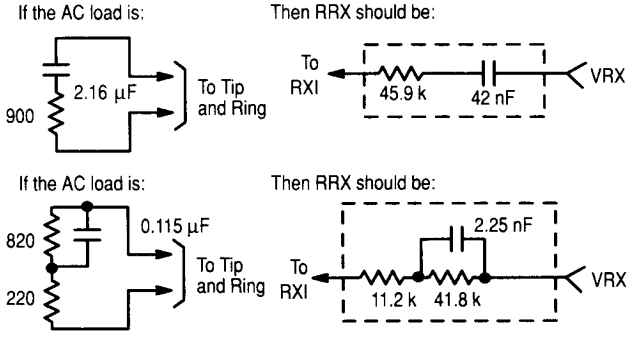
$$\text{where } Z_L = \left[\frac{R_{ac}}{2} // RS // (RC + 31\ k)\right] \bullet 2 \qquad \text{(Equation 14)}$$

a) Resistive Loads

For a 600 Ω resistive system, set RRX = 30.6 kΩ, and for a 900 Ω resistive system, set RRX = 45.9 kΩ.

b) Complex Loads

For complex (non-resistive) loads, the RRX resistor needs to be replaced with a network having the same configuration as the complex load, but with all impedance values scaled up by a factor of 51 (for 0 dB gain). If a gain other than 0 dB is desired, the scaling factor is determined from Equation 12. This methods applies **only** if the RRO network has been made complex comparable to the load according to the procedure in the previous section (Equations 5–9a), such that $R_{ac} = Z_{ac}$. Using a scaling factor of 51, and the previous examples, yields:



The preceeding procedure will yield a receive gain which is constant with respect to frequency. The RRX resistor, or network, must have a tolerance equal to or better than the required system tolerance for receive gain.

7) Transmit Gain (G_{TX})

Setting the transmit gain involves selecting RTX1 and RTX2 in Figure 28. The voltage gain from V_L to V_{TX} is calculated from the following:

$$G_{TX} = \frac{V_{TX}}{V_L} = \frac{RTX2 \bullet 31\ k \bullet 0.328}{RTX1 \bullet (RC + 31\ k)} \qquad \text{(Equation 15)}$$

For 0 dB gain, set RTX2 = 3.15 x RTX1 (for RC = 1.0 k). The actual values of RTX2 and RTX1 are not critical — only their ratio so as to provide the proper gain at the op amp. Once the ratio is established, the two resistors can be selected from a set of standard resistor values. The minimum value for RTX1 is limited by the drive capability of TXO, which is a nominal ±800 µA peak (±275 µA minimum). As a general rule, RTX1 should be between 6.0 kΩ and 20 kΩ. The load on TXO is the parallel combination of RTX1 and RRO.

CTX is for DC blocking, and is typically a large value (1.0 µF) so as to not be a significant impedance. In general, it should **not** be used for low frequency rolloff as that will affect the transhybrid rejection (discussed in the next section). Low frequency rolloff should be done after the op amp. High frequency rolloff can be set by placing a capacitor across RTX2.

For complex loads (at Tip and Ring), if RRO and RRX have been made complex comparable to the load as described in the previous sections, neither RTX1 nor RTX2 needs to be complex since both the transmit and receive signals which appear at TXO will be flat with respect to frequency.

RTX1 and RTX2 must have a tolerance equal to or better than the required system tolerance for the transmit gain.

8) Balance Network (RB) — Transhybrid Rejection

When a receive signal is applied to V_{RX} to produce a signal at Tip and Ring, the two-to-four wire arrangement of a hybrid (the MC33120) results in a reflected signal at TXO. Transhybrid rejection involves canceling that reflected signal before it appears at V_{TX}. The method used is to insert the RB resistor (or network) as shown in Figure 36. The current I_B, supplied form V_{RX}, cancels the current I_{TX1} supplied from TXO (Node A is a virtual ground). Good transhybrid cancellation requires that the currents be equal in magnitude **and** 180° out of phase at node A.

Using the equations for transmit and receive gains, the current I_{TX1} is equal to:

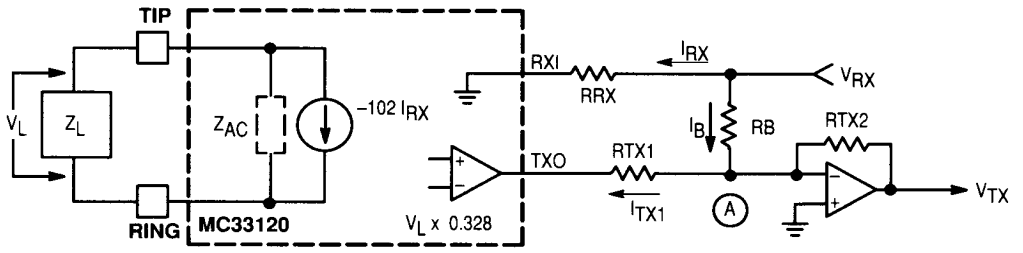
$$I_{TX1} = \frac{33.5 \bullet V_{RX} \bullet Z_{ac} \bullet Z_L \bullet 31\ k}{RRX \bullet [Z_{ac} + Z_L] \bullet RTX1 \bullet (RC + 31\ k)} \qquad \text{(Equation 16)}$$

a) For the case where RRO and RRX are comparable in configuration to Z_L:

Since $I_B = V_{RX}/RB$, then RB can be determined from:

$$RB = \frac{RRX \bullet RTX1 \bullet (RC + 31\ k)}{33.5 \bullet [Z_{ac}//Z_L] \bullet 31\ k} \qquad \text{(Equation 17)}$$

FIGURE 36 — BALANCE RESISTOR



Equation 17 provides a value for an RB resistor which will provide the correct magnitude for I_B. The correct phase relationship is provided by the fact that the signal at TXO is out of phase with that at V_{RX}. The phase relationship will be 180° **only** if RRO and RRX are of a configuration identical to that of the load. This applies regardless of whether the load, Z_L, (and RRO and RRX) are purely resistive or of a complex nature. Equation 17 reduces to a non-complex resistance if RRX, Z_{ac}, and Z_L are all comparably complex.

For the case where $Z_{ac} = Z_L$, RRX = 51 • Z_{ac}, and RC = 1.0 k, Equation 17 reduces to:

$$RB = 3.15 \bullet RTX1 \qquad \text{(Equation 18)}$$

b) For the case where Z_{ac} and Z_L do not have the same frequency characteristics:

For the case where, for reasons of cost and/or simplicity, the load (R_L) is considered resistive (whereas in reality it is not a pure resistance) and therefore resistors, rather than networks, were selected for RRO and RRX, using a simple resistor for RB may not provide sufficient transhybrid rejection due to a phase angle difference between V_{RX} and TXO. The terminating impedance may therefore not necessarily be matched exactly to the line impedance, but the resulting circuit still provides sufficiently correct performance for receive gain, transmit gain, and return loss. The rejection can be improved in this case by replacing RB with the configuration shown in Figure 37. Even on a very short phone line there is a reactive component to the load due to the two compensation capacitors (C_C, Figure 4) at the transistor collectors. The two capacitors can be considered in series with each other, and across the load as shown in Figure 37. To simplify the explanation, the current source and Z_{ac} of Figure 36 are replaced with the Thevenin voltage source and series Z_{ac}. Since Z_L and Z_{ac} are not matched, there will be a phase shift from V_{RX} to the signal across Tip and Ring. This phase shift is also present at TXO. The same phase shift is generated at node B in the RB network by making RB1 equal to Z_{ac}, and Z_L equal to the load. RB2 is then calculated from:

$$RB2 = \frac{RRX \bullet RTX1 \bullet (RC + 31\ k)}{33.5 \bullet Z_{ac} \bullet 31\ k} \qquad \text{(Equation 19)}$$

For example, for a system where the load is considered a 600 Ω resistor (RRO = 20.3 kΩ, RRX = 30.6 kΩ, RTX1 = 10 kΩ, and RC = 1.0 kΩ), RB1 would be a 600 Ω resistor, Z_L (in the RB network) would be a 600 Ω resistor in parallel with a 0.005 µF capacitor, and RB2 calculates to 15.715 kΩ.

The RB resistor, or network, must have a tolerance equal to or better than the required system tolerance for transhybrid rejection.

9) Logic Interface

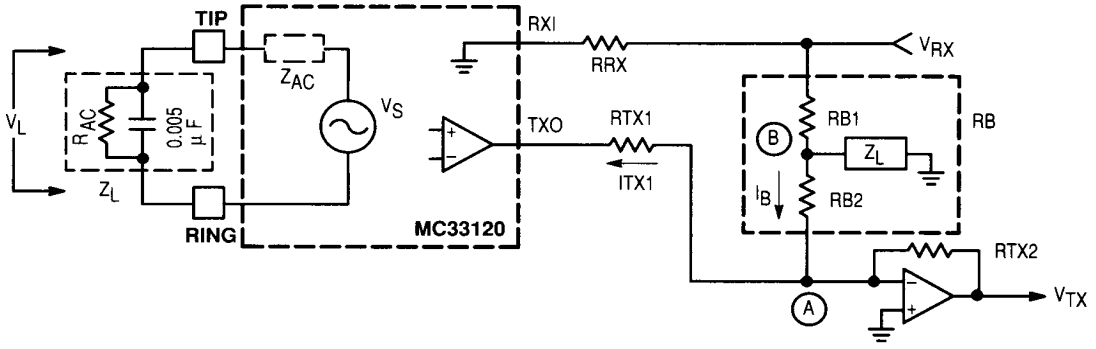
The logic circuit (output ST1, and the I/O labeled ST2/PDI) is depicted in Figure 30, and functions according to the truth table in Table 1.

a) Output Characteristics

ST1 is a traditional NPN pull-down with a 15 kΩ pull-up resistor. Figures 19 and 20 indicate its output characteristics.

ST2 is configured with the following items: a) a 1.0 mA current source for a pull-down which is active only when ST2 is internally set low; b) an 800 µA current source pull-up which is active only when ST2 is internally set high; c) a positive feedback aspect within this output circuit which provides considerable hysteresis for stability reasons. Its output characteristics are shown in Figures 21 and 22. Due to this configuration, any external pull-up resistance which is applied to this pin must be greater than 15 kΩ, or the output may not reliably switch from high to low. Any external pull-down resistance does not affect this output's ability to

FIGURE 37 — BALANCE NETWORK



switch from low-to-high, but **does** affect the maximum longitudinal currents which can be accepted by the circuit (see the section on Longitudinal Current capability). The capacitor (C_T) is required to provide a time delay, for stability reasons, during transitions between off-hook and on-hook. This capacitor additionally affects maximum longitudinal currents, as well as stability during pulse dialing (explained below).

b) Hook Status

The MC33120 uses the sense currents at CP and CN to activate the hook status circuit. The sensing is configured such that the circuit monitors the impedance across Tip/Ring, which results in the hookswitch thresholds being virtually independent of the battery voltage. The off-hook to on-hook threshold is affected by the choice of RRF according to the graph of Figure 8, but is not affected by the value of RS. The on-hook to off-hook threshold is affected by the value of RS according to the graph of Figure 9, but is not affected by RRF. Varying the RC resistors does not affect the thresholds significantly.

When the telephone is on-hook (ST1 = Hi, ST2 = Low), the MC33120 is internally powered down, the external transistors are shut off, and power consumption is at a minimum. Upon closure of the phone's hookswitch, ST1 will switch low within 10 μs. ST2 will then change state slowly due to the external capacitor (C_T = 5.0 μF). There is a ≈8.0 millisecond delay for ST2 to reach the threshold necessary to activate the internal bias circuit, which in turn activates the external drive transistors to supply loop current. This delay is necessary to prevent instabilities during the transition to off-hook.

Upon opening the telephone's hookswitch, ST1 will switch high within ≈200 μs. ST2 then requires ≈60 ms to reach the threshold to switch off the internal bias circuit, which in turn shuts down the external drive transistors.

c) Pulse Dialing

During pulse dialing, ST1 will change state concurrent with the hookswitch. ST2 is kept from switching during pulse dialing by the external capacitor (C_T), which keeps the MC33120 in a powered up condition and stable. If the C_T capacitor is too small, the voltage at ST2 could droop to the PDI threshold (see section e below) during each pulse. This could cause the MC33120 to create additional noise on the line as it would cycle between a power-up and power-down condition with each dialing pulse.

d) Fault Detection

Faults are defined as excessive leakage from Tip to V_{EE} and/or ground, and from Ring to V_{EE} and/or ground. A single fault is any one of the above conditions, while a double fault is defined as excessive leakage from Tip to V_{EE} **and** from Ring to V_{CC}, as depicted in Figure 38. Refer to Figures 11–15 for the resistance, R_{LK}, which will cause the MC33120 to switch to a power-down condition. If the leakage resistance is less than that indicated in the graphs, the MC33120 will power-down itself and the two external transistors, thereby protecting them from overheating. Both status outputs (ST1 and ST2) will be at a logic low, indicating a fault condition. A fault condition is detected by monitoring an imbalance in the magnitudes of the currents at TSI and RSI, and/or a polarity reversal at Tip and Ring.

The MC33120 will detect the following conditions:

1) When on-hook (see Figure 11):
   a) <2.0 kΩ between Ring and V_{CC}, with no hysteresis at this threshold, or
   b) <2.5 kΩ between Tip and V_{EE}, with no hysteresis at this threshold, or
   c) Both a and b simultaneously.

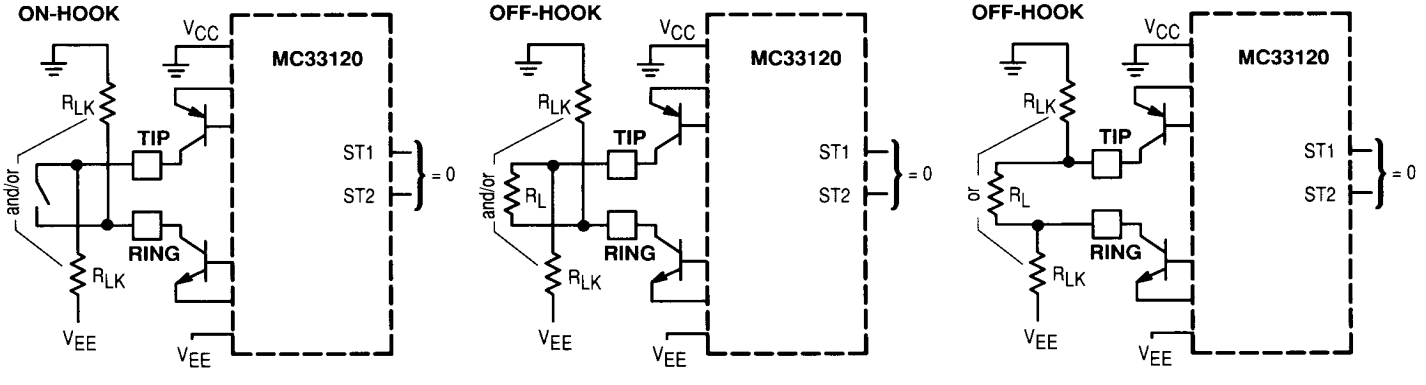
Leakage from Tip to V_{CC} and/or Ring to V_{EE} are not detected as faults while the MC33120 is on-hook.

2) When off-hook (600 Ω between Tip and Ring):
   a) <500 Ω between Tip and V_{CC}, or
   b) <600 Ω between Tip and V_{EE}, or
   c) <500 Ω between Ring and V_{EE}, or
   d) <600 Ω between Ring and V_{CC}, or
   e) Both b and d simultaneously

A simultaneous occurrence of conditions a) and c) is not detected as a fault. See Figures 12–15 for the threshold variation with R_L. Resetting of the fault detection circuit requires that the leakage resistance be increased to a value between 10 kΩ and 20 kΩ, depending on V_{EE}, R_L, and R_S. Both ST1 and ST2 should be monitored for hookswitch status to preclude not detecting a fault condition.

Figure 15 indicates the variation in fault thresholds for Tip-to-V_{CC} and Ring-to-Battery faults, and is valid only for loop resistances of 200 Ω to 1.0 kΩ. On loops larger than

FIGURE 38 — FAULT DETECTION



1.0 kΩ, the MC33120 does not reliably indicate the fault condition at ST1 and ST2, but may indicate on-hook status instead. This does not apply to Tip-to-Battery and Ring-to-V_{CC} faults which are correctly detected for lines beyond 1.0 kΩ.

e) PDI Input

The ST2 output can also be used as an input (PDI input) to power down the circuit, denying loop current to the subscriber (by shutting off the external pass transistors), regardless of the hookswitch position. Powering down is accomplished by pulling PDI to a logic low with an open collector output, or an NPN transistor as shown in Figure 30. The switching threshold is ≈+1.5 V. The current out of PDI, when pulled low, is ≈800 μA. Releasing PDI allows the MC33120 to resume normal operation.

If the external telephone is off-hook while the MC33120 is powered down, sense currents at CP and TSI will result in some loop current flowing through the loop and back into CN and RSI. This current is generally on the order of 1.0 to 3.0 mA, determined primarily by the RS resistors, loop resistance, and V_{EE}. ST1 will continue to indicate the telephone's actual hook status while PDI is held low. The on-to-off hook threshold is the same as that during normal operation, but the off-to-on hook threshold is >250 kΩ.

When powered down with the PDI pin, the receive gain (V_{RXI} to Tip/Ring) is muted by >90 dB, and the transmit gain (Tip/Ring to TXO) is muted by >30 dB.

Power Dissipation, Calculation and Considerations

a) Reliability

The maximum power dissipated by the MC33120 must be considered, and managed, so as to not exceed the junction temperature listed in the Absolute Maximum Ratings. Exceeding this temperature on a recurring basis will reduce long term reliability, and possibly degrade performance. The junction temperature also affects the statistical lifetime of the device, due to long term thermal effects within the package. Today's plastic integrated circuit packages are as reliable as ceramic packages under most environmental conditions. However, when the ultimate in system reliability is required, thermal managements must be considered as a prime system design goal.

Modern plastic package assembly technology utilizes gold wire bonded to aluminum bonding pads throughout the electronics industry. When exposed to high temperatures for protracted periods of time an intermetallic compound can form in the bond area resulting in high impedance contacts and degradation of device performance. Since the formation of intermetallic compounds is directly related to device junction temperature, it is incumbent on the designer to determine that the device junction temperature is consistent with system reliability goals.

Based on the results of almost ten years of +125°C operating life testing, Table 2 has been derived indicating the relationship between junction temperature and time to 0.1% wire bond failure.

TABLE 2 — STATISTICAL LIFETIME

Junction Temperature (°C)	Time (Hours)	Time (Years)
80	1,032,200	117.8
90	419,300	47.9
100	178,700	20.4
110	79,600	9.4
120	37,000	4.2
130	17,800	2.0
140	8,900	1.0

Motorola MECL Device Data, DL122

The "time" in Table 2 refers to the time the device is operating at that junction temperature. Since the MC33120 is at a low power condition (nominally 68 mW) when on-hook, the duty cycle must be considered. For example, if a statistical duty cycle of 20% off-hook time is used, operation at 130°C junction temperature (when off-hook) would result in a statistical lifetime of ≈10 years.

b) Power and Junction Temperature Calculation

The power within the IC is calculated by subtracting the power dissipated in the two wire side (the transistors and the load) from the power delivered to the IC by the power supplies. Refer to Figure 4 and 27.

$$P_D = |V_{DD} \bullet I_{DD}| + |V_{EE} \bullet I_{EE}| - (I_{LOOP} \bullet |V_{EP} - V_{EN}|)$$

(Equation 20)

The terms V_{EP} and V_{EN} are the DC voltages, with respect to ground, at the EP and EN pins. These voltages can be measured, or can be approximated by:

$$V_{EP} \approx -(30\ \Omega \bullet I_{LOOP})$$
$$V_{EN} \approx V_{EE} + 2.1\ V + (I_{LOOP} \bullet 35\ \Omega)$$

Refer to Figure 23. The junction temperature is then calculated from:

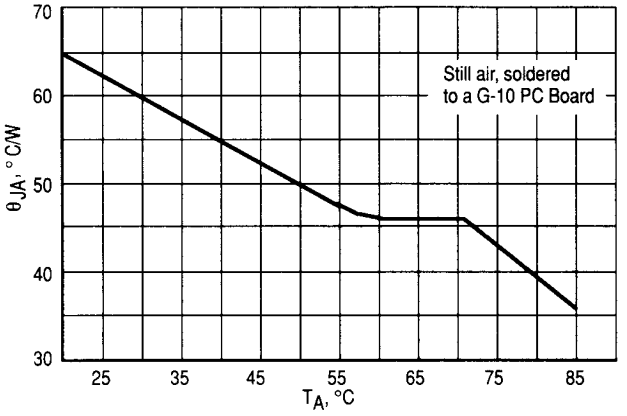
$$T_J = T_A + (P_D \bullet \theta_{JA})$$

(Equation 21)

where T_A is the ambient air temperature at the IC package, and θ_{JA} is the junction-to-ambient thermal resistance shown in Figure 39. The highest junction temperature will occur at maximum V_{EE} and V_{DD}, maximum loop current, and maximum ambient temperature.

If the above calculations indicate the junction temperature will exceed the maximum specified, then it is necessary to reduce the maximum loop current, ambient temperature, and/or V_{EE} supply voltage. Air flow should not be restricted near the IC by tall components or other objects since even a small amount of air flow can substantially reduce junction temperature. For example, typically an air flow of 300 LFPM (3.5 mph) can reduce the effective θ_{JA} by 14 to 20% from that which occurs in still air. Additionally, providing as much copper area as possible at the IC pins will assist in drawing away heat from within the IC package. For additional information on this subject, refer to the "Thermal Considerations" section of *Motorola MECL System Design Handbook* (HB205), and the "System Design Considerations" section of *Motorola MECL Device Data* (DL122).

FIGURE 39 — THERMAL RESISTANCE (JUNCTION TO AMBIENT)



Selecting the Transistors

The specifications for the two loop current pass transistors involve their current gain, voltage rating, and power dissipation capabilities at the highest ambient temperatures. Power dissipation during both normal operation and faults must be considered when determining worst case situations. Generally, more power is dissipated during a fault condition than during normal operation.

The transistors' minimum beta is recommended to be 40 at the loop currents involved in the application. A lower beta could degrade gain and balance performance. Maximum beta should be less than 500 to prevent possible oscillations. Darlington type transistors should not be used. The voltage rating should be a minimum of 80 V, although the choice of protection scheme may require a higher rating.

Referring to Figure 27, during normal operation the loop current and the voltage across the transistors are both at a maximum when the load impedance (R_L) is at a minimum. The loop current is determined by RRF and the graphs of Figures 5–7. The voltage across each transistor is determined from the following:

$$V_T = \frac{|V_{EE}| - 2.1 - [(65 + 2RP + R_L) \bullet I_{LOOP}]}{2} \quad \text{(Equation 22)}$$

The power in each transistor is then ($V_T \bullet I_{LOOP}$). The voltage across the two transistors will always be nearly equal during normal operation, resulting in equal power dissipation. The graph of Figure 24 indicates the power dissipated in each transistor where RP = 100 Ω.

During a fault condition, depicted in Figure 38, if the leakage resistance from Tip to V_{EE} or from Ring to V_{CC} is less than that shown in Figures 12–14 (when off-hook), the MC33120 will power down the transistors to protect them from overheating. Should the leakage resistance be slightly higher than that shown in the graphs, however, and the fault detection has not been activated, the power in one transistor (in a single fault, both transistors in a double fault) will be higher than normal. The power will depend on V_{EE}, R_L, RP and the leakage resistance. Table 3 is a guide of the power in the transistor dissipating the higher power level.

TABLE 3 — TRANSISTOR POWER DURING A FAULT

V_{EE}	R_S	R_L	P_{PNP}	P_{NPN}
–58	9.1 k	200	1.64	1.34
–48	9.1 k	200	1.05	0.957
–58	9.1 k	600	1.37	1.11
–48	9.1 k	600	0.746	0.616
–58	9.1 k	1.0 k	0.897	0.68
–48	9.1 k	1.0 k	0.232	0.194
–58	5.1 k	200	1.8	1.55
–58	11 k	200	1.53	1.3

The power (in watts) in the two right columns indicates the power dissipated by that transistor if it is carrying the maximum fault current. The system designer should attempt to predict possible fault conditions for the system, and then measure the conditions on the transistors during the worse case fault(s).

For most applications involving a nominal V_{EE} of – 48 V (with a maximum of – 58 V), a maximum loop current of 30 to 40 mA, and a maximum T_A of +85°C, the MJD243 and MJD253 DPAK transistors are recommended. When mounted as described in their data sheet, they will handle both the normal loop current as well as most fault conditions. If faults are not expected to occur in a particular application, then smaller package transistors, such as MPS6717 and MPS6729, may be used. Each application must be evaluated individually when selecting the transistors.

Other possible transistors which can be considered:

PNP	NPN
MJD253-1	MJD243-1
MJE253	MJE243
MJD32	MJD31
MJD42	MJD41
MJD350	MJD340
TIP30A,B,C	TIP29A,B,C

Longitudinal Current Capability

The maximum longitudinal current which can be handled without distortion is a function of loop current, battery feed resistance, the longitudinal impedance, and the components on ST2.

Since the pass transistors cannot pass current in the reverse direction, the DC loop current provides one upper boundary for the peak longitudinal current plus peak speech signal current. The battery feed resistance determines, in effect, the DC voltage across the transistors, which is a measure of the headroom available for the circuit to handle the peak longitudinal voltage plus peak speech signal voltage. The longitudinal impedance, determined by the R_S resistors (equation 4), determines the longitudinal current for a given longitudinal voltage.

While analysis of the above items may yield one value of maximum longitudinal current, a different limit (which may be higher or lower) is imposed by the capacitor C_T, and any pulldown resistance R_T, on Pin 12 (ST2). This is due to the fact that the sense currents at TSI and RSI will be alternately mismatched as Tip and Ring move up and down together in the presence of longitudinal signals. When the longitudinals are strong, the internal fault detect circuit is activated with each 1/2 cycle, which attempts to switch ST2 low (see the section on Fault Detection). The speed at which ST2 can

switch low is a function of both the external capacitor, C_T and any pulldown resistance, R_T.

The graphs of Figures 25 and 26 indicate the maximum longitudinal current which can be handled (in Tip **and** in Ring) without distortion or causing ST2 to switch low.

PC Board Layout Considerations

PC board considerations include thermal, RFI/EMI, transient conditions, interconnection of the four wire side to the codec/filter, and others. Wirewrapped boards should be avoided — breadboarding should be done on a (at least) reasonably neat PC board.

a) Thermal

Power dissipated by the MC33120 and the two transistors must be removed to prevent excessively high junction temperatures. The equations for calculating junction temperatures are mentioned elsewhere in this data sheet. Heat is removed by both air flow and copper foil on the PC board. Since even a small amount of air flow substantially reduces junction temperatures compared to still air, tall components or other objects should not be placed such that they block air flow across the heat generating devices. Increasing, wherever possible, the area of the copper foil at the IC pins will provide additional heat removal capability. A ground plane can generally help here, while at the same time helping to reduces RFI problems.

b) RFI/EMI

While the MC33120 is intended for use at audio frequencies, the internal amplifiers have bandwidths in excess of 1.0 MHz, and can therefore respond to externally induced RFI and EMI. Interference signals can come in on the phone line, or be radiated on to the PC board from nearby radio stations or from high frequency circuitry (digital & microprocessor circuitry) in the vicinity of the line card.

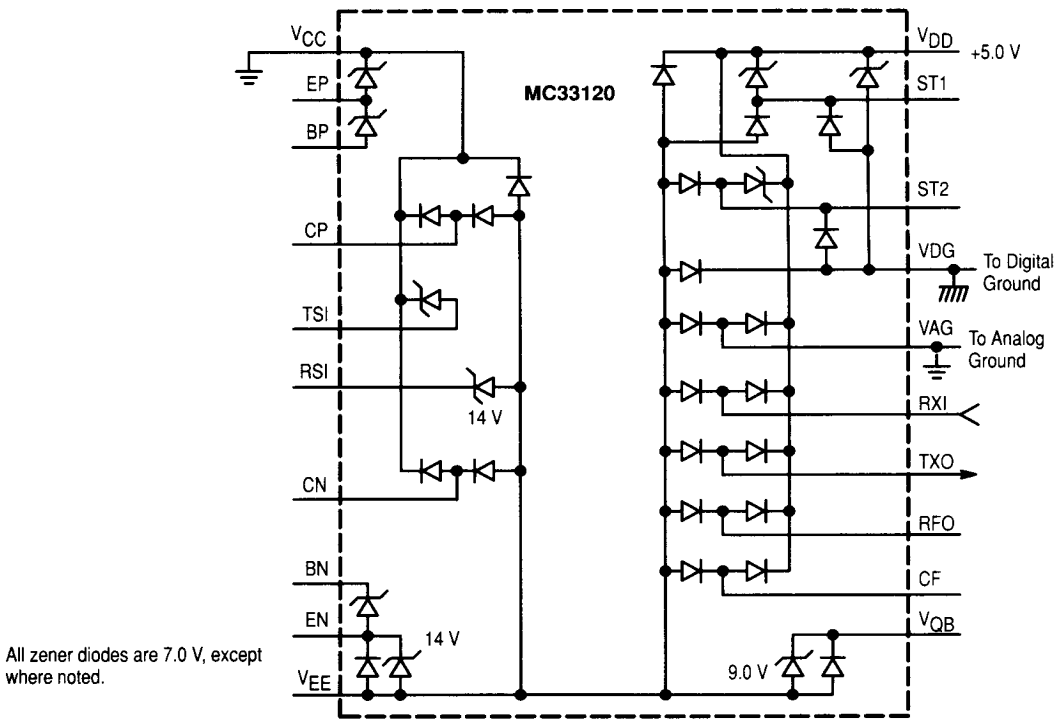
Usually RFI entering from the phone line at Tip and Ring can be removed by the compensation capacitors (C_C) provided they are connected to a good quality RF ground (generally the same ground which connects to V_{CC} on the MC33120). The ground track should be as wide and as direct as possible to minimize lead inductance. Generally better results can be obtained if an RF bleedoff to earth (or chassis) ground can be provided where the twisted pair phone line comes into the system.

To minimize problems due to noise radiating directly onto the PC board from nearby high frequency circuitry, all components associated with the MC33120 should be physically as close as possible to the IC. The most sensitive pins in this respect are the CP, CN, RSI, TSI, VAG and RXI pins. Keeping the tracks short minimizes their "antenna" effect.

c) Transient Conditions

When transient voltages come in to Tip and Ring, the transient currents, which can be several amperes, must be carried by the ground line (V_{CC}) and/or the V_{EE} line. These tracks, along with the protection and clamping devices, must be designed for these currents at the frequencies involved. If the tracks are narrow, not only may they be destroyed by the high currents, but their inductance can allow the voltage at the IC, and other nearby components, to rise to damaging levels.

FIGURE 40 — PROTECTION DIODES



All zener diodes are 7.0 V, except where noted.

The protection circuits shown in Figure 4, and in other figures in this data sheet, are such that the bulk of the transient energy is dissipated by **external** components (the protection resistors and the clamp diodes). The MC33120 has internal diodes to limit voltage excursions on the pins, and to pass a small amount of the transient current — typically less than 1.0 ampere peak. The arrangement of the diodes is shown in Figure 40.

d) Interconnection of the four-wire side

The connections on the four-wire side to the codec and other digital circuitry involves keeping digital noise out of the speech paths, and also ensuring that potentially destructive transients on Tip and Ring do not get through to the +5.0 V system.

Basically, digital connections to ST1 and ST2 should be referenced to the V_{DD} and V_{DG} pins, while the transmit and receive analog signals should be referenced to the analog ground (V_{AG}). V_{CC} should be connected to a clean battery ground, and generally should **not** be connected directly to V_{DG} and/or V_{AG} (on the line card) when strong transients are anticipated. Even with a good layout, V_{CC} can move several volts when a transient hits, possibly damaging components on the +5.0 V line **if** their grounds have a direct connection at the line card. The MC33120 is designed to allow V_{CC} to move as much as ±30 V with respect to V_{DG} and V_{AG} **on a transient basis only.** V_{CC} and the other grounds should preferably be connected together **at the power supply** rather than at the IC. Internally, the MC33120 has clamp diodes on the 4-wire side pins as shown in Figure 40.

If the codec has a single ground pin, as in Figure 41, it will be the reference for both the digital and analog signals, and must be connected to both V_{AG} and V_{DG} on the MC33120. If the codec has separate digital and analog grounds, as in Figure 42 (the MC145503 internally generates the analog ground), then each ground should be connected to the appropriate ground on the MC33120.

e) Other

A 0.1 µF capacitor should be provided across V_{CC} to V_{EE} on the MC33120 to help keep idle channel noise to a minimum.

The C_{QB} capacitor (on the V_{QB} pin) forms a pole with an internal 7.5 kΩ resistor to filter noise from the V_{EE} pin,

FIGURE 41 — CONNECTION TO A CODEC WITH A SINGLE GROUND

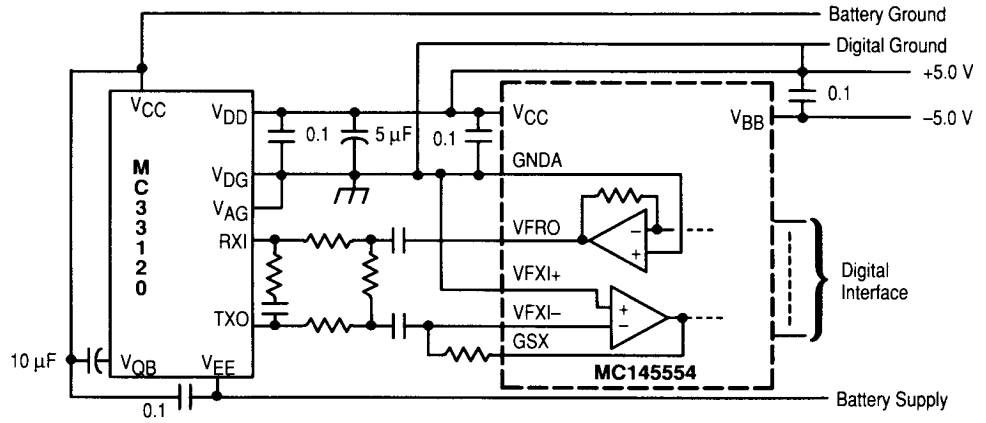
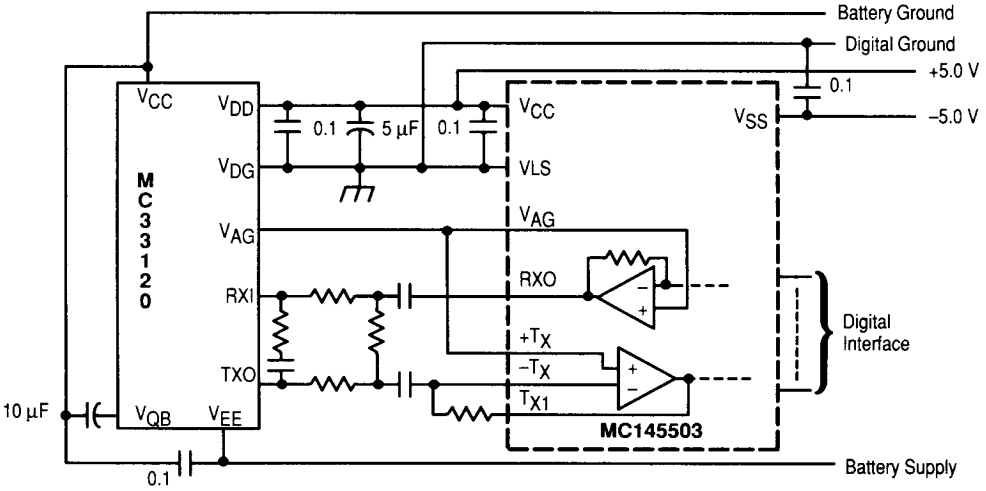


FIGURE 42 — CONNECTION TO A CODEC WITH SEPARATE GROUNDS



providing an internal quiet battery supply for the speech amplifiers. Power supply rejection will depend on the value and quality of this capacitor at the frequencies of concern. Tantalum capacitors generally have better high frequency characteristics then electrolytics. See Figure 17 and 18 for ripple rejection characteristics (the four-wire data was measured at pin 11 (TXO)). Figure 16 indicates ripple rejection from the +5.0 V supply (V_{DD}).

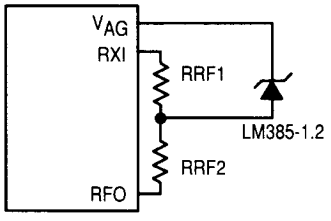
In general, PC board tracks carrying analog signals (on the four wire side and Tip/Ring) should not be routed through the digital section where they could pick up digital noise. Any tracks longer than a few inches should be considered an antenna and should be checked for potential noise or RFI pickup which could affect the circuit operation.

Alternate Circuit Configurations

a) Loop Current Limit

Replacing the RRF resistor with the circuit in Figure 43 will change the DC loop current characteristics in two ways from the graphs of Figures 5–7; a) the maximum loop current on a short line can be reduced while increasing the current on a long line, and b) the temperature dependence of the maximum current is reduced to the TC of the external reference diode.

FIGURE 43 — ALTERNATE CURRENT LIMIT CIRCUIT



The LM385-1.2 is a precision temperature stable zener diode. As the load impedance at Tip and Ring is reduced, the voltage at RFO goes increasingly negative. When the zener diode is turned on, the current into RXI is then clamped at a value determined by RRF1 and the zener diode. To calculate the two resistors, use the following procedure:

RRF1 must be >0.7 • (RRF1 + RRF2);

Determine RRF1 to set the current limit on a short line by using the following equation:

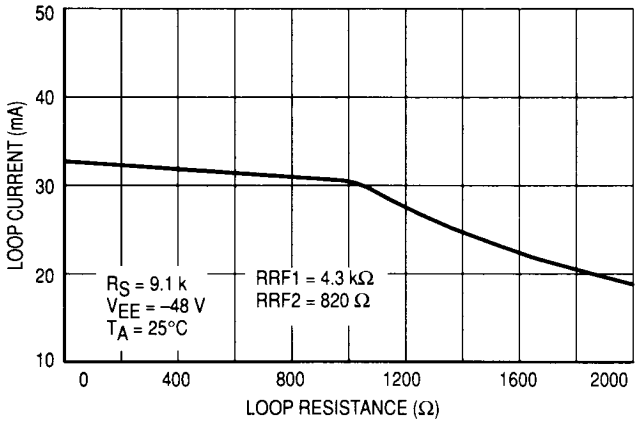
$$RRF1 = \frac{102 \bullet 1.23\ V}{I_{LOOP\ (MAX)} - 3.0\ mA} \qquad \text{(Equation 23)}$$

Then using Equation 1 calculate RRF for the long line current. RRF2 is then determined by;

$$RRF2 = RRF - RRF1 \qquad \text{(Equation 24)}$$

Figure 44 illustrates one example using the above circuit. Comparing this graph to the 5100 Ω curve of Figure 6 shows a substantial decrease in the current limit (at R_L = 0), resulting in reduced power consumption and dissipation. Use of this circuit does not affect the hookswitch or fault thresholds.

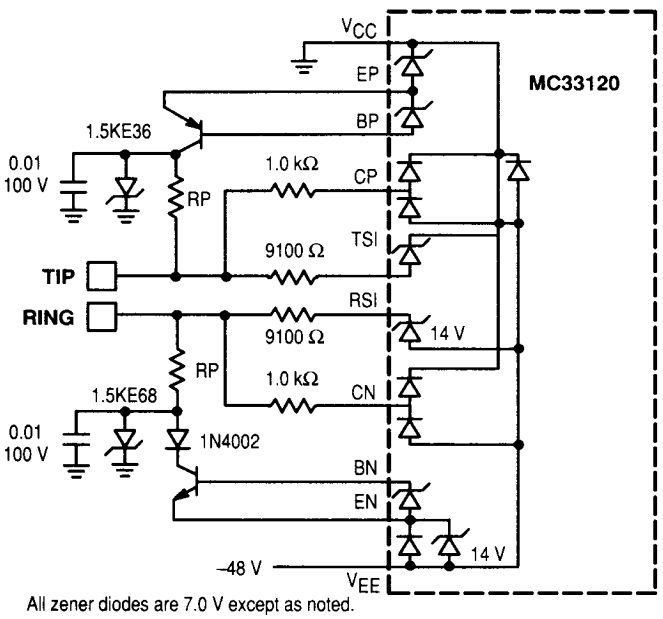
FIGURE 44 — LOOP CURRENT versus LOOP RESISTANCE ALTERNATE LOOP CURRENT LIMIT CONFIGURATION



b) Protection Scheme

The protection circuit shown in Figure 45 has the advantage of drawing ≈90% of the transient current from ground (V_{CC}) on a negative transient, rather than from the V_{EE} line as the circuit of Figure 4 does. The majority of the transient current flows through the RP resistors and the Mosorbs while a small amount (≈10%) flows through the sense resistors and the CP, CN, RSI pins. On a positive transient, all the current (except at RSI) is directed to ground. The diode in the NPN's collector prevents reverse current through the base-collector junction of the transistor during a negative transient.

FIGURE 45 — ALTERNATE PROTECTION SCHEME



All zener diodes are 7.0 V except as noted.

CIRCUIT PERFORMANCE

The following three circuits are presented as typical application examples, and the accompanying graphs indicate their measured performance. The first circuit (Figure 46) has a 600 Ω pure resistance as the AC load. The second circuit (Figures 47) has as an AC load a 900 Ω resistor in series with a 2.16 µF capacitor. The third circuit (Figure 48) has as an AC load, a complex network composed of an 820 Ω resistor in parallel with 0.115 µF, and those in series with a 220 Ω resistor. In the graphs of Figures 49–51, R_L = Return Loss, THR = Transhybrid Rejection, GTX = Transmit Gain, GRX = Receive Gain.

FIGURE 46 — 600 Ω SYSTEM

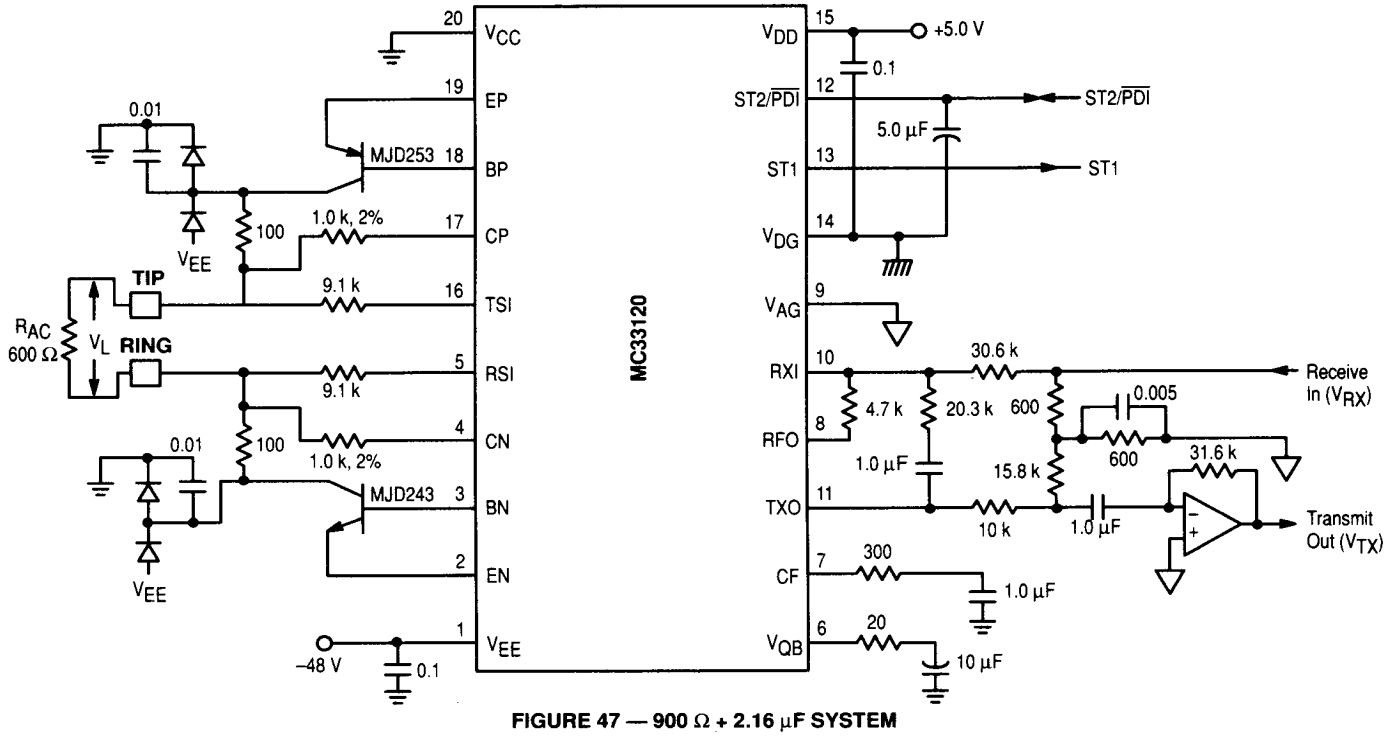


FIGURE 47 — 900 Ω + 2.16 µF SYSTEM

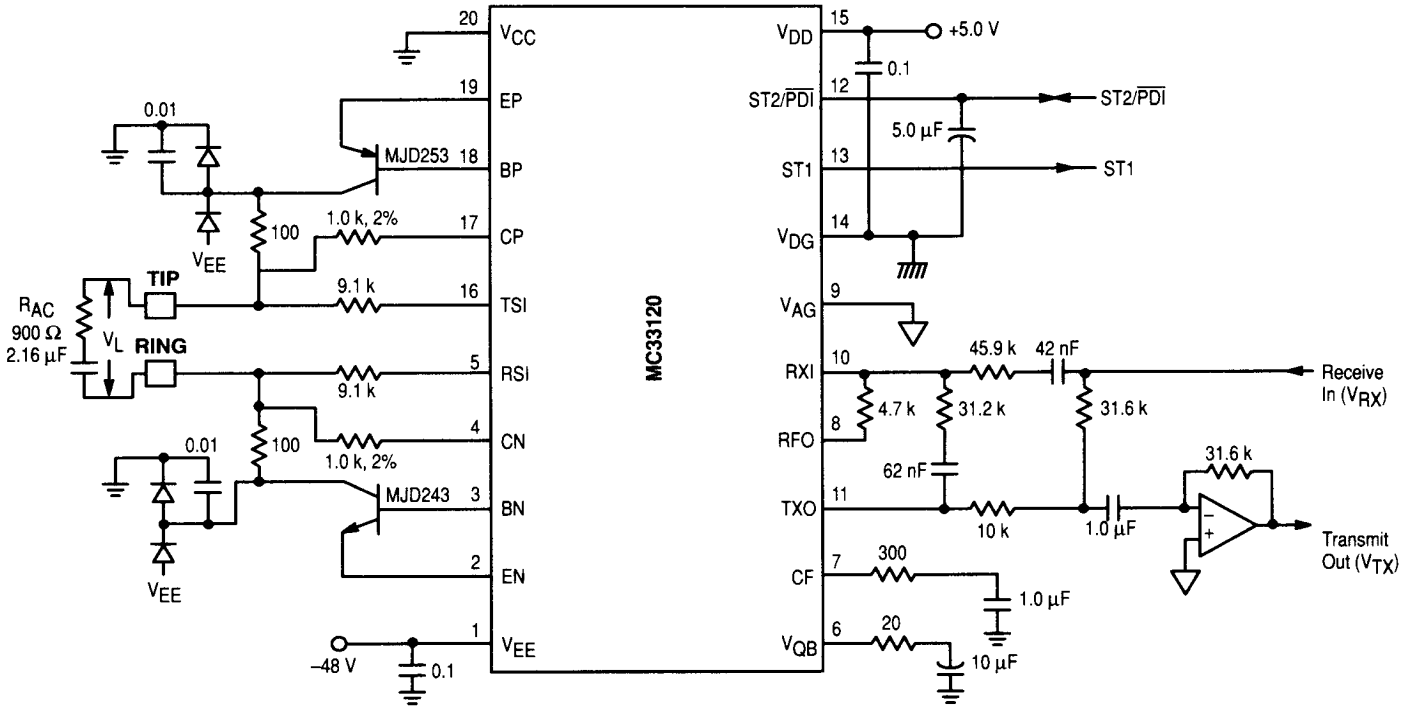


FIGURE 48 — 220 Ω + 820 Ω//0.115 μF SYSTEM

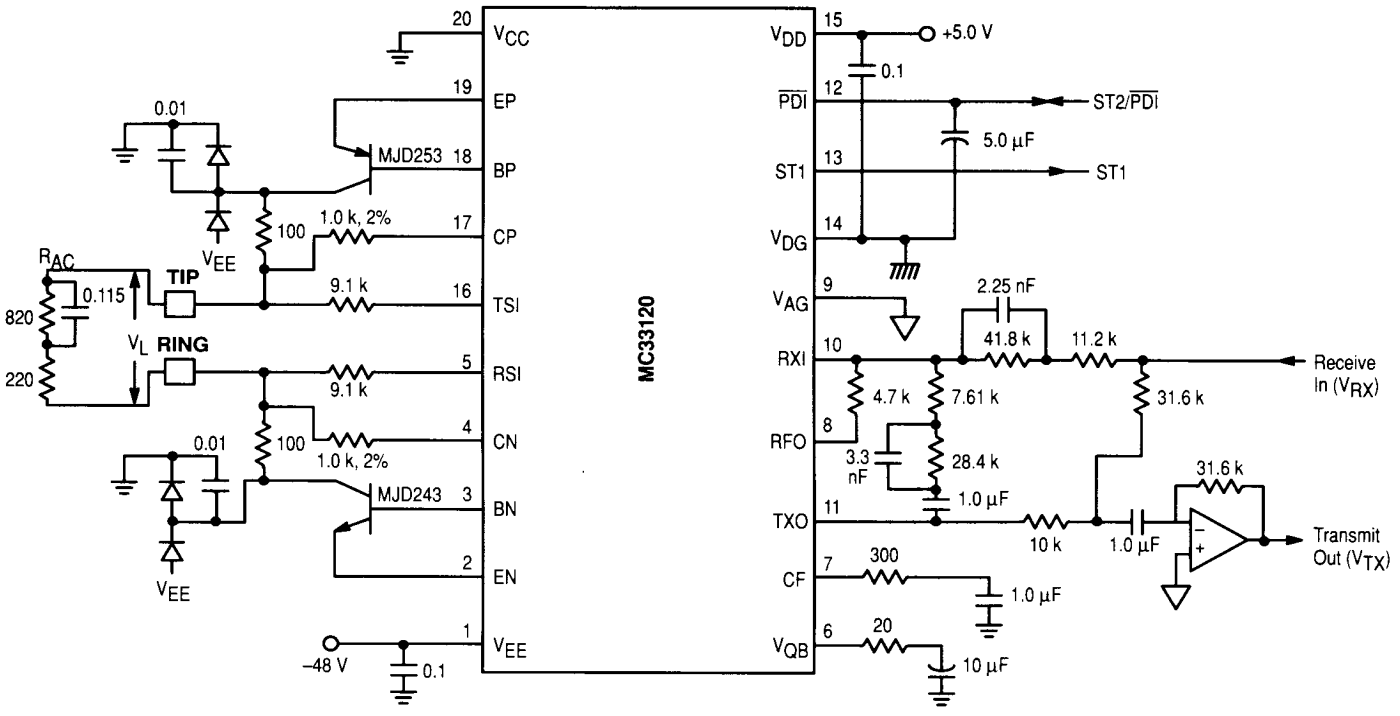


FIGURE 49 — CIRCUIT PERFORMANCE, 600 Ω SYSTEM

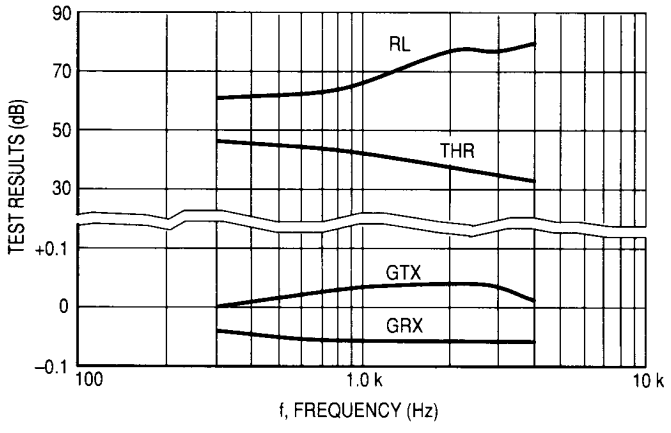


FIGURE 50 — CIRCUIT PERFORMANCE 900 Ω + 2.16 μF SYSTEM

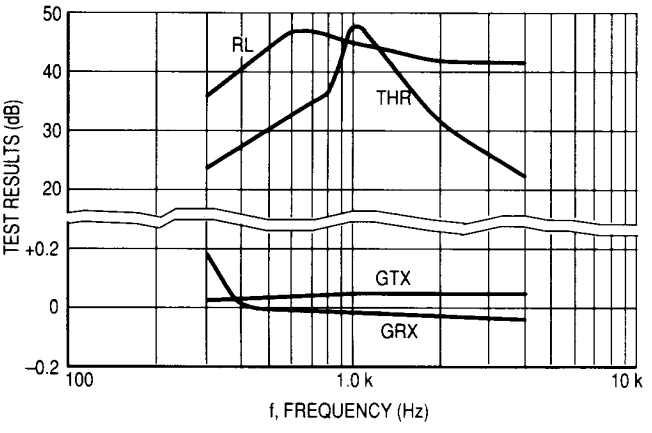


FIGURE 51 — CIRCUIT PERFORMANCE
820 Ω//0.115 μF + 220 Ω SYSTEM

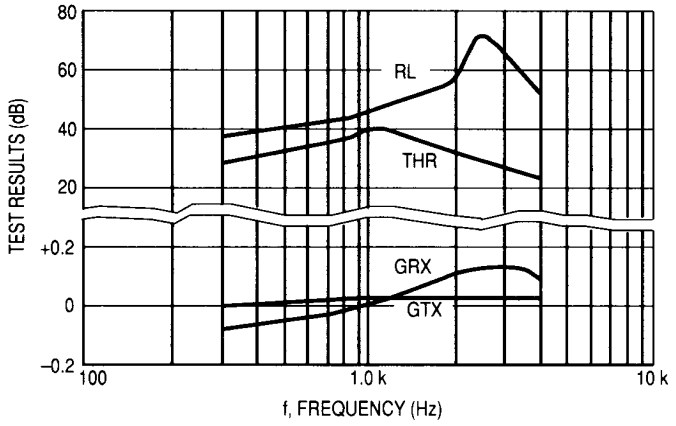
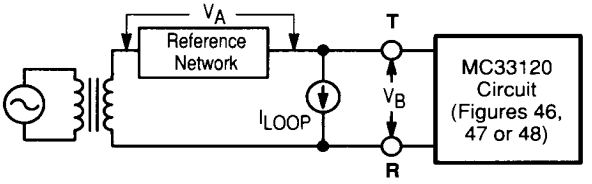


FIGURE 52 — RETURN LOSS TEST CIRCUIT
FOR FIGURES 46 TO 51



Reference Network = R_{AC} of Figures 46 to 48.
Return Loss = $20 \log \left| \frac{V_A + V_B}{V_A - V_B} \right|$

GLOSSARY

ATTENUATION — A decrease in magnitude of a communication signal, usually expressed in dB.

BALANCE NETWORK — That part of the SLIC circuit which provides transhybrid rejection.

BANDWIDTH — The range of information carrying frequencies of a communication system.

BATTERY — The voltage which provides the loop current, and in some cases powers the SLIC circuit. The name derives from the fact that COs have always used batteries, in conjunction with AC power, to provide this voltage.

BATTERY FEED RESISTANCE — The equivalent Thevenin DC resistance of the SLIC circuit for supplying loop current. Traditionally it is 400 Ω.

C-MESSAGE FILTER — A frequency weighting which evaluates the effects of noise on a typical subscriber's system.

CENTRAL OFFICE — Abbreviated CO, it is a main telephone office, usually within a few miles of its subscribers, that houses switching gear for interconnection within its exchange area, and to the rest of the telephone system. A typical CO can handle up to 10,000 subscriber numbers.

CODEC — Coder/Decoder — Interfacing between the SLIC and the digital switch, it converts the SLIC's transmit signal to digital, and converts the digital receive signal to analog.

dB — A power or voltage measurement unit, referred to another power or voltage. It is generally computed as:

$$10 \bullet \log (P_1 / P_2)$$

for power measurements, and

$$20 \bullet \log (V_1 / V_2)$$

for voltage measurements.

dBm — An indication of signal power. 1.0 mW across 600 Ω, or 0.775 V rms, is defined as 0 dBm. Any other voltage level is converted to dBm by:

dBm = 20 • log (Vrms/0.775), or
dBm = [20 • log (Vrms)] + 2.22.

dBmp — Indicates dBm measurement using a psophometric weighting filter.

dBrn — Indicates a dBm measurement relative to 1.0 pW power level into 600 Ω. Generally used for noise measurements, 0 dBrn = –90 dBm.

dBrnC — Indicates a dBrn measurement using a C-message weighting filter.

DTMF — Dual Tone Multifrequency. It is the "tone dialing" system based on outputting two non-harmonic related frequencies simultaneously to identify the number dialed. Eight frequencies have been assigned to the four rows and four columns of a keypad.

FAULT — An incorrect condition where Tip is accidentally connected to the battery voltage, or Ring is connected to ground, or both. The most common fault is Ring to ground.

FOUR WIRE CIRCUIT — The portion of a telephone, or central office, which operates on two pairs of wires. One pair is for the transmit path, and one pair is for the receive path.

FULL DUPLEX — A transmission system which permits communication in both directions simultaneously. The standard handset telephone system is full duplex.

GAIN — The change in signal amplitude (increase or decrease) after passing through an amplifier, or other circuit stage. Usually expressed in dB, an increase is a positive number, and a decrease is a negative number.

HALF DUPLEX — A transmission system which permits communication in one direction at a time. CB radios, with "push-to-talk" switches, and voice activated speakerphones, are half duplex.

HOOKSWITCH — A switch, within the telephone, which connects the telephone circuit to the subscriber loop. The name derives from old telephones where the switch was activated by lifting the receiver off and onto a hook on the side of the phone.

HYBRID — Another name for a two-to-four wire converter.

IDLE CHANNEL NOISE — Residual background noise when transmit and receive signals are absent.

LINE CARD — The PC board and circuitry in the CO or PBX which connects to the subscriber's phone line. A line card may hold circuitry for one subscriber, or a number of subscribers.

LONGITUDINAL BALANCE — The ability of the SLIC to reject longitudinal signals on Tip and Ring.

LONGITUDINAL SIGNALS — Common mode signals.

LOOP — The loop formed by the two subscriber wires (Tip and Ring) connected to the telephone at one end, and the central office (or PBX) at the other end. Generally, it is a floating system not referred to ground, or AC power.

LOOP CURRENT — The DC current which flows through the subscriber loop. It is typically provided by the central office or PBX, and ranges from 20 to 120 mA.

OFF HOOK — The condition when the telephone is connected to the phone system, permitting the loop current to flow. The central office detects the DC current as an indication that the phone is busy.

ON HOOK — The condition when the telephone is disconnected from the phone system, and no DC loop current flows. The central office regards an on-hook phone as available for ringing.

PABX — Private Automatic Branch Exchange. In effect, a miniature central office, it is a customer owned switching system servicing the phones within a facility, such as an office building. A portion of the PABX connects to the Bell (or other local) telephone system.

PROTECTION, PRIMARY — Usually consisting of carbon blocks or gas discharge tubes, it absorbs the bulk of a lightning induced transient by clamping the voltages to less than ±1500 V.

PROTECTION, SECONDARY — Usually located on the line card, it protects the SLIC and associated circuits from transient surges. Typically, it must be capable of clamping a ±1.5 kV surge of 1.0 ms duration.

PULSE DIALING — A dialing system whereby the loop current is interrupted a number of times in quick succession. The number of interruptions corresponds to the number dialed, and the interruption rate is typically 10 per second. The old rotary phones, and many new pushbutton phones, use pulse dialing.

RECEIVE PATH — Within the CO or PBX it is the speech path from the internal switching system towards the phone line (Tip & Ring).

REN — Ringer Equivalence Number. An indication of the impedance or loading factor of a telephone bell or ringer circuit. An REN of 1.0 equals ≈8.0 kΩ. The Bell system typically permits a maximum of 5.0 REN (1.6 kΩ) on an individual subscriber line. A minimum REN of 0.2 (40 kΩ) is required by the Bell system.

RETURN LOSS — Expressed in dB, it is a measure of how well the SLIC's AC impedance matches the line's AC characteristic impedance. With a perfect match, there is no reflected signal, and therefore infinite return loss. It is calculated from:

$$RL = 20 \bullet \log \frac{(Z_{LINE} + Z_{CKT})}{(Z_{LINE} - Z_{CKT})}$$

RING — One of the two wires connecting the central office to a telephone. The name derives from the ring portion of the plugs used by operators (in older equipment) to make the connection. Ring is traditionally negative with respect to Tip.

SLIC — Subscriber Line Interface Circuit. It is the circuitry within the CO or PBX which connects to the user's phone line.

SUBSCRIBER — The customer at the telephone end of the line.

SUBSCRIBER LINE — The system consisting of the user's telephone, the interconnecting wires, and the central office equipment dedicated to that subscriber (also referred to as a loop).

TIP — One of the two wires connecitng the central office to a telephone. The name derives from the tip of the plugs used by operators (in older equipment) to make the connection. Tip is traditionally positive with respect to Ring.

TRANSHYBRID REJECTION — The rejection (in dB) of the reflected signal in the transmit path resulting from a receive signal applied to the SLIC.

TRANSMIT PATH — Within the CO or PBX it is the speech path from the phone line (Tip & Ring) towards the internal switching system.

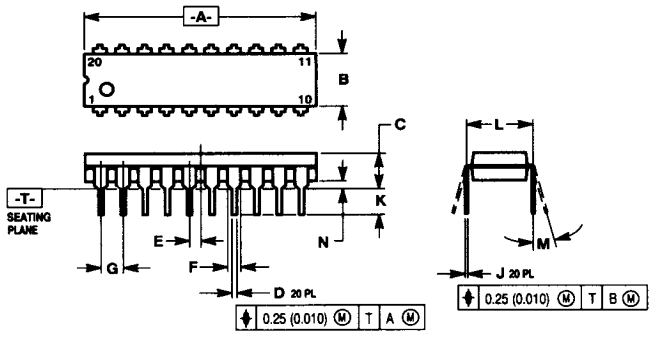
TWO WIRE CIRCUIT — Refers to the two wires connecting the central office to the subscriber's telephone. Commonly referred to as Tip and Ring, the two wires carry both transmit and receive signals in a differential manner.

TWO-TO-FOUR WIRE CONVERTER — A circuit which has four wires (on one side) — two (signal & ground) for the outgoing signal, and two for the incoming signal. The outgoing signal is sent out differentially on the two wire side (the other side), and incoming differential signals received on the two wire side are directed to the four wire side. Additional circuit within cancels the reflected outgoing signal to keep it separate from the incoming signal.

VOICEBAND — That portion of the audio frequency range used for transmission across the telephone system. Typically it is 300 to 3400 Hz.

OUTLINE DIMENSIONS

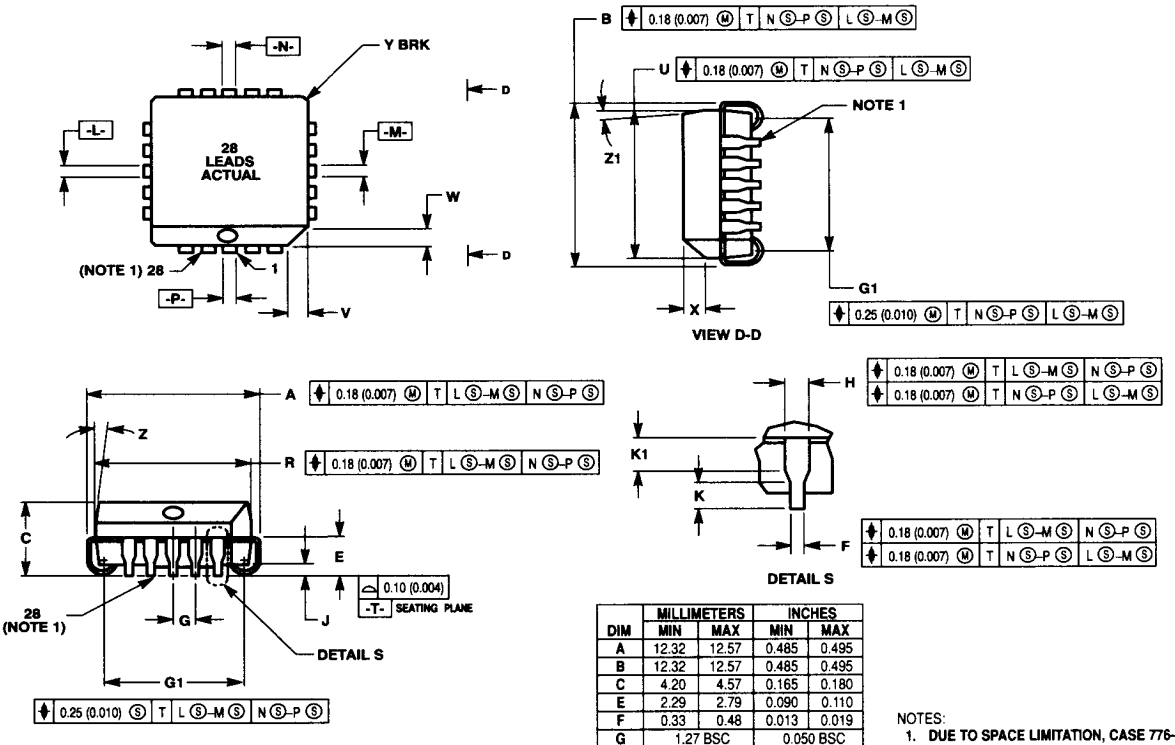
P SUFFIX
PLASTIC PACKAGE
CASE 738-03



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION "L" TO CENTER OF LEAD WHEN FORMED PARALLEL.
4. DIMENSION "B" DOES NOT INCLUDE MOLD FLASH.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	25.66	27.17	1.010	1.070
B	6.10	6.60	0.240	0.260
C	3.81	4.57	0.150	0.180
D	0.39	0.55	0.015	0.022
E	1.27 BSC		0.050 BSC	
F	1.27	1.77	0.050	0.070
G	2.54 BSC		0.100 BSC	
J	0.21	0.38	0.008	0.015
K	2.80	3.55	0.110	0.140
L	7.62 BSC		0.300 BSC	
M	0°	15°	0°	15°
N	0.51	1.01	0.020	0.040

FN SUFFIX
PLCC
CASE 776-02



	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	12.32	12.57	0.485	0.495
B	12.32	12.57	0.485	0.495
C	4.20	4.57	0.165	0.180
E	2.29	2.79	0.090	0.110
F	0.33	0.48	0.013	0.019
G	1.27 BSC		0.050 BSC	
H	0.66	0.81	0.026	0.032
J	0.51	—	0.020	—
K	0.64	—	0.025	—
R	11.43	11.58	0.450	0.456
U	11.43	11.58	0.450	0.456
V	1.07	1.21	0.042	0.048
W	1.07	1.21	0.042	0.048
X	1.07	1.42	0.042	0.056
Y	—	0.50	—	0.020
Z	2	10	2	10
G1	10.42	10.92	0.410	0.430
K1	1.02	—	0.040	—
Z1	2	10	2	10

NOTES:
1. **DUE TO SPACE LIMITATION, CASE 776-02 SHALL BE REPRESENTED BY A GENERAL (SMALLER) CASE OUTLINE DRAWING RATHER THAN SHOWING ALL 28 LEADS.**
2. DATUMS -L-, -M-, -N-, AND -P- DETERMINED WHERE TOP OF LEAD SHOULDER EXIT PLASTIC BODY AT MOLD PARTING LINE.
3. DIM G1, TRUE POSITION TO BE MEASURED AT DATUM -T-, SEATING PLANE.
4. DIM R AND U DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTRUSION IS 0.25 (0.010) PER SIDE.
5. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
6. CONTROLLING DIMENSION: INCH.