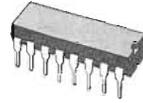


4-BIT SHIFT REGISTER WITH 3-STATE OUTPUTS

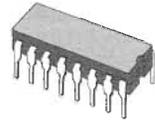
- SHIFT LEFT OR PARALLEL 4-BIT REGISTER
- 3-STATE OUTPUTS
- INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS
- FULLY TTL AND CMOS COMPATIBLE

DESCRIPTION

The T74LS395A is a 4-Bit Registers with 3-state outputs and can operate in either a synchronous parallel load or a serial shift-right mode, as determined by the Select input. An asynchronous active LOW Master Reset (MR) input overrides the synchronous operations and clears the register. An active Low Outputs Enable (OE) input controls the 3-state output buffer, but does not interfere with the operations. The fourth stage also has a conventional output for linking purposes in multistage serial operations.



B1
(Plastic Package)



D1
(Ceramic Package)



M1
(Micro Package)

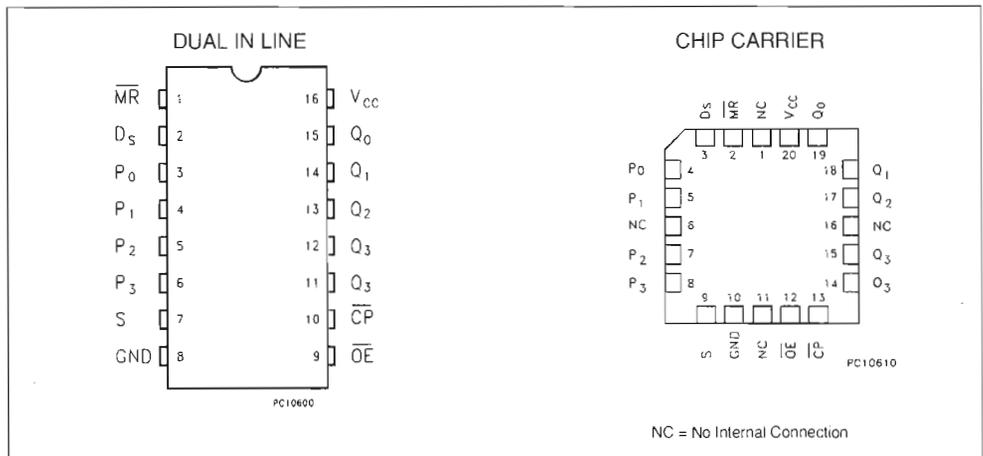


C1
(Plastic Chip Carrier)

ORDER CODES :

T74LS395A D1 T74LS395A C1
 T74LS395A B1 T74LS395A M1

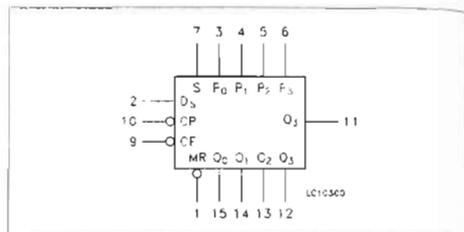
PIN CONNECTION (top view)



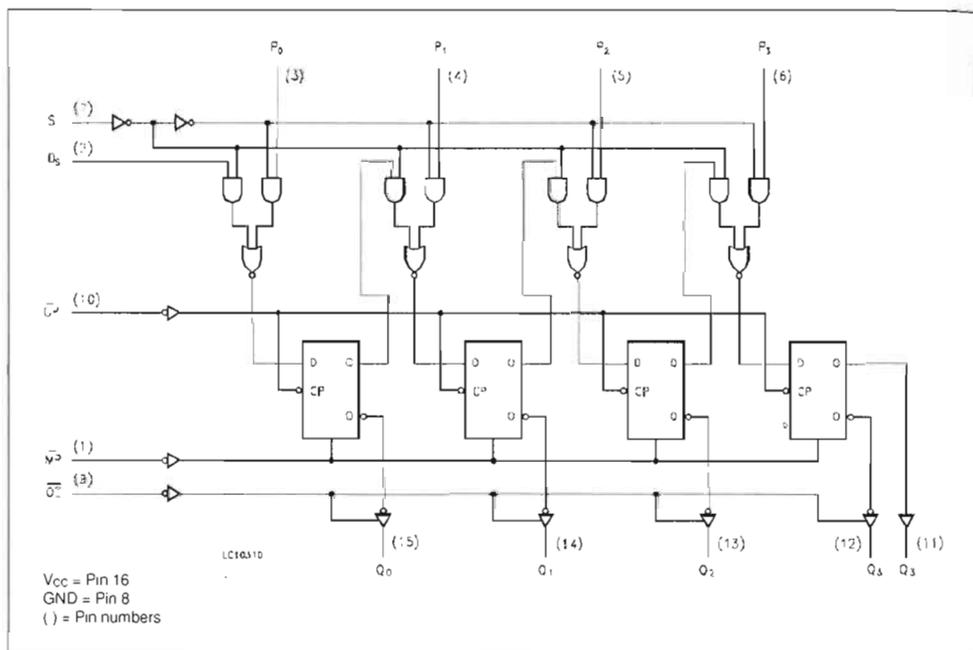
PIN NAMES

P ₀ -P ₃	Parallel Inputs
D _S	Serial Data Inputs
S	Mode Select Input
CP	Clock (Active LOW) Input
MR	Master Reset (Active LOW) Input
OE	Output Enable (Active LOW) Input
Q ₀ -Q ₃	3-State Register Outputs
Q ₃	Register Output

LOGIC SYMBOL



LOGIC DIAGRAM



FUNCTIONAL DESCRIPTION

The LS395A contains four D-type edge-triggered flip-flop and auxiliary gating to select a D input either from a Parallel (P_n) input or from the preceding stage. When the Select input is HIGH, the P_n inputs are enabled. A LOW signal on the S input enables the serial inputs for shift-right operations, as indicated in the Truth Table.

Stage changes are initiated by HIGH to LOW transitions on the Clock Pulse (CP) input. Signals on the P_n, D_S and S inputs can change when the Clock is in either state, provided that the recommended set-

up and hold times are observed. When the S input is LOW, a CP HIGH-LOW transition transfers data from Q₀ to Q₁, Q₁ to Q₂ and Q₂ to Q₃. A left-shift is accomplished by connecting the outputs back to the P_n inputs but offset one place to the left, i.e., O₃ to P₂, O₂ to P₁ and O₁ to P₀, with P₃ acting as the linking input from another package.

When the \overline{OE} input is HIGH, the output buffers are disable and O₀ - O₃ outputs are in a high impedance condition. The shifting, parallel loading or resetting operations can still be accomplished, however.

MODE SELECT - TRUTH TABLE

Operating Mode	Inputs @ t_n					Outputs @ t_{n+1}			
	MR	CP	S	D _s	P _n	O ₀	O ₁	O ₂	O ₃
Asynchronous Reset	L	X	X	X	X	L	L	L	L
Shift, SET First Stage	H	\overline{L}	L	H	X	H	O _{0n}	O _{1n}	O _{2n}
Shift, RESET First Stage	H	\overline{L}	L	L	P _n	L	O _{0n}	O _{1n}	O _{2n}
Shift, Parallel Load	H	\overline{L}	H	X	X	P ₀	P ₁	P ₂	P ₃

H = HIGH Voltage Level

L = LOW Voltage Level

X = Don't Care

t_n, t_{n+1} = time before and after CP HIGH to LOW transitionNOTE: When OE is LOW, outputs O₀-O₃ are in the high impedance state, however, this does not affect other operation or the O₃ output.

ABSOLUTE MAXIMUM RATING

Symbol	Parameter	Value	Unit
V _{CC}	Supply Voltage	- 0.5 to 7	V
V _I	Input Voltage, Applied to Input	- 0.5 to 15	V
V _O	Output Voltage, Applied to Output	- 0.5 to 10	V
I _I	Input Current, Into Inputs	- 30 to 5	mA
I _O	Output Current, Into Outputs	50	mA

Stresses in excess of those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions in excess of those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

GUARANTEED OPERATING RANGE

Part Numbers	Supply Voltage			Temperature
	Min.	Typ.	Max.	
T74LS395AXX	4.75 V	5.0 V	5.25 V	0 °C to + 70 °C

XX = package type.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

Symbol	Parameter		Limits			Test Condition (note 1)	Unit
			Min.	Typ. (*)	Max.		
V _{IH}	Input HIGH Voltage		2.0			Guaranteed Input HIGH Voltage for All Input	V
V _{IL}	Input LOW Voltage				0.8	Guaranteed Input LOW Voltage for All Input	V
V _{CD}	Input Clamp Diode Voltage				- 1.5	V _{CC} = MIN, I _{IN} = -18 mA	V
V _{OH}	Output HIGH Voltage	Q ₀ , Q ₁ , Q ₂ , Q ₃	2.4			I _{OH} = -2.6 mA V _{CC} = MIN, V _{IH} = 2.0 V V _{IL} = V _{ILmax}	V
		Q ₃	2.7			I _{OH} = -400 μA	
V _{OL}	Output LOW Voltage	Q ₀ , Q ₁ , Q ₂ , Q ₃		0.35	0.5	I _{OL} = 24 mA V _{CC} = MIN, V _{IH} = 2.0 V V _{IL} = V _{IL max}	V
		Q ₃		0.35	0.5	I _{OL} = 8.0 mA	
I _{ozH}	Output Off Current HIGH	Q ₀ , Q ₁ , Q ₂ , Q ₃			20	V _{CC} = MAX, V _{OUT} = 2.7 V V _E = 2.0 V	μA
I _{ozL}	Output Off Current LOW	Q ₀ , Q ₁ , Q ₂ , Q ₃			- 20	V _{CC} = MAX, V _{OUT} = 0.5 V V _E = 2.0 V	μA
I _{IH}	Input HIGH Current				20	V _{CC} = MAX, V _{IN} = 2.7 V V _{CC} = MAX, V _{IN} = 7.0 V	μA mA
					0.1		
I _{IL}	Input LOW Current				- 0.4	V _{CC} = MAX, V _{IN} = 0.4 V	mA
I _{OS}	Output Short Circuit Current (note 2)	Q ₀ , Q ₁ , Q ₂ , Q ₃	- 30		- 130	V _{CC} = MAX, V _{OUT} = 0 V	mA
		Q ₃	- 20		- 100		
I _{CC}	Power Supply Current				34	Cond. a Cond. b	V _{CC} = MAX (See Note 3)
					31		

- Notes :**
- Conditions for testing, not shown in the Table, are chosen to guarantee operation under "worst case" conditions
 - Not more than one output should be shorted at a time.
 - I_{CC} is measured with the outputs open, DS input and S input at 4.5 V and Pn inputs grounded under the following conditions:
 - OE at 4.5 V and a 3 V positive pulse applied to CP input.
 - OE and CP input grounded.
- (*) Typical values are at V_{CC} = 5.0 V, T_A = 25 °C.

AC CHARACTERISTICS: $T_A = 25^\circ\text{C}$

Symbol	Parameter	Limits			Test Conditions	Units
		Min.	Typ.	Max.		
f_{MAX}	Maximum Clock Frequency	30	45		O_0, O_1, O_2, O_3 outputs: $R_L = 667\ \Omega$ $C_L = 45\ \text{pF}$ O_3 output: $R_L = 2.0\ \text{K}\Omega$ $C_L = 15\ \text{pF}$ $C_L = 5\ \text{pF}$	MHz
t_{PHL}	Propagation Delay, High to Low Level Output from Clear		22	35		ns
t_{PLH}	Propagation Delay Time Low to High Level Output		15	30		ns
t_{PHL}	Propagation Delay Time High to Low Level Output		20	30		ns
t_{PZH}	Output Enable Time to High Level		15	25		ns
t_{PZL}	Output Enable Time to Low Level		17	25		ns
t_{PHZ}	Output Disable Time from High Level		11	17		ns
t_{PLZ}	Output Disable Time from Low Level		12	20		ns

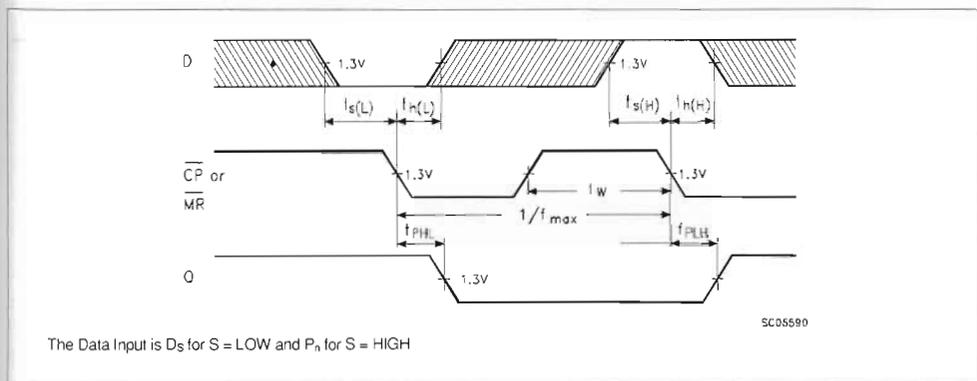
AC SET-UP REQUIREMENTS: $T_A = 25^\circ\text{C}$

Symbol	Parameter		Limits			Test Conditions	Units
			Min.	Typ.	Max.		
$t_w(\text{CP})$	Clock Pulse Width		16			$V_{\text{CC}} = 5.0\ \text{V}$	ns
t_s^*	Set-up Time	Load/Shift Input	40				ns
		All other Inputs	20				ns
t_h^*	Hold Time		10			ns	

* High or Low Level Data

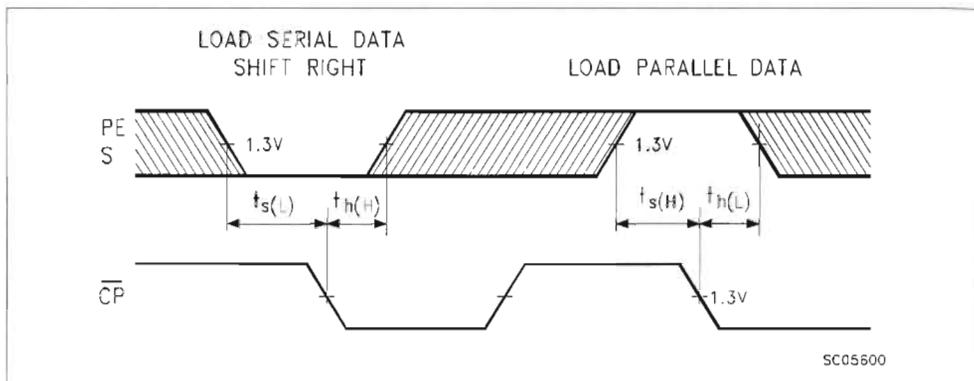
AC WAVEFORMS AND LOAD CIRCUIT

Figure 1

The Data Input is D_S for S = LOW and D_H for S = HIGH

The shaded areas indicate when the input is permitted to change for predictable output performance.

Figure 2



The shaded areas indicate when the input is permitted to change for predictable output performance.

Figure 3

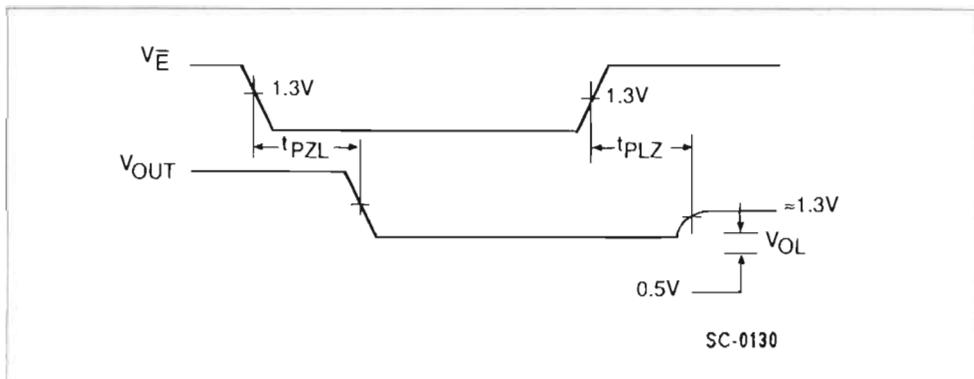


Figure 4

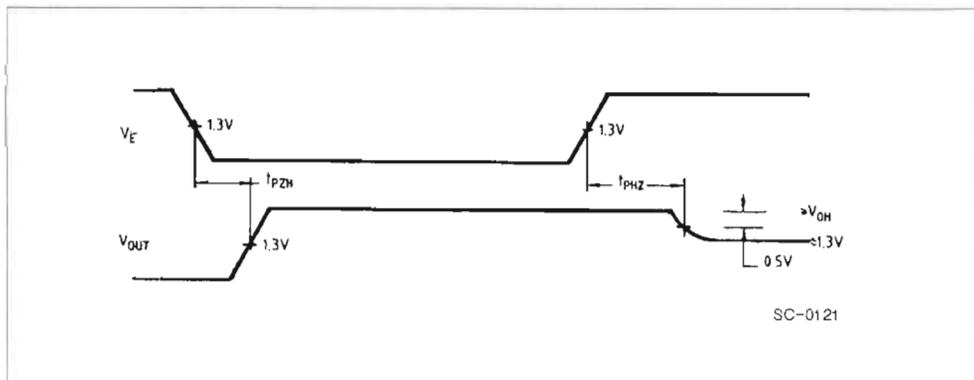
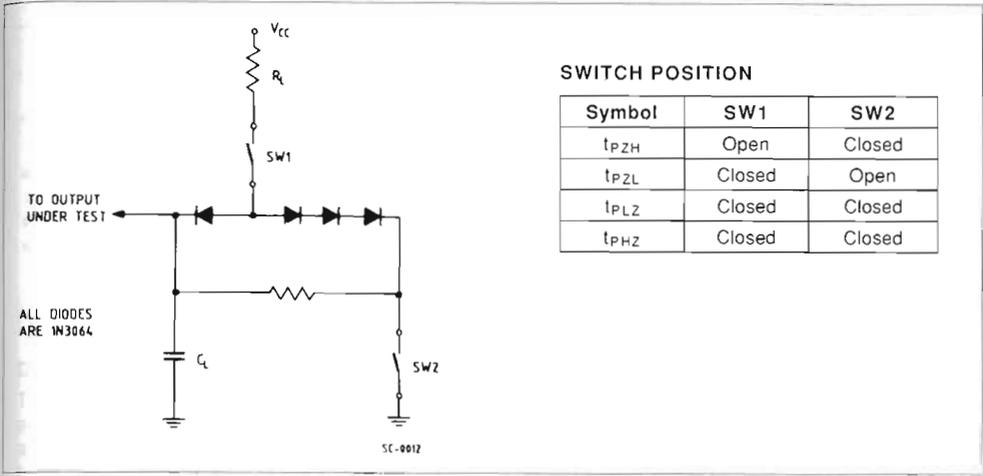


Figure 5.



SWITCH POSITION

Symbol	SW1	SW2
t_{PZH}	Open	Closed
t_{PZL}	Closed	Open
t_{PLZ}	Closed	Closed
t_{PHZ}	Closed	Closed