

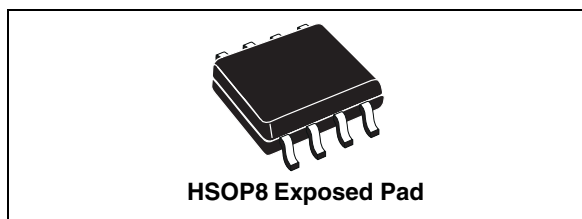
## 2.5A switch step down switching regulator

### General features

- 2.5A Internal switch
- Operating input voltage from 4V to 36V
- 3.3V / ( $\pm 2\%$ ) reference voltage
- Output voltage adjustable from 1.235V to 35V
- Low dropout operation: 100% duty cycle
- 250KHz Internally fixed frequency
- Voltage feedforward
- Zero load current operation
- Internal current limiting
- Inhibit for zero current consumption
- Synchronization
- Protection against feedback disconnection
- Thermal shutdown

### Applications

- Consumer: STB, DVD, TV, VCR, car radio, LCD monitors
- Networking: XDSL, modems, DC-DC modules
- Computer: printers, audio/graphic cards, optical storage, hard disk drive
- Industrial: changers, car battery, DC-DC converters



### Description

The L5973D is a step down monolithic power switching regulator with a minimum switch current limit of 2.5A so it is able to deliver more than 2A DC current to the load depending on the application conditions.

The output voltage can be set from 1.235V to 35V.

The high current level is also achieved thanks to an SO8 package with exposed frame, that allows to reduce the  $R_{th(j-amb)}$  down to approximately  $40^{\circ}\text{C/W}$ .

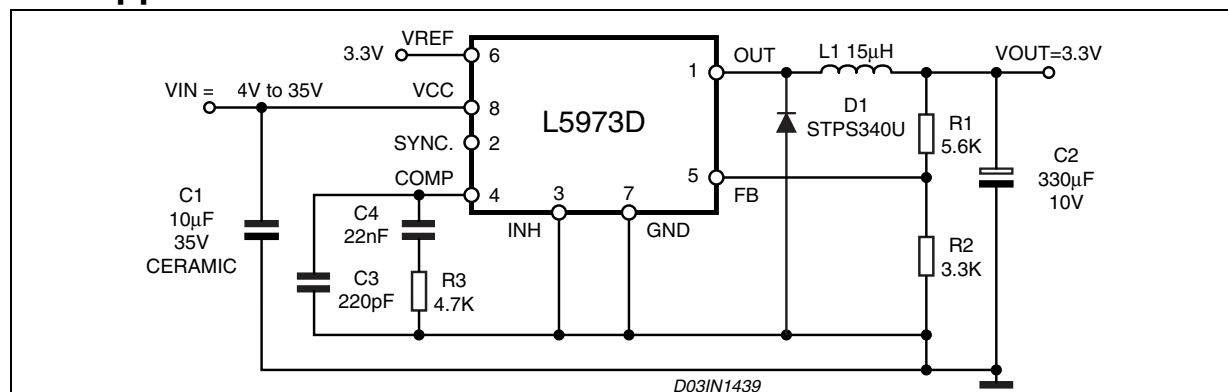
The device uses an internal P-Channel D-MOS transistor (with a typical  $R_{dson}$  of 250mW) as switching element to minimize the size of the external components.

An internal oscillator fixes the switching frequency at 250KHz.

Having a minimum input voltage of 4V only, it is particularly suitable for 5V bus, available in all computer related applications.

Pulse by pulse current limit with the internal frequency modulation offers an effective constant current short circuit protection.

### Test application circuit



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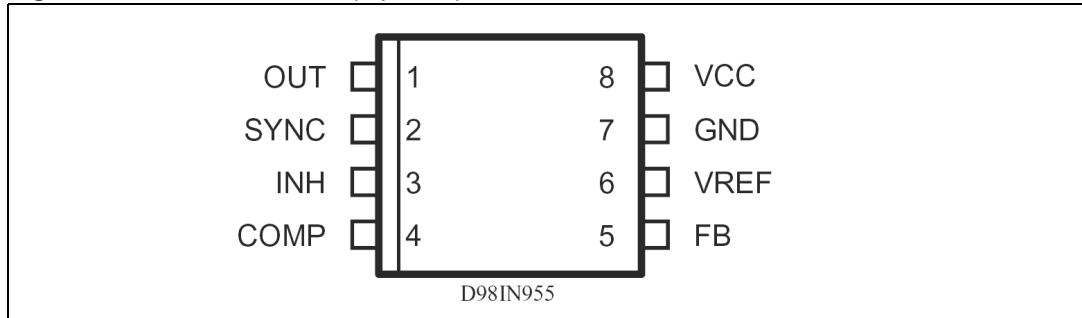
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# 1 Pin settings

## 1.1 Pin connection

Figure 1. Pin connection (top view)



## 1.2 Pin description

Table 1. Pin description

N°	Type	Description
1	OUT	Regulator Output.
2	SYNC	Master/slave synchronization.
3	INH	A logical signal (active high) disables the device. If INH not used the pin must be grounded. When it is open an internal pull-up disable the device.
4	COMP	E/A output for frequency compensation.
5	FB	Feedback input. Connecting directly to this pin results in an output voltage of 1.23V. An external resistive divider is required for higher output voltages.
6	VREF	3.3V $V_{REF}$ No cap is requested for stability.
7	GND	Ground.
8	VCC	Unregulated DC input voltage.

## 2 Electrical data

### 2.1 Maximum ratings

**Table 2. Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_8$	Input Voltage	40	V
$V_1$	Output DC voltage Output peak voltage at $t = 0.1\mu\text{s}$	-1 to 40 -5 to 40	V V
$I_1$	Maximum output current	int. limit.	
$V_4, V_5$	Analog pins	4	V
$V_3$	INH	-0.3V to $V_{CC}$	
$V_2$	SYNC	-0.3 to 4	V
$P_{tot}$	Power dissipation at $T_A \leq 60^\circ\text{C}$	2.25	W
$T_j$	Operating junction temperature range	-40 to 150	$^\circ\text{C}$
$T_{stg}$	Storage temperature range	-55 to 150	$^\circ\text{C}$

### 2.2 Thermal data

**Table 3. Thermal data**

Symbol	Parameter	HSOP8 Exposed Pad	Unit
$R_{thJA}$	Maximum thermal resistance junction-ambient	40 <sup>(1)</sup>	$^\circ\text{C/W}$

1. Package mounted on board

### 3 Electrical characteristics

**Table 4. Electrical characteristics** ( $T_J = 25^\circ\text{C}$ ,  $V_{CC} = 12\text{V}$ , unless otherwise specified)

Symbol	Parameter	Test condition	Min	Typ	Max	Unit	
$V_{CC}$	Operating input voltage range	$V_o = 1.235\text{V}$ ; $I_o = 2\text{A}$	(1)	4		36	V
$R_{DS(on)}$	Mosfet on Resistance		(1)		0.250	0.5	$\Omega$
$I_l$	Maximum limiting current	$V_{CC} = 4.4\text{V}$ to $36\text{V}$		2.5	3	3.5	A
$f_s$	Switching frequency		(1)	212	250	280	KHz
				225	250	275	KHz
	Duty cycle			0		100	%
<b>Dynamic characteristics</b> (see test circuit ).							
$V_5$	Voltage feedback	$4.4\text{V} < V_{CC} < 36\text{V}$ , $20\text{mA} < I_o < 2\text{A}$		1.220	1.235	1.25	V
			(1)	1.198	1.235	1.272	V
$h$	Efficiency	$V_o = 5\text{V}$ , $V_{CC} = 12\text{V}$			90		%
<b>DC characteristics</b>							
$I_{qop}$	Total operating quiescent current		(1)		3	5	mA
$I_q$	Quiescent current	Duty Cycle = 0; $V_{FB} = 1.5\text{V}$				2.5	mA
$I_{qst-by}$	Total stand-by quiescent current	$V_{inh} > 2.2\text{V}$	(1)		50	100	$\mu\text{A}$
		$V_{CC} = 36\text{V}$ ; $V_{inh} > 2.2\text{V}$	(1)		80	150	$\mu\text{A}$
<b>Inhibit</b>							
	INH threshold voltage	Device ON				0.8	V
		Device OFF		2.2			V
<b>Error amplifier</b>							
$V_{OH}$	High level output voltage	$V_{FB} = 1\text{V}$		3.5			V
$V_{OL}$	Low level output voltage	$V_{FB} = 1.5\text{V}$				0.4	V
$I_o$ source	Source output current	$V_{COMP} = 1.9\text{V}$ ; $V_{FB} = 1\text{V}$		200	300		$\mu\text{A}$
$I_o$ sink	Sink output current	$V_{COMP} = 1.9\text{V}$ ; $V_{FB} = 1.5\text{V}$		1	1.5		mA

**Table 4. Electrical characteristics** (  $T_J = 25^\circ\text{C}$ ,  $V_{CC} = 12\text{V}$ , unless otherwise specified)

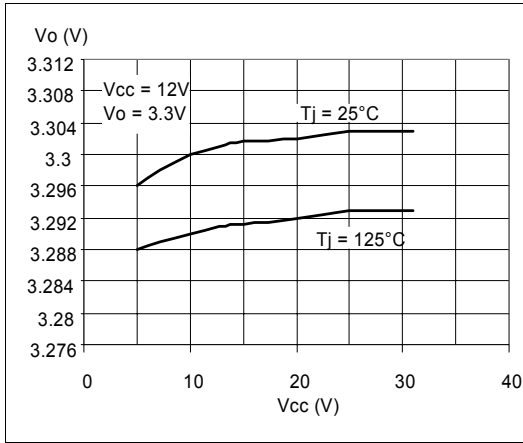
Symbol	Parameter	Test condition	Min	Typ	Max	Unit
$I_b$	Source bias current			2.5	4	$\mu\text{A}$
	DC open loop gain	$R_L = \infty$	50	57		dB
gm	Transconductance	$I_{\text{comp}} = -0.1\text{mA}$ to $0.1\text{mA}$ $V_{\text{COMP}} = 1.9\text{V}$		2.3		mS
<b>Sync function</b>						
	High input voltage	$V_{CC} = 4.4\text{V}$ to $36\text{V}$	2.5		$V_{\text{REF}}$	V
	Low input voltage	$V_{CC} = 4.4\text{V}$ to $36\text{V}$			0.74	V
	Slave sink current	$V_{\text{sync}} = 0.74\text{V}$ <sup>(2)</sup> $V_{\text{sync}} = 2.33\text{V}$	0.11 0.21		0.25 0.45	mA mA
	Master output amplitude	$I_{\text{source}} = 3\text{mA}$	2.75	3		V
	Output pulse width	no load, $V_{\text{sync}} = 1.65\text{V}$	0.20	0.35		$\mu\text{s}$
<b>Reference section</b>						
	Reference voltage		3.234	3.3	3.366	V
		$I_{\text{REF}} = 0$ to $5\text{mA}$ $V_{CC} = 4.4\text{V}$ to $36\text{V}$	(1) 3.2	3.3	3.399	V
	Line regulation	$I_{\text{REF}} = 0\text{mA}$ $V_{CC} = 4.4\text{V}$ to $36\text{V}$		5	10	mV
	Load regulation	$I_{\text{REF}} = 0$ to $5\text{mA}$		8	15	mV
	Short circuit current		10	18	30	mA

1. Specification Referred to  $T_J$  from  $-40$  to  $125^\circ\text{C}$ . Specification over the  $-40$  to  $+125$   $T_J$  Temperature range are assured by design, characterization and statistical correlation.

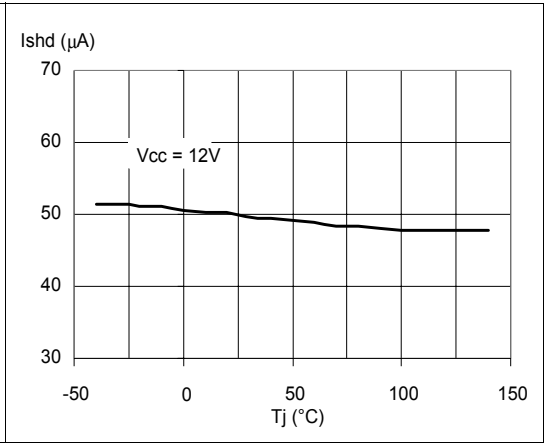
2. Guaranteed by design.

# 4 Typical characteristics

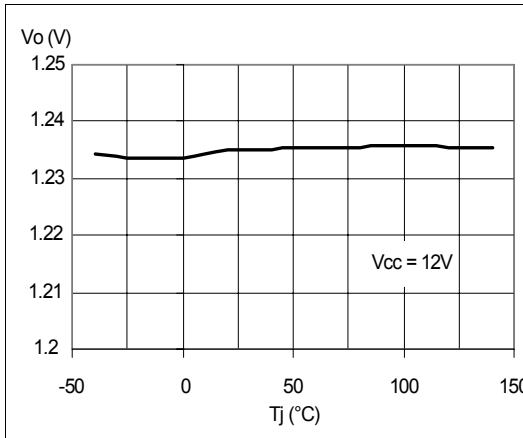
**Figure 2. Line regulation**



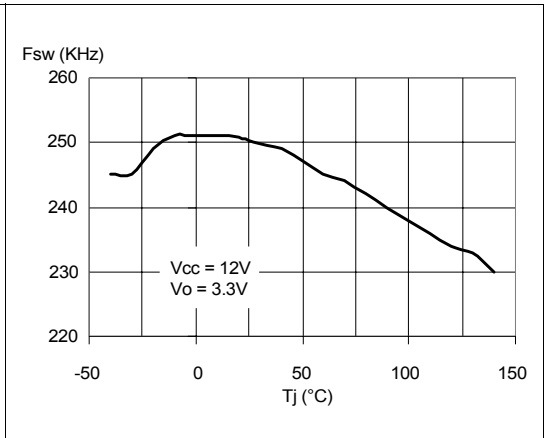
**Figure 3. Shutdown current vs. junction temperature**



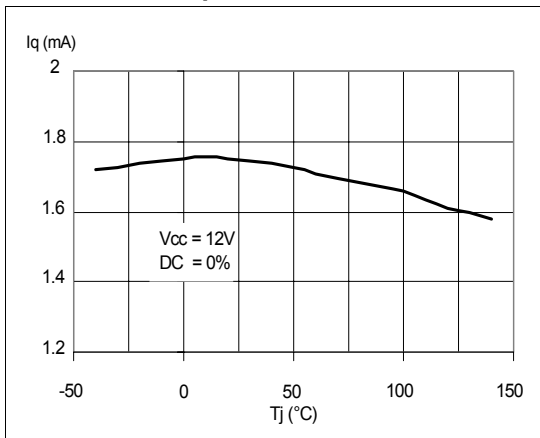
**Figure 4. Output voltage vs. junction temperature**



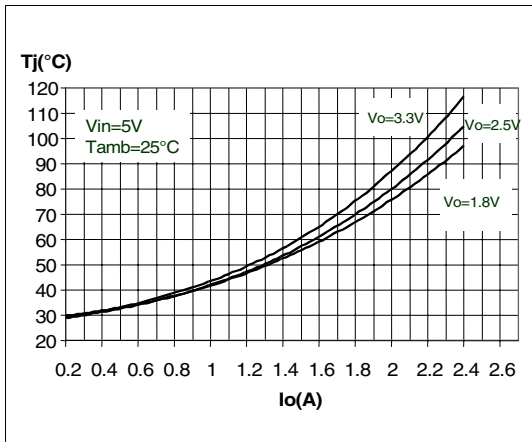
**Figure 5. Switching frequency vs. junction temperature**



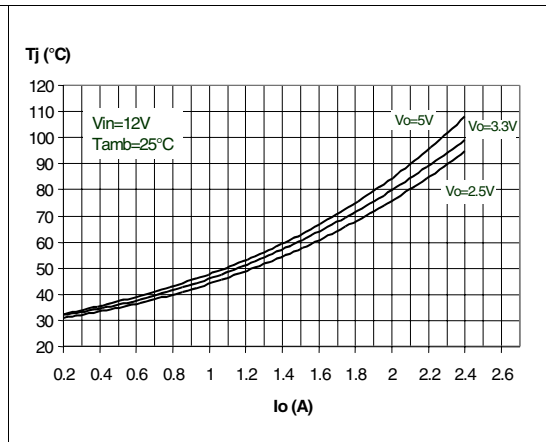
**Figure 6. Quiescent current vs. junction temperature**



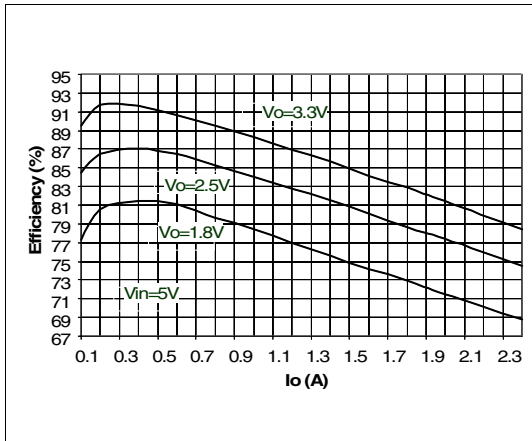
**Figure 7. Junction temperature vs. output current**



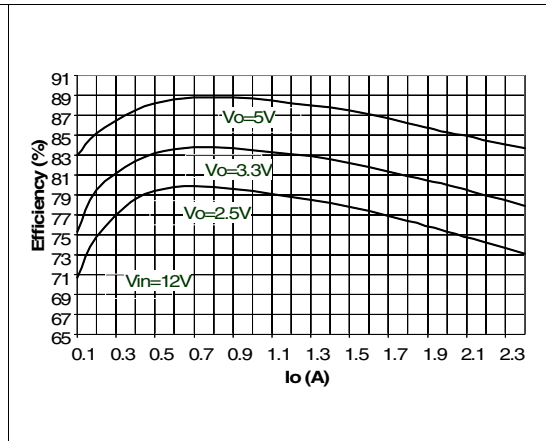
**Figure 8. Junction temperature vs. output current**



**Figure 9. Efficiency vs. output current**



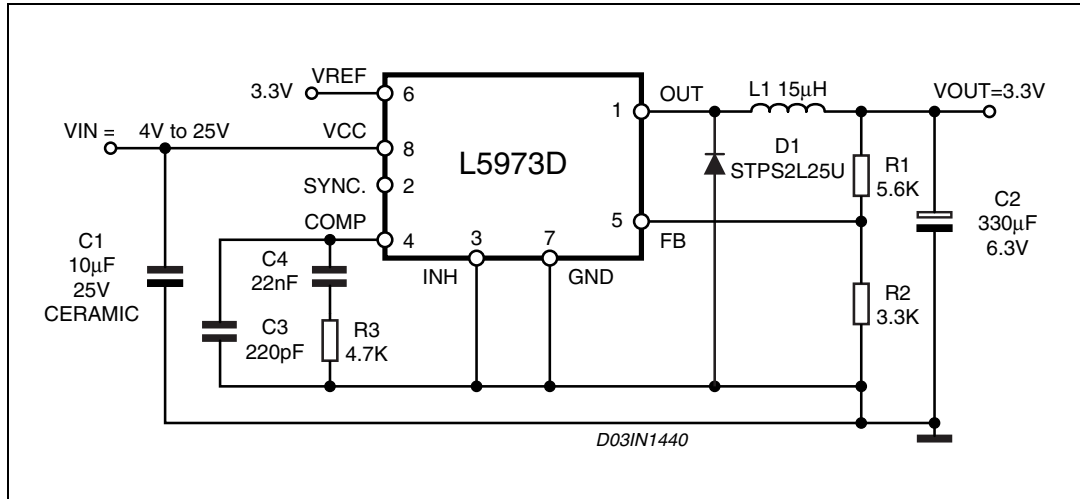
**Figure 10. Efficiency vs. output current**



## 5 Application circuit

In figure 6 is shown the demo board application circuit, where the input supply voltage,  $V_{CC}$ , can range from 4V to 25V due to the rated voltage of the input capacitor and the output voltage is adjustable from 1.235V to  $V_{CC}$ .

**Figure 11. Demo board application circuit**



**Table 5. Component list**

Reference	Part number	Description	Manufacturer
C1		10µF, 25V	TOKIN
C2	POSCAP 6TPB330M	330µF, 6.3V	Sanyo
C3	C1206C221J5GAC	220pF, 5%, 50V	KEMET
C4	C1206C223K5RAC	22nF, 10%, 50V	KEMET
R1		5.6K, 1%, 0.1W 0603	Neohm
R2		3.3K, 1%, 0.1W 0603	Neohm
R3		4.7K, 1%, 0.1W 0603	Neohm
D1	STPS2L25U	2A, 25V	ST
L1	DO3316P-153	15µH, 3A	COILCRAFT

Figure 12. PCB layout (component side)

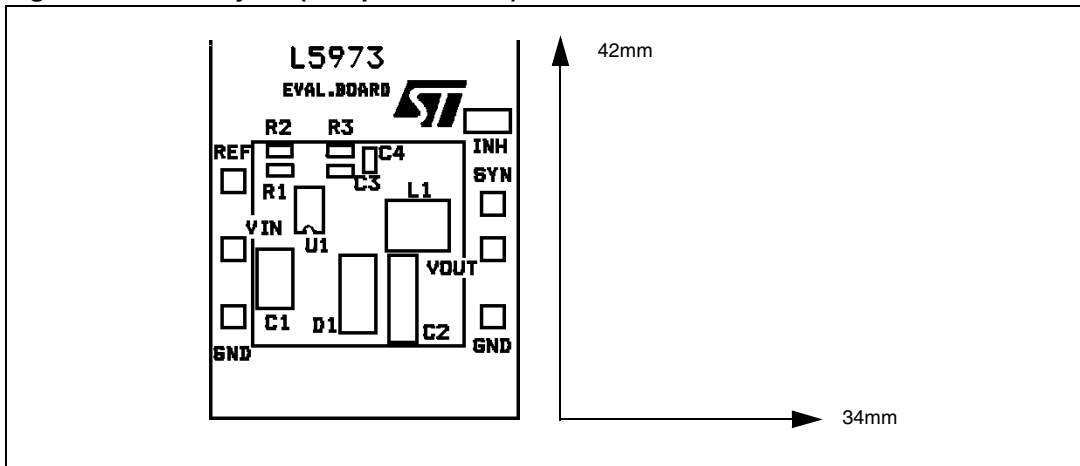


Figure 13. PCB layout (bottom side)

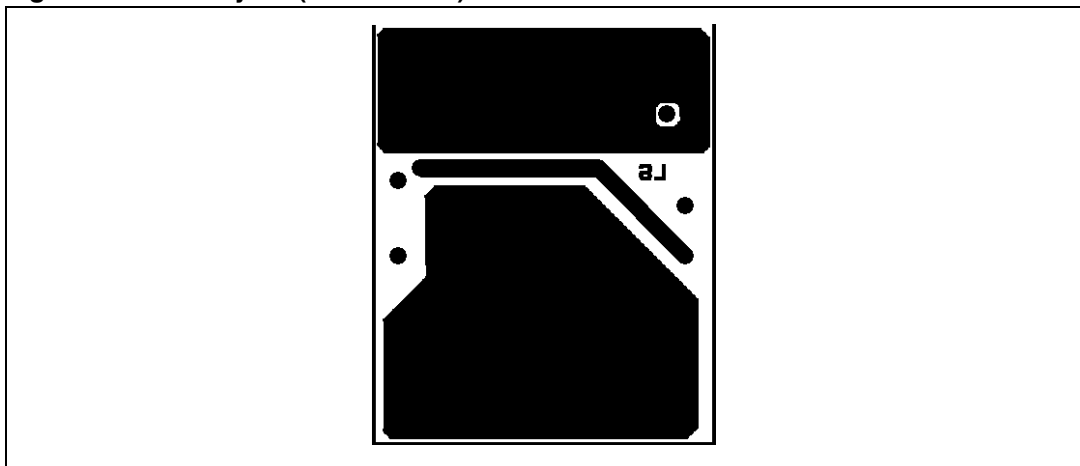
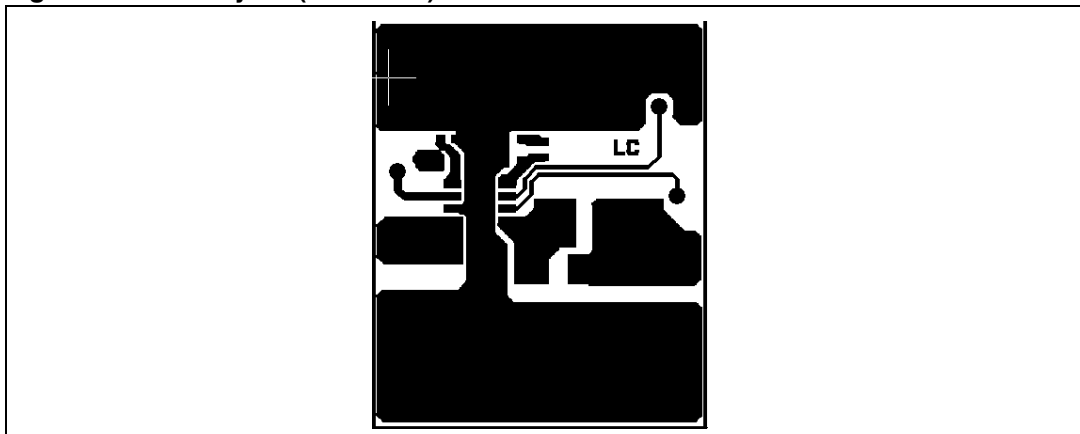


Figure 14. PCB layout (front side)



Below some graphs show the  $T_J$  versus output current in different conditions of the input and output voltage and some efficiency measurements.

## 6 Application ideas

Figure 15. Positive buck-boost regulator

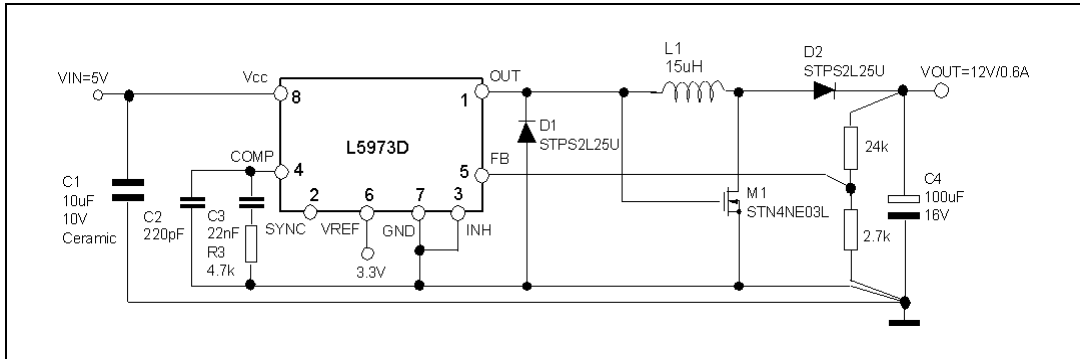


Figure 16. Buck-boost regulator

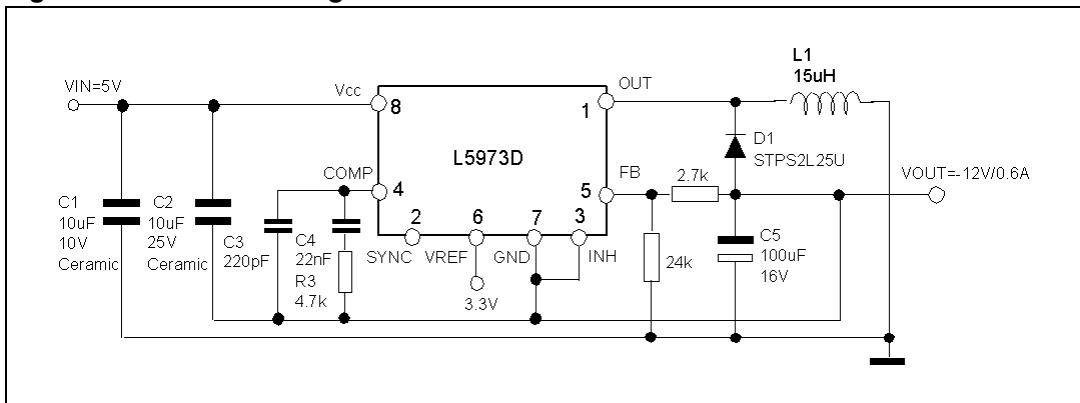
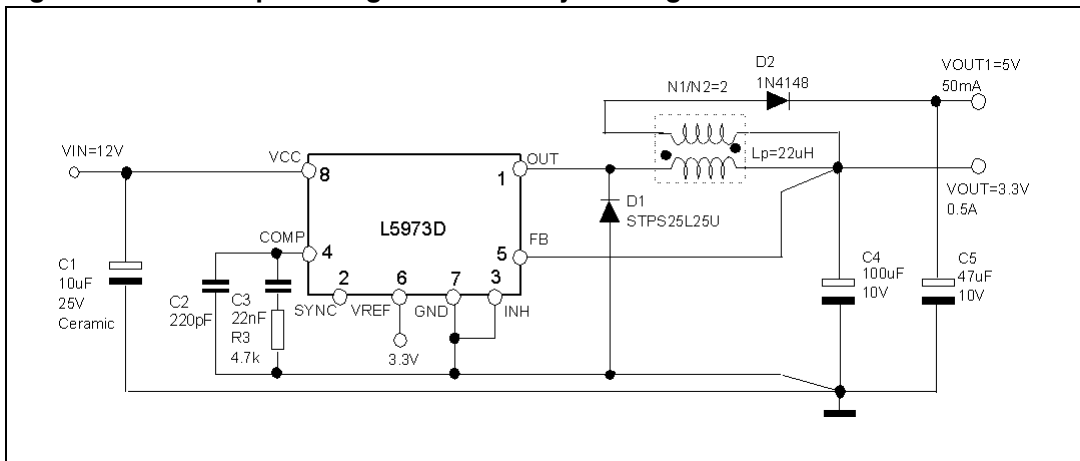


Figure 17. Dual output voltage with auxiliary winding



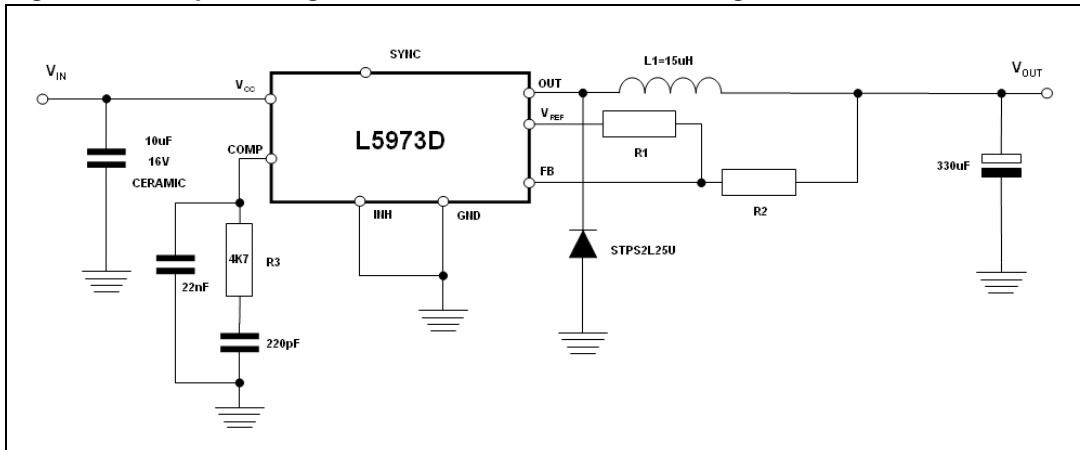
When an output voltage below the internal reference (1.235V) is required, the circuit reported in the figure 18 can be used. In this case the minimum voltage reachable is 0.6V and can be easily calculated with the following formula:

$$V_{OUT} = V_{FB} - [(V_{REF} - V_{FB}) \times (R_2 / R_1)]$$

If the load is not present, a resistor connected between  $V_{OUT}$  and GND is required in order to avoid that the voltage across  $C_{OUT}$  increases.

The value of this resistor has to be calculated taking into account that the current flowing through this resistance has to be higher than the current flowing through  $R_2$ .

**Figure 18. Output voltage below the 1.235V internal voltage reference**



## 7 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect . The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: [www.st.com](http://www.st.com)



## 8 Order code

**Table 7. Order code**

<b>Part number</b>	<b>Package</b>	<b>Packaging</b>
L5973DD	HSOP8 (Exposed Pad)	Tube
L5973DD013TR	HSOP8 (Exposed Pad)	Tape and reel

## 9 Revision history

**Table 8. Revision history**

Date	Revision	Changes
01-Nov-2005	10	Updated Package Information
22-May-2006	11	Electrical characteristic <a href="#">Table 4</a> updated, new application idea <a href="#">Figure 18</a> added, new template

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