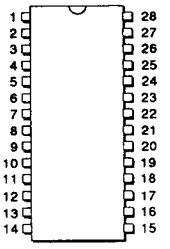
FEATURES

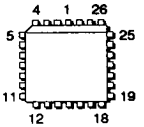
- ☐ Complete 2400 bps modem and 9600/7200/4800/2400 bps Sendfax
- ☐ Single 5V supply with 10 mW power down mode
- ☐ Pin compatible with Sierra SC11024 2400 bps modem
- ☐ Compatible with CCITT V.29, V.27ter, V.22 bis, V.22, V.21, and BELL 212A and 103 standards
- ☐ Integrated DTMF/Guard tone generator, call progress monitor
- ☐ 2100/2225 Hz tone detector
- ☐ Contains an on-chip hybrid
- ☐ Analog, digital, and remote digital loopback
- ☐ Compatible with SC11011, SC11021, SC11061, SC11074, SC11075 and SC11091 controllers
- ☐ Programmable audio output
- ☐ CMOS technology
- ☐ Synchronous & Asynchronous modes
- ☐ EIA 2188 Class 2 compatible firmware available

28-PIN DIP PACKAGE



SC11054CN

28-PIN PLCC PACKAGE



SC11054CV

GENERAL DESCRIPTION

The SC11054 is a complete 2400 bps, 5V only modem IC including a Sendfax capability up to 9600 bps. This IC contains all modem functions except the adaptive equalizer. It is used in conjunction with an external controller, such as the Sierra SC11011 (for either parallel bus or RS-232 applications) and memory to implement a 2400 bps full duplex modem, compatible with the CCITT V.22 bis recommendation, having Sendfax capability at 9600/7200 bps compatible with the V.29 recommendation or 4800/

BLOCK DIAGRAM

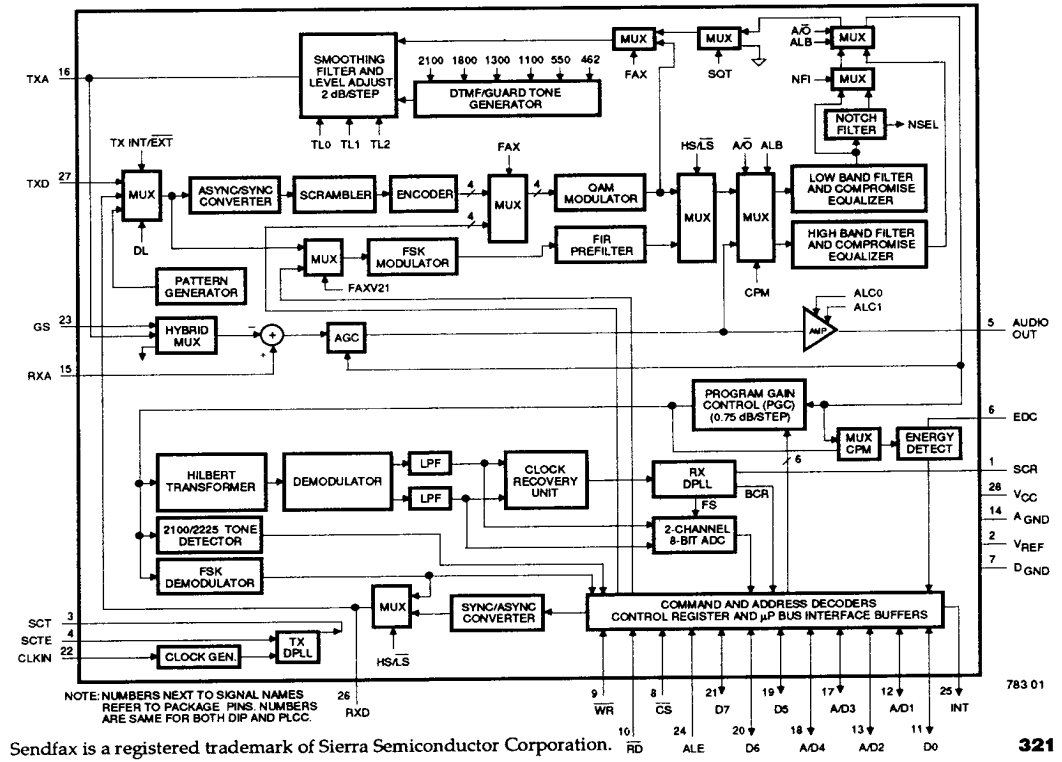


IMAGE UNAVAILABLE

FUNCTIONAL DESCRIPTION OF THE SC11054 MODEM

The SC11054 includes the following (See Block Diagram, Figure 1):

- ☐ Full transmitter consisting of
  - – Async to Sync converter
  - – Scrambler
  - – Data encoder
  - – 75% square root of raised cosine pulse shaper in V.22 mode, 50/90% square root of raised cosine shaping in V.27 4800/2400 bps modes and 20% square root of raised cosine shaping in V.29 9600/7200 bps modes
  - – Quadrature amplitude and phase modulators
  - – FSK (Bell 103 and CCITT V.21) modulator
  - – Hybrid
- ☐ High band and low band filters
- ☐ High band and low band compromise equalizers
- ☐ V.22 notch filter (selectable at 550 or 1800 Hz)
- ☐ Transmit smoothing filter
- ☐ Programmable attenuator for transmit level adjust
- ☐ DTMF, 462 Hz, 550 Hz, 1100 Hz, 1300 Hz, 1800 Hz, and 2100 Hz tone generator
- ☐ Tone detector for 2100/2225 Hz frequencies
- ☐ Transmit clock circuit for synchronous operation (slave, external, and internal modes)
- ☐ Pattern generator for generating fixed digital patterns in handshaking mode
- ☐ Receive section consisting of
  - – 64-step programmable gain controller (PGC)
  - – Energy detector at the output of the PGC
  - – Hilbert transformer
  - – Quadrature amplitude and phase demodulators (free running carrier) with low pass filters
  - – Baud timing recovery circuit (sampling clock of 600 Hz)
  - – FSK demodulator
  - – Sync to Async converter
- ☐ Two channel 8-bit analog to digital converter (ADC)
- ☐ Control and Status registers
- ☐ 8-bit microprocessor interface with interrupt and multiplexed address/data lines
- ☐ Audio output with level adjust

Transmitter (V.22bis, V.22, 212A and V.21 and 103)

Since data terminals and computers may not have the timing accuracy required for 2400/1200 bps transmission (0.01%), timing correction on the incoming data stream must be made. The async/sync converter accepts asynchronous serial data clocked at a rate between 2400/1200 Hz +2.3%, –2.5%. It outputs serial data at a fixed rate of 2400/1200 Hz ±0.01% derived from the master clock oscillator. To compensate for the input and output rate differences, a stop bit is either deleted or inserted when necessary. If the input data rate is slower than the output data rate, a stop bit is inserted. If the input data rate is faster than the output data rate, a stop bit is deleted. The output of the async/sync converter is applied to the scrambler.

The scrambler is a 17-bit shift register clocked at 2400/1200 Hz. Outputs from the 14th and 17th stages are exclusive OR'd and further exclusive OR'd with the input data. The resultant data is applied to the D input of the shift register. Outputs from the first four/two stages of the shift register form the quad/dibit that is applied to the QAM/QPSK modulator. The purpose of the scrambler is to randomize data so that the energy of the modulated carrier is spread over the band of interest—either the high band, centered at 2400 Hz, or the low band, centered at 1200 Hz.

In the 2400 bps mode, the modem actually sends four bits at a time, called a quadbit. The actual rate of transmission for a quadbit is 600 baud. This is the optimum rate of transmission over the general switched telephone network for a full duplex FDM (frequency division multiplexing) modem because band limit filters in the central office cut off at about 3000 Hz.

In the 2400 bps data rate, the data to be transmitted is divided into groups of four consecutive bits (quadbits). The first two bits of the quadbit are encoded as a phase quadrant change relative to the quadrant occupied by the preceding signal element. The last two bits define one of the four signaling elements associated with the new quadrant.

In the 1200 bps data rate, the data stream is divided into groups of two consecutive bits (dibits). The dibits are used to determine the phase quadrant change relative to the quadrant occupied by the preceding signal element. The resulting signaling elements from the inphase (I) and quadrature (Q) channels are passed through baseband filters with a square root of raised cosine shape. The filtered signals subsequently modulate sine and cosine carriers, and add to form the QAM/QPSK signal. The

monitor mode, the low-band filter is scaled down by a factor of 2.5 to center it over a frequency range of 300 to 660 Hz. Thus, during call establishment in the originate mode, call progress tones can be monitored through the scaled low-band filter and the modem answer tone or voice can be monitored through the unscaled high-band filter.

The low-band filter is a 10th order switched-capacitor band-pass filter with a center frequency of 1200 Hz. In the originate mode, this filter is used in the transmit direction; in the answer mode, it is used in the receive direction. When analog loopback is used in the originate mode, this filter, together with the low-band delay equalizer, is in the test loop.

The low-band delay equalizer is a 10th order switched-capacitor all-pass filter that compensates for the group delay variation of the low-band filter and half of the compromise line characteristics, producing a flat delay response within the pass-band.

The high-band filter is a 10th order switched-capacitor band-pass filter with a center frequency of 2400 Hz. In the answer mode, this filter is used in the transmit direction; in the originate mode, it is used in the receive direction. When analog loopback is used in the answer mode, this filter, together with the high-band delay delay equalizer, will be in the test loop.

The high-band delay equalizer is a 10th order switched-capacitor all-pass filter that compensates for the group delay variation of the high-band filter and half of the compromise line characteristics, producing a flat delay response within the pass-band. The transmit smoothing filter is a second-order low-pass switched-capacitor filter that adds the modem transmit signal to the V.22 guard tones. It also provides a 2 dB per step programmable gain function to set the output level.

Transmitter (V.29 and V.27ter)

In these modes the functions required to convert the transmit data to transmit analog signal are partitioned between the analog and controller chips. The firmware implemented in the controller chip performs the scrambling and also generates the training sequences as required by the V.29 and V.27ter specifications. Next, it carries out the encoding function based on the selected mode and bit rate (9600/7200/4800/2400 bps) and determines the new location of the constellation point. A 4-bit word (a_3 a_2 a_1 a_0) has been assigned to each constellation point to facilitate the quadrature modulation by the analog chip. (See figures 2a and b). Every two baud periods (2400/1600/1200 bauds), the analog chip sends an interrupt to the controller, within 250 µs, the controller has to write an 8-bit word into the FAXR register of the analog chip, that conveys the constellation point locations for two consecutive bauds (8-bit word corresponds to 8-bits of Tx data in 9600 bps mode, 6 bits in 7200 bps mode, 6 bits in 4800 bps mode and 4 bits in 2400 bps mode).

The analog chip will perform quadrature modulation on the 4 LSB's first and 4 MSB's on the next baud period. It also caries out square root of raised cosine shaping based on the selected baud rate. In fax mode (V.29, V.27ter) the modulated signal will directly feed the transmit smoothing filter, bypassing the band pass filter and equalizer.

Transmitter (V.21 FAX)

In FAX mode (BR3 =1 or BR2 =1) the operation of V.21 modem, referred to as V.21FAX, is half-duplex and uses the high channel.

The input/output data will be handled through the controller interface instead of the TXD/RXD pins.When transmitting in V.21 mode, the analog chip sends interrupts to the controller at a 300 Hz ±.01% rate which serves as a timing base. Within 2 ms after every eight interrupts, the controller has to

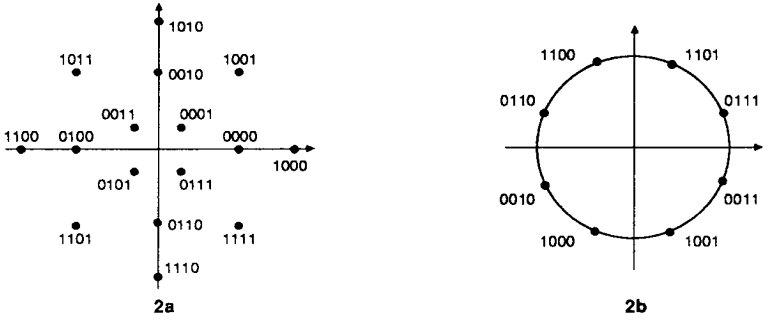


Figure 1. 4-Bit Words ($a_3a_2a_1a_0$) Identifying Constellation Points in V.29 (2a) and V.27ter (2b)

write an 8-bit word into the FAXR register that corresponds to eight consecutive transmit data bits with the LSB to be sent first.

The analog chip will perform a parallel-to serial conversion on the 8-bit word and feed the result into the FSK modulator block. The signal path from FSK modulator input to TXA pin will be similar to the normal V.21 mode.

Receiver (V.22 bis, V.22, 212A, V.21 and 103)

The receiver section consists of an energy detector, programmable gain control (PGC), part of the QAM/QPSK demodulator, FSK demodulator, 8-bit ADC and sync/async converter.

The received signal is routed through the appropriate band-pass filter and applied to the energy detector and PGC circuit. The energy detector provides detection within 17 to 24 msec. It is set to turn on when the signal exceeds –43 dBm and turn off when the signal falls below –48 dBm measured at the chip. A 2 dB minimum hysteresis is provided between the turn on and turn off levels. In call progress mode, the energy detector is connected to the output of the PGC to allow detection level adjustment.

The output of the receive filter is applied to the programmable gain control (PGC). This circuit has a wide overall range of 47.25 dB and provides 64 steps of 0.75 dB/step. The PGC gain is controlled by the external processor. It also provides auto-zeroing to minimize the output DC offset voltage.

The QAM/QPSK demodulator uses a coherent demodulation technique. Output of the programmable gain control (PGC) is applied to a Hilbert transformer that produces an in-phase and 90° out of phase component. These components are then demodulated to baseband in a mixer stage where individual components are multiplied by a free-running carrier. The baseband components are low-pass filtered to produce I and Q (Inphase and Quadrature) channel outputs. The I and Q channel outputs are both filtered by 300 Hz band-pass filters. Then they are rectified, summed and passed through a band-pass filter giving a 600 Hz signal. This signal is applied to a digital phase lock loop (DPLL) to produce a baud rate clock. Using the recovered clock signal, the I and Q channels are sampled and digitized into 8-bit samples by the ADC. Each channel (I and Q) is sampled twice during a baud period, once at the middle and once at the end of the baud period, allowing T/2 or T sampling operation. The external processor is interrupted once every baud period (1.667 msec). The processor should read the I and Q samples (within 100 µs from the time interrupt is issued), and perform adaptive equalization, carrier phase tracking, data decoding, and data descrambling. One quad/dibit is transferred from the SC11054 during each baud period.

In the asynchronous mode, data received from the processor is applied to the sync/async converter to reconstruct the originally transmitted asynchronous data. For data which had stop bits deleted at the transmitter (overspeed data), these stop bits are re-inserted. Underspeed data is passed essentially unchanged. The sync/async converter has two modes of operation. In the basic signaling mode, the buffer can accept an overspeed which corresponds to one missing stop bit in eight characters. The length of the start bit and data elements will be the same, and the stop bit will be reduced by 12.5%. In the extended-signaling range, the buffer can accept one missing stop bit in four characters and the stop bits will be reduced by 25% to allow for overspeed in the transmitting terminal. Output of the sync/async converter, along with the output of the FSK demodulator, is applied to a multiplexer. The multiplexer selects the appropriate output, depending on the operating speed and output data received on the RXD pin.

For low-speed operation, the FSK demodulator is used. The output of the PGC amplifier is passed through a zero crossing detector and applied to a counter that is reset on zero crossings. The counter is designed to cycle at a rate 4 times faster than the carrier signal. The counter output is low-pass filtered and hard limited to generate FSK data.

To improve the performance of the receiver at low signal levels, while maintaining a wide amplitude range, a 1-bit AGC circuit is placed prior to the band-pass filter. The decision thresholds of this AGC are controlled by the AGCVT bit. When AGCVT = 1, the thresholds will be 6 dB further apart than when AGCVT = 0, so that the probability of gain change will be reduced. The status of the AGC gain is available through the AGCO bit. AGC will have 8 dB more gain when AGCO = 1. Status of AGCO should be monitored at every baud timing period and when it makes a transition (causing a gain-hit) the PGC's gain shouldbe modified accordingly to prevent divergence of the adaptive equalizer.

Receiver (V.21 FAX)

When receiving in V.21FAX mode, which is half-duplex, the serial output data from FSK demodulator will be loaded into a serial-to-parallel register. The timing for serial shift as well as interrupt is derived from the received data through a resettable counter. The counter divides an input clock of 9.6 kHz by 32 to generate a 300 Hz signal. On every high to low transition of data the counter is reset and resynchronized to data timing. Assuming a received bit rate of 300 BPS ±0.01%, the interrupt should have an aver-

age frequency of 300 Hz ±.01%. The controller should count the interrupt pulses and read the contents of FAXV21R register within 1.5 ms after every eighth pulse. The LSB corresponds to FSK demodulator output that has been received first in time.

A flag detector is implemented on the chip to facilitate detection of flag sequences (Hex 7E) in V.21 FAX mode. The decoder, detects the flag itself or possible rotations of it; i.e. it detects 01111110, 00111111, 1001111, 11001111, 11100111, 11110011, 11111100. If any of these combinations is detected, then FLAGDET bit of the status register will go high and stay high until the condition goes away. The flag detector output is updated on every interrupt pulse in the V.21FAX receive mode. To ensure that the flag detector is not triggered by false data, it is recommended that the FLAGDET bit be checked for at least 16 consectutive interrupts after this bit gets set. If it does not stay high continuously the received data may not be a true flag sequence. Flag detector should be used in V.21FAX receive mode only.

Tone Detector

A digital tone detector has been implemented in the SC11054 to facilitate detection of 2100/2225 Hz tones. The output of the PGC is passed through a zero crossing detector which in turn feeds a digital timer that verifies the period of the tone. If four consecutive periods of input tone pass the requirements, then, the appropriate tone detector output (TD2100 or TD2225 bit in status register) goes high. To detect these tones user must insert the highband filter in the receive path to allow their passage, also, PGC gain must be set properly to amplify the input to the tone detector. It will be a good practice to monitor ED bit when reading TD to ensure that the signal energy is within acceptable limits.

With the PGC gain word (PGCR) set to 011111 the tone detector threshold will be typically -43dBm.

Hybrid

The signal on the phone line is the sum of the transmit and receive signals. The hybrid subtracts the transmitted signal from the signal on the line to form the received signal. It is important to match the hybrid impedance as closely as possible to the telephone line to produce only the received signal. When the internal hybrid is used, by turning the "Hybrid" code on through the interface, this matching is provided by an external resistor connected between the TXA and RXA pins on the SC11054. The filter section provides sufficient attenuation of the out-of-band signals to eliminate leftover transmit signals from the received signal. The hybrid also acts as a first order low-pass antialiasing filter. The hybrid can be deactivated by the controller.

The SC11054 internal hybrid is intended to simplify the phone line interface. The internal hybrid can compensate for the loss in the line coupling transformer used in the DAA. By tying the GS pin to AGND, V_{REF} or V_{CC}, compensation levels of 0, +2, +3 dB, respectively are provided.

With a higher loss transformer, some degradation in performance at lower signal levels will occur. Specifically, the bit error rate, when operating at receive signal levels below –40 dBm in the presence of noise, will be higher. The energy detect on/off levels measured at the line will also be different from those specified at the chip. An external hybrid circuit, shown in Figure 2, can be used to overcome these losses and achieve maximum performance. In this case, the internal hybrid must be turned off by setting bit 6 of the TXCR register to 0.

The external hybrid circuit uses two operational amplifiers, one in the transmit path and the other in the receive path. The SC11054 internal transmit stage provides a gain of 6 dB over the transmit signal level desired at the line. Under ideal conditions, with no loss in the transformer and perfect line matching, the signal level at the line will then be the desired value. In practice, however, there is impedance mismatch and a loss in the coupling transformer. Therefore, it may be desired to provide a gain in the transmit and receive paths to overcome the loss. The receive gain (G_R) and transmit gain (G_T) are set by the ratios of resistors R2, R1 and R6, R5, respectively (Figure 2).

The circuit can be analyzed as follows:

$$V_R = -\frac{R2}{R1}\left(V_{TR}\right) + \left(1+\frac{R2}{R1}\right)\left(\frac{R4}{R3+R4}\right)V_y$$

$$V_y = -\frac{R6}{R5}V_x$$

If R6/R5 is chosen to equal the loss in the transformer, it can be assumed that V_y is twice as high as V_{TX} (transmit portion of the total line signal). Since $V_{TR} = V_{TX} + V_{RX}$ and $V_y = 2V_{TX}$,

$$V_R = -\frac{R2}{R1}\left(V_{TX}+V_{RX}\right) + \left(1+\frac{R2}{R1}\right)\left(\frac{R4}{R3+R4}\right)2V_{TX}$$

$$= -\frac{R2}{R1}V_{RX} + \left[\left(1+\frac{R2}{R1}\right)\left(\frac{2R4}{R3+R4}\right) - \frac{R2}{R1}\right]V_{TX}$$

To eliminate any transmit signal from appearing at the received signal input, the second term in the above equation must be set to zero, giving:

$$\left(1+\frac{R2}{R1}\right)\left(\frac{2R4}{R3+R4}\right) = \frac{R2}{R1}$$

Solving for R3/R4:

$$\frac{R3}{R4} = 1 + \frac{2R1}{R2}$$

Additionally,

$$G_R = \frac{R2}{R1} \text{ and } G_T = \frac{R6}{R5}$$

These equations can be solved to select component values that meet the desired requirements. For example, if the transmit and receive

loss in the coupling transformer is 2.5 dB, then:

$$\frac{R2}{R1} = \text{INV Log}\left(\frac{G_{RdB}}{20}\right) = \text{INV Log}\left(\frac{2.5}{20}\right) = 1.333$$

Similarly, $\frac{R6}{R5} = 1.333$ and $\frac{R3}{R4} = 2.5$

Some typical values are:

R1=20KΩ, R2=27KΩ, R3=13KΩ, R4= 5.1KΩ, R5=20KΩ, and R6=27KΩ

It should be noted that the transmit amplifier is only needed to overcome the loss in line coupling. It can be eliminated since the transmit signal level specification is typically stated as a maximum. Amplifier B, resistors R5 and R6, and capacitor C1 can be eliminated, and point X can be connected to point Y in the circuit of Figure 2 to achieve a more cost effective external hybrid arrangement.

The SC11054 with the internal hybrid may also be used on a 4-wire system where the transmit and receive signals are kept separate. In this mode, the "Hybrid" code must be turned off. The transmit signal is connected to a 600 Ω line transformer through a 600 Ω resistor.

Tone Generator

The tone generator section consists of a DTMF generator, V.22 guard-tone, and 1300 and 2100 Hz tone generators. The DTMF generator produces all of the tones corresponding to digits 0 through 9 and A, B, C, D, *, and # keys. The V.22 guard-tone generator produces either 550 Hz or 1800 Hz. Selection of either the 550 Hz or 1800 Hz tone will cascade the corresponding notch filter with the low-band filter. The tones are selected by applying appropriate codes through the tone control register. Before a tone can be generated, tone mode must be selected. Facility is also provided to generate single tones corresponding to 1300, 1100, 464 and 2100 Hz and the individual rows or columns of the DTMF signal.

Audio Output Stage

A programmable attenuator that can drive a load impedance of 50K Ohms is provided to allow monitoring of the received line signal through an external speaker. The attenuator is connected to the output of the hybrid. Four levels of attenuation—no attenuation, 6 dB attenuation, 12 dB attenuation, and squelch are provided through the ALC1 and ALC0 audio output level control codes. Output of the attenuator is available on the audio output pin where an external audio amplifier (LM386 type) can be connected to drive a low impedance speaker. The output can directly drive a high impedance transducer, but the volume level will be low.

Clock Input

CLKIN (Pin 22) of the SC11054 should be connected to a 9.8304 MHz clock source with an accuracy of ±0.01%.

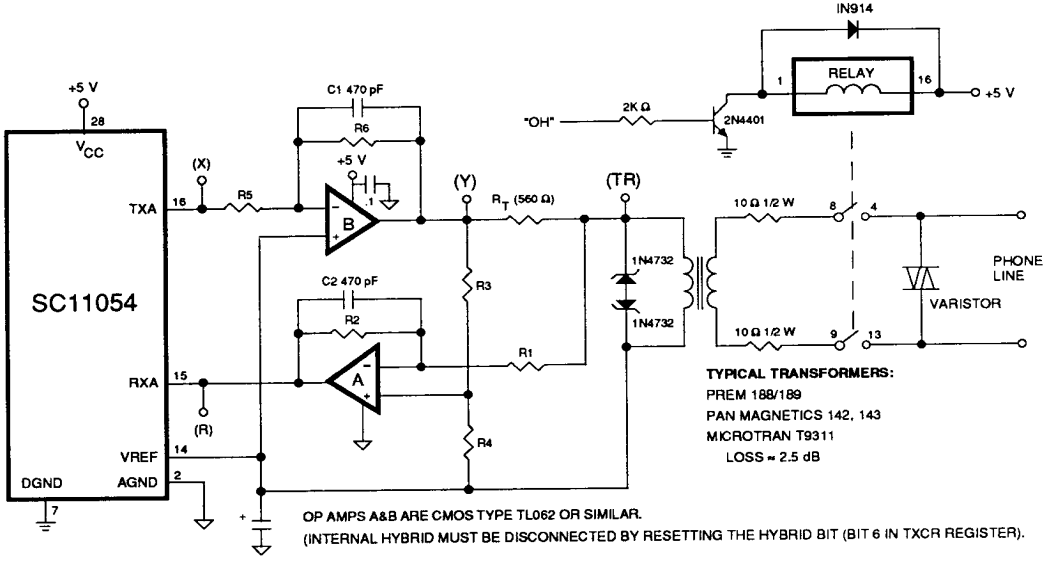


Figure 2. Using an External Hybrid with the SC11054

FUNCTIONAL DESCRIPTION OF THE SC11011 CONTROLLER

The SC11011 modem controller, implemented in Sierra's CMOS process, was designed specifically to handle all of the modem control functions, as well as the interface to a system bus or an RS-232 serial interface. Besides including a 16-bit microprocessor, 8k by 8 bytes of ROM and 128 by 8 bytes of RAM, it also contains the functionality of a 82C50B UART, greatly simplifying the interface to a parallel system bus, such as the one used in IBM's PC. In fact, a complete, Hayes compatible modem with Sendfax capability for the PC consists of the SC11011 controller with external memory, the SC11054 modem and the DAA. All of the popular communications software written for the PC will work with the SC11054/SC11011 set.

The SC11011 can be configured for RS-232 applications. The difference is that the UART is wired so that the serial data from the RS-232 port is converted to parallel data handled by the internal processor. Pins are provided for connecting the familiar switches and indicator lamps found on most stand-alone modems, although the switches and lamps are not needed for operation—all of the switch settings can be done through software.

The controller receives an 8-bit signal sample from the SC11054 and performs adaptive equalization, carrier phase recovery, data decode, and descrambling. The controller is configured for parallel or serial applications by the firmware. The controller is designed by using a 16-bit 2900 processor to perform the digital signal processing and the control functions. Its instruction set is a subset of the Intel 8096 instruction set, but operates faster than the 8096.

The SC11011 provides a standard 5V logic level interface—RS-232 drivers are required to interface to the port. Firmware for external memory is available for the SC11054. It includes the Hayes "AT" command set, and T.30 protocol. When used with the SC11011 controller, it emulates a Hayes-type stand-alone or internal modem with Sendfax.

The SC11011 is available in a 68 pin PLCC. The 68 pin package allows the controller to access external ROM of up to 32K bytes and external RAM of up to 16K bytes. This allows users to customize their own software, and provides a means for software development. The serial controller can talk to both an SC11054 and an SC22201 (EERAM).

The SC11011 requires a single +5 V power supply. Besides the interface for the SC11054 modem, when the SC11011 controller is used for internal applications, it has an eight-bit data port, three address lines, a chip select input, an interrupt line, and the DOST and DIST control lines found in the 82C50B UART. It also has control lines for ring indication, the off-hook relay, and a data/voice relay; these lines connect to the DAA.

When used in RS-232 applications the SC11011's, eight-bit port becomes the switch input lines, and the address, chip select, INTO, DIST and DOST lines become the lines for the RS-232 interface, and modem status. These lines are also used to drive the LEDs. Internally, all of these lines are treated as programmable I/O ports under software control.

The interface to the SC11054 is via an 8-bit address/data bus and the control lines for read and write. The same interface is used for access to an electrical erasable random access memory (SC22201). There are six clock multiplexed address/data bus cycles. A ready signal is provided for the interface to a high speed PC-AT type bus cycle. The 68 pin package, has 15 extra address lines and chip selects for external ROM and external RAM interfaces.

The SC11011 is truly an ASIC DSP & controller—it is designed to control a modem or other peripheral that operates at a moderately slow data rate up to 2400 bits per second. What's unique about the SC11011, for example, is that it allows a slow peripheral to interface to a high speed bus without making the main processor add unnecessary wait states.

This is done through the UART interface and the on-chip registers which look somewhat like dual port registers. The main processor can write to and read from them at will, while the on-chip controller can do the same. The controller was designed this way because most communications software has to have unrestrained access to the UART registers. To make the SC11011 compatible with this software, the registers were included.

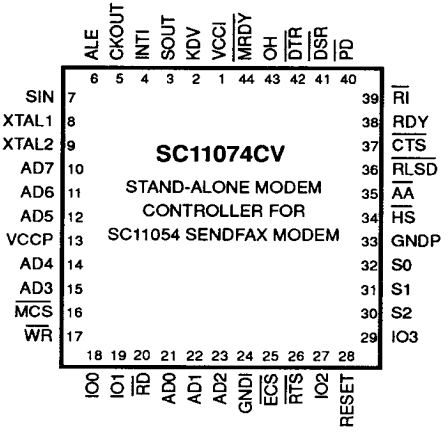
The internal processor monitors the registers to determine the mode of operation—command mode or data mode; at power-up, it is automatically put in the command mode and it looks for instructions. Once carrier is detected, it goes into the data mode, and stays there until an escape sequence is entered, just like a Hayes-type modem. The escape sequence is three + signs—+++ —in the default mode, but it can be changed in the software.

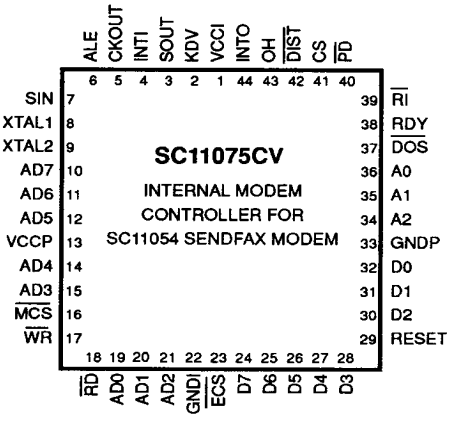
The actual processor contains a 16-bit data path and can execute 54 instructions with three different addressing modes: direct, indirect, and immediate. There is 8K by 8 of ROM on the chip for program storage.

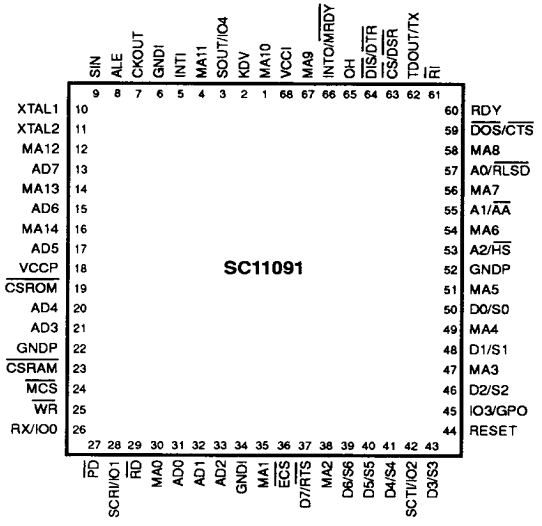
To the system bus, the SC11011 looks and acts like an 8250B UART. Communications software written for this UART will work with the SC11011.

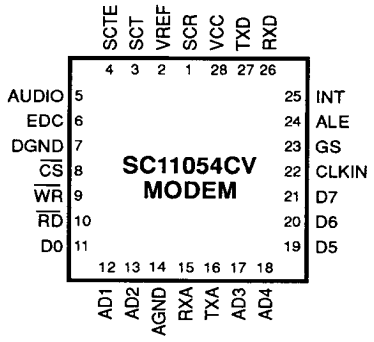
IMAGE UNAVAILABLE

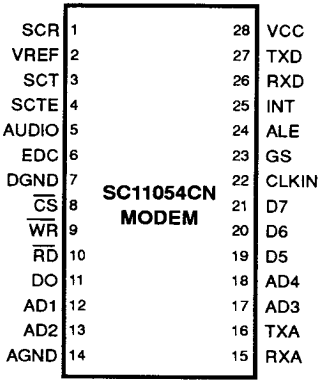
CONNECTION DIAGRAM FOR CONTROLLERS & MODEMS (continued)











PIN DESCRIPTIONS

PIN NO.	PIN NAME	DESCRIPTION
1	SCR	Synchronous Clock Receive (Data set source); Output; TTL; Used only in bit synchronous mode; Recovered by the Receiver Phase Locked Loop from the far end modem. Data on RXD is valid at the rising edge of this clock.
2	V_{REF}	Reference Ground; Generated inside the chip and is equal to $V_{CC}/2$.
3	SCT	Synchronous Clock Transmit (Data set source); Output; TTL; Used only in bit synchronous mode; Generated internally by the SC11024 Clock Generator; Rate = 1200 Hz ±0.01% or 2400 Hz ±0.01%.
4	SCTE	Synchronous Clock Transmit External (DTE source); Input; TTL; Used only in bit synchronous mode; Data on TXD line is latched by the SC11024 at the rising edge of this clock. Clock rate = 1200 Hz ±0.01% or 2400 Hz ±0.01%.
5	AUDIO	Audio output; The hybrid output is passed through a programmable attenuator and fed to this analog pin. Four different levels can be attained by controlling bit 0 and bit 1 of the AUDIO register as specified under AUDIO register description.
6	EDC	Capacitor for energy detect; A 1.0 µF capacitor should be connected between this pin and AGND.
7	DGND	Digital ground
8	$\overline{CS}$	Chip Select; Input; TTL; Active low.
9	$\overline{WR}$	Write; Input; TTL; Normally high; Data on AD7–AD0 is written into the SC11024 registers at the rising edge of this pulse.
10	$\overline{RD}$	Read; Input; TTL; Normally high; Data on AD7–AD0 is to be read by the processor at the rising edge of this pulse.
12,13,17,18	AD1–AD4	Multiplexed address/data bus (8-bits); Input/Output; TTL; A/D4–A/D1 (4-bits) are used for multiplexed addressing of internal registers.
14	AGND	Analog Ground
15	RXA	Receive analog; Input
16	TXA	Transmit analog; Output
11,19–21	D0, D5–D7	Bits 0, 5, 6 and 7 are don't cares as far as address is concerned.
22	CLKIN	Clock input; 9.8304 MHz clock input from the controller.
23	GS	Gain Select to compensate for loss in line coupling transformer. When left open or tied to AGND, the compensation is 0 dB; connected to VREF, +2 dB compensation is provided; And when tied to V_{CC}, the compensation is +3 dB.
24	ALE	Address Latch Enable; Input; TTL; The address on A/D4–A/D1 is latched into the SC11054 Address decoder at the falling edge of this normally low pulse.
25	INT	Interrupt; Output; TTL; Normally low; A short (13 µs typical) positive pulse is generated after all A to D conversions are completed.
26	RXD	Received Data; Output; TTL
27	TXD	Transmit Data; Input; TTL
28	V_{CC}	+5 V supply

REGISTERS

There are fourteen 8-bit registers interfacing to the microprocessor bus. Six of these registers can only be read by the processor (called READ registers) and the remaining eight can be written into by the processor (called CONTROL registers). Bit 1 of the "Tone" register can be read and written by the processor, Table 1 shows the address and bit assignments for these registers.

A chip select pin is provided for multi-peripheral addressing by the processor.

Table 1. READ Registers

ADDRESS BITS				NAME	MSB			BIT NUMBER				LSB
A4	A3	A2	A1		7	6	5	4	3	2	1	0
0	0	0	0	Q1	Q17	Q16	Q15	Q14	Q13	Q12	Q11	Q10
0	0	0	1	I1	I17	I16	I15	I14	I13	I12	I11	I10
0	0	1	0	Q2	Q27	Q26	Q25	Q24	Q23	Q22	Q21	Q20
0	0	1	1	I2	I27	I26	I25	I24	I23	I22	I21	I20
0	1	0	0	Status	X	X	FLAGDET	AGCO	TD2100	TD2225	FSKD	ED
0	1	0	1	FAXV21R	R7	R6	R5	R4	R3	R2	R1	R0
0	1	X	1	Unused		Unused						
0	1	1	X	Unused		Unused						

STATUS Register: Address (A4–A1) = 0100

BIT NUMBER	BIT NAME	DESCRIPTION
Bits 7–6	Unused	
Bits 5	FLAGDET	Flag Sequence detector output. When set, flag sequence is present in V.21FAX mode.
Bit 4	AGCO	Status of internal 1-bit AGC. When this bit is set, RXA signal is amplified by 8 dB before entering the bandpass filters.
Bit 3	TD2100	2100 Hz tone detector output. TD2100=1 when this tone is present.
Bit 2	TD2225	2225 Hz tone detector output. TD2225=1 when this tone is present.
Bit 1	FSKD	Received FSK data. FSKD = 1 when mark is received.
Bit 0	ED	Energy detect circuit output. ED = 1 when energy detected.

Note: When reading unused bits, the corresponding bus lines will not be driven by the SC11054 and will be floating.

FAXV21R Register: Address (A4–A1) = 0101

BIT NUMBER	BIT NAME	DESCRIPTION
Bits 7–0	R7–R0	In V.21 FAX receive mode this register will be loaded by received data and should be read every eighth interrupt pulse. LSB (R0) corresponds to the data bit received first in time.

Table 1a. READ Registers

Q1 Register:	Stores midbaud inphase sample output of ADC.
I1 Register:	Stores midbaud quadrature sample output of ADC.
Q2 Register:	Stores endbaud inphase sample output of ADC.
I2 Register:	Stores endbaud quadrature sample output of ADC.

Note: All samples are represented in two's complement form.

Table 2. CONTROL Registers

ADDRESS BITS				NAME	BIT NUMBER							
A4	A3	A2	A1		7	6	5	4	3	2	1	0
1	0	0	0	TXCR	BR2	HYBRID	TXSEL2	TXSEL1	TXSEL0	SQT	BR1	BR0
1	0	0	1	MCRA	SLAVE	LCK/$\overline{\text{INT}}$	RNGX	SYNC	WLS1	WLS0	A/$\overline{\text{O}}$	RXMRK
1	0	1	0	MCRB	BR3	PD	TONDETE	CPM	ALB	TL2	TL1	TL0
1	0	1	1	TONE	X	HNDSHK	TONEON	DTMF	D3	D2	D1	D0
1	1	0	0	PGCR	X	AGCVT	G5	G4	G3	G2	G1	G0
1	1	0	1	DATA	X	PLLJAM	PLLFRZ	PLLFAST	RD3	RD2	RD1	RD0
1	1	1	0	AUDIO	X	DISS	PGCZ	TST2	TST1	TST0	ALC1	ALC0
1	1	1	1	FAXR	B7	B6	B5	B4	B3	B2	B1	B0

Transmit Control Register (TXCR): Address (A4–A1) = 1000
(Note: When writing into these registers, the bus lines corresponding to the unused bits are ignored by the SC11054.)

BIT NUMBER	BIT NAME	DESCRIPTION
Bit 7	BR2	This bit in conjunction with BR3, BR1 and BR0 selects bit rate.
Bit 6	HYBRID	When set, the transmitter output (TXA) is connected to the inverting input of the receive buffer to allow the use of the on-chip hybrid circuit for 2 to 4 wire conversion.
Bit 5 Bit 4 Bit 3	TXSEL2 and TXSEL1 and TXSEL0	Transmit Select bits. These 3 bits determine the data transmitted by the transmitter according to the following table:

TXSEL2	TXSEL1	TXSEL0	TRANSMITTED DATA
0	0	0	External data sent by DTE.
0	0	1	Unscrambled S1 (Note 1).
0	1	0	Unscrambled Space.
0	1	1	Unscrambled Mark.
1	0	0	Scrambled RX. Digital loop back mode (Note 2).
1	0	1	Scrambled Reversals (Notes 3 and 4).
1	1	0	Scrambled Space (Note 4).
1	1	1	Scrambled Mark (Note 4).

Note 1: S1 is a pattern of 0011 transmitted at 1200 bps rate regardless of BR1. If in FSK mode (BR0 = 1), then reversals are sent. This pattern cannot be sent at 2400 bps rate.
Note 2: In this mode, the received data, after being descrambled, is sent back to the scrambler. The modem will automatically go to the Synchronous mode. Slave bit has to be set.
Note 3: Reversals are continuous streams of 01.
Note 4: When in FSK mode (BR0 = 1), TXSEL2 is ignored since scrambling is not applicable.

Bit 2	SQT	When this bit is set, the transmitter is squelched by connecting the output of MUX1 (see the block diagram) to analog ground.
Bit 1 Bit 0	BR1 and BR0	Bit Rate Selection bits based on the following table:

BR3	BR2	BR1	BR0	BIT RATE
0	0	0	0	2400 bps V.22 bis
0	0	1	0	1200 bps V.22/212A
0	0	0	1	0–300 bps Bell 103
0	0	1	1	0–300 bps CCITT V.21
0	1	0	0	4800 bps V.27
0	1	1	0	2400 bps V.27
X	1	0	1	N.A.
1	X	0	1	N.A.
X	1	1	1	0–300 bps V.21 FAX
1	X	1	1	0–300 bps V.21 FAX
1	0	0	0	9600 bps V.29
1	0	1	0	7200 bps V.29
1	1	X	0	N.A.

CONTROL REGISTERS (Cont.)

Mode Control Register A (MCRA): Address (A4–A1) = 1001

BIT NUMBER	BIT NAME	DESCRIPTION
Bit 7	SLAVE	When set, receiver timing will be used as clock source for transmitter. LCK/INTB and SYNC bits must be high for slave mode
Bit 6	LCK/INTB	Determines the clock source for the transmitter. When this bit is set, the clock source is externally provided on SCTE (pin 4), and when cleared, it is internally generated (SCT). This bit can select the clock source independent of Sync/Async mode selection (see below). When in Digital Loop-Back mode, the clock source will be forced to the Slave mode (SCR).
Bit 5	RNGX	Range extender for the receiver Sync/Async converter. When set, the receiver Sync/Async can insert up to one stop bit per four (8, 9, 10 or 11-bit) characters to compensate for a far end DTE being up to 2.3% over speed. The transmitter Async/Sync always handles this overspeed condition regardless of this bit's condition.
Bit 4	SYNC	When set, operate in bit synchronous mode; when clear, operate in character asynchronous mode. When in Digital Loop-Back mode, the SC11046 will be forced to the Synchronous mode.
Bit 3 and Bit 2	WLS1 and WLS0	Word length select bits in asynchronous mode, according to the following table:

WLS1	WLS0	NUMBER OF BITS PER CHARACTER
1	0	8
1	1	9
0	0	10
0	1	11

Bit 1	A/$\overline{O}$	When set, operate in answer mode; when clear, operate in originate mode.
Bit 0	RXMARK	When set, the RXD pin is clamped to the high logical level.

Mode Control Register B (MCRB): Address (A4–A1) = 1010

BIT NUMBER	BIT NAME	DESCRIPTION
Bit 7	BR3	This bit in conjunction with BR2–BR0 selects the bit rate.
Bit 6	PD	When this bit is set, chip will be powered down. When cleared normal operation is restored.
Bit 5	TONDETE	When this bit is set, 2100/2225 Hz tone detector will be enabled. However, for proper functioning, highband filter must be set in the receive path to pass these tones. Tone amplification before detection can be set by PGC.
Bit 4	CPM	Call progress monitor mode. When set, the receive path can be connected to the high band filter to detect answer tone (ALB=0) or to the low band filter scaled down 2.5 times (ALB=1) to listen for the call progress tones during auto dialing.
Bit 3	ALB	Analog Loop Back. When set, the transmitter output (TXA) is connected to the receive path, bypassing the receive filter.
Bit 2 and Bit 1 and Bit 0	TL2 and TL1 and TL0	Transmit level adjust bits based. In FAX modes maximum transmit level will be 2 dB lower than modem mode (BR3=BR2=0).

			TRANSMIT LEVEL AT TXA PIN	
TL2	TL1	TL0	MODEM MODE BR3=BR2=0	FAX MODE BR3=1 or BR2=1
0	0	0	-3 dBm	-5 dBm
0	0	1	-5 dBm	-5 dBm
0	1	0	-7 dBm	-7 dBm
0	1	1	-9 dBm	-9 dBm
1	0	0	-11 dBm	-11 dBm
1	0	1	-13 dBm	-13 dBm
1	1	0	-15 dBm	-15 dBm
1	1	1	-17 dBm	-17 dBm

CONTROL REGISTERS (Cont.)

TONE Register: Address (A4–A1) = 1011

BIT NUMBER	BIT NAME	DESCRIPTION
Bit 7	Unused	
Bit 6	HNDSHK	This bit is set only during handshaking sequence. When set, both FSK and PSK/QAM demodulators are enabled. When cleared, FSK demodulator is disabled when in high speed mode.
Bit 5	TONEON	When set, the output of the tone generator appears at TXA. When cleared, the output of the tone generator is squelched.
Bit 4	DTMF*	When set, the DTMF generator is turned on. When cleared, the DTMF generator is turned off, but other tones can be generated.
Bits 3–0	D3–D0	Specify the desired tone (see the following table):

DTMF	D3	D2	D1	D0	DIGIT DIALED	TONE OUTPUT	FREQUENCIES (HZ)
1	0	0	0	0	0	941	1336
1	0	0	0	1	1	697	1209
1	0	0	1	0	2	697	1336
1	0	0	1	1	3	697	1477
1	0	1	0	0	4	770	1209
1	0	1	0	1	5	770	1336
1	0	1	1	0	6	770	1477
1	0	1	1	1	7	852	1209
1	1	0	0	0	8	852	1336
1	1	0	0	1	9	852	1477
1	1	0	1	0	*	941	1209
1	1	0	1	1	(A)	697	1633
1	1	1	0	0	(B)	770	1633
1	1	1	0	1	(C)	852	1633
1	1	1	1	0	#	941	1477
1	1	1	1	1	(D)	941	1633
0	0	0	0	0	No tone; tone generator turned off		
0	0	0	0	1	550		
0	0	0	1	0	1800		
0	0	0	1	1	2100		
0	0	1	0	0	1300		
0	0	1	0	1	1100		
0	0	1	1	x	462		
0	1	x	x	x	No tone; tone generator turned off		

Note: TONEON must also be set to generate DTMF signals.

Programmable Gain Controller Register (PGCR): Address (A4–A1) = 1100

BIT NUMBER	BIT NAME	DESCRIPTION
Bit 7	Unused	
Bit 6	AGCVT	When set, prevents gain hit due to AGC's gain step. This bit must be set during the handshaking after detecting the four point constellation and before switching to 16-way decision making.
Bits 5–0	G5–G0	Control the gain of the PGC within a range from –10 to +37.5 dB in 0.75 dB steps. (See the following table):

CONTROL REGISTERS (Cont.)

G5	G4	G3	G2	G1	G0	PGC GAIN (dB)
0	0	0	0	0	0	–10.0
0	0	0	0	0	1	–9.25
0	0	0	0	1	0	–8.5
0	0	0	1	0	0	–7.0
0	0	1	0	0	0	–4.0
0	1	0	0	0	0	+2.0
1	0	0	0	0	0	+14.0
1	1	1	1	1	1	+37.25

Note: Signal level is adjusted (before entering the filter) by an internal AGC with +12 dB or 0 dB gain, plus a fixed gain of 5 dB.

DATA Register: Address (A4–A1) = 1101

BIT NUMBER	BIT NAME	DESCRIPTION
Bit 7	Unused	
Bit 6	PLLJAM	When this bit is set, the DPLL will be reset by the next rising edge of the received baud clock. This bit must remain high for at least one baud period. It should be cleared by the processor to end the jamming mode. PLLFRZ (see below) overrides PLLJAM when both are enabled.
Bit 5	PLLFRZ	Phase locked loop freeze. When this bit is set, the DPLL begins to run freely regardless of the received baud clock. To re-enable the DPLL locking, the bit must be cleared by the processor. PLLFRZ overrides PLLJAM when both are enabled.
Bit 4	PLLFAST	When set, the DPLL operates in "fast" locking mode. In this mode, the DPLL is updated on every baud period by 13 µs steps. When this bit is cleared (default mode), the DPLL operates in "normal" locking mode and is updated once every 8 baud periods by 6.5 µs steps.
Bit 3–0	RD3–RD0	Four-bit Received Data. Used only in high speed (1200 or 2400 bps) mode, they are descrambled by the processor and shifted out by the SC11054. Sync to Async is also done by the SC11054, when in the asynchronous mode. RD0 is the first bit appearing on the RXD pin, followed by RD1, RD2 and RD3. In the 1200 bps mode, only RD0 and RD1 are shifted out during one baud period.

AUDIO Register: Address (A4–A1) = 1110

BIT NUMBER	BIT NAME	DESCRIPTION
Bit 7	Unused	
Bit 6	DISS	When this bit is set, the scrambler is disabled, when cleared, it is enabled. Transmit select bits (TXSEL0–2) override this bit when in "transmit internal mode"
Bit 5	PGCZ	When set, the output of the PGC is grounded. DC offset of the demodulator can be stored and canceled by the controller.
Bit 4–2	TEST	Test bits used for factory testing. For normal chip operation, these bits must be cleared.
Bit 1	ALC1	Audio level control bit 1.
Bit 0	ALC0	Audio level control bit 0. These two bits are used to control the audio level at AUDIO pin according to the following table:

ALC1	ALC0	AUDIO ATTENUATION (dB)
0	0	Audio off
0	1	12
1	0	6
1	1	0 (no attenuation)

Note: The audio signal may be amplified by 8 dB by the line receiver AGC before being fed to the audio attenuator.

CONTROL REGISTERS (Cont.)

FAX Register: Address (A4–A1) = 1111

BIT NUMBER	BIT NAME	DESCRIPTION
Bits 7–0	B7–B0	In V.27 or V.29 modes, this register has to be loaded at every interrupt with an 8-bit word that identifies constellation points for two consecutive baud periods. 4 LSB's correspond to first baud in time. In V.21FAX mode, when transmitting, the register should be loaded every eighth interrupt pulse. In V.21FAX, LSB is the data bit which is first in time.

SYNCHRONOUS OPERATION

Transmitter Timing

Case 1—SC11054 Provides the Timing to the Data Terminal Equipment (DTE). See Figure 4.

If the DTE can lock to an external clock, then all that needs to be done is to put the SC11054 in the synchronous mode. This provides a 2400/1200 Hz clock on the SCT pin that can be used as a clock source for the DTE. The Transmit Phase-Locked-Loop (TX PLL) of the SC11054 will be in free-running mode.

Case 2—SC11054 Should Lock Its Transmit Timing to the Clock Source Provided by the DTE.

In this case, after selecting synchronous mode, also select "Locked" mode.

The TX PLL of SC11054 will then synchronize itself to the clock provided on its "SCTE" pin.

Case 3—Slave mode. The Transmit Timing is slaved to the receiver recovered clock. Select synchronous and "Locked" mode and set SLAVE bit.

In either case, the SC11054 will sample the data on the rising edge of the clock.

Receiver Timing

In synchronous mode, the recovered clock will be provided on the SCR pin and the transitions of RXD will be on the falling edges of this clock. Data is valid on the rising edge of the clock.

SYNCHRONOUS MODE CHART

Transmitter Timing

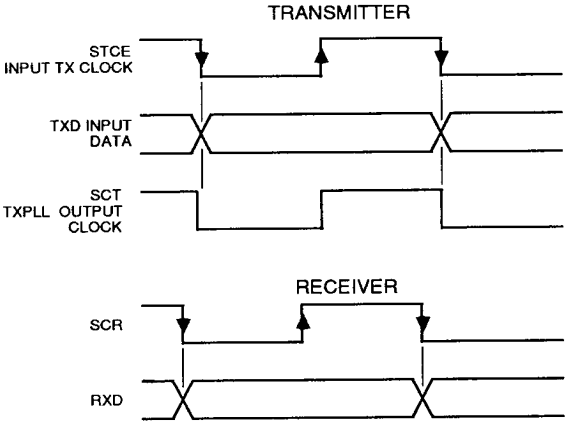


Figure 4a. SC11054 Synchronous Mode Timing Diagrams.

SPECIFICATIONS

Absolute Maximum Ratings (Notes 1–3)

Supply Voltage, V_{CC}–GND	7 V
DC Input Voltage (Analog Signals)	AGND–0.6 to V_{CC} +0.6 V
DC Input Voltage (Digital Signals)	DGND–0.6 to V_{CC} +0.6 V
Storage Temperature Range	–65 to 150°C
Power Dissipation (Note 3)	500 mW
Lead Temperature (Soldering 10 Sec.)	300°C

Operating Conditions

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNITS
T_A	Ambient Temperature		0		70	°C
V_{CC}	Positive Supply Voltage		4.5	5.0	5.5	V
AGND, DGND	Ground			0		V
F_C	Clock Frequency		9.8295	9.8304	9.8313	MHz
T_R, T_F	Input Rise or Fall Time	All digital inputs except CLKIN			500	ns
T_R, T_F	Input Rise or Fall Time	CLKIN			20	ns

DC Electrical Characteristics (T_A = 0 TO 70°C, V_{CC} = +5 V ± 10%)

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNITS
I_{CC}	Quiescent Current	Normal Power Down Mode		13 1.0	25 4	mA mA
V_{IH}	High Level Input Voltage; Digital pins		2.4			V
V_{IL}	Low Level Input Voltage; Digital pins				0.8	V
V_{OH}	High Level Ouput (I_{OH} = 0.5 mA)		2.4			V
V_{OL}	Low Level Ouput (I_{OL} = 1.6 mA)				0.6	V
VXTA	Maximum Peak Output Level on TXA pin	V_{CC} = +5 V	3			V_{PP}

Notes: 1. Absolute maximum ratings are those values beyond which damage to the device may occur.
2. Unless otherwise specified, all voltages are referenced to ground.
3. Power dissipation temperature derating—Plastic package: –12 mW/C from 65°C to 85°C.

SPECIFICATIONS (Cont.)

AC Electrical Characteristics

	SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
		Processor Bus Interface: (See Figure 4)					
1	TAVLL	Address valid to end of ALE		41			ns
2	TLLAX	Address hold after end of ALE		61			ns
3	TAVDV	Address valid to output data valid				336	ns
4	TRLDV	$\overline{RD}$ active low to output data valid				194	ns
5	TRXDZ	End of $\overline{RD}$ to output data Hi Z				61	ns
6	TLHLL	ALE pulse width		71			ns
7	TRLRH	$\overline{RD}$ pulse width		214			ns
8	TWLWH	$\overline{WR}$ pulse width		148			ns
9	TQVWX	Data valid to end of $\overline{WR}$ active		132			ns
10	TWXQX	Data hold after end of $\overline{WR}$		56			ns
11	TLLRL	End of ALE to $\overline{RD}$ or $\overline{WR}$ active		60			ns
12	TRHLH	End of $\overline{RD}$ to next ALE		60			ns
13	TWXLH	End of $\overline{WR}$ to next ALE		60			ns

BUS TIMING

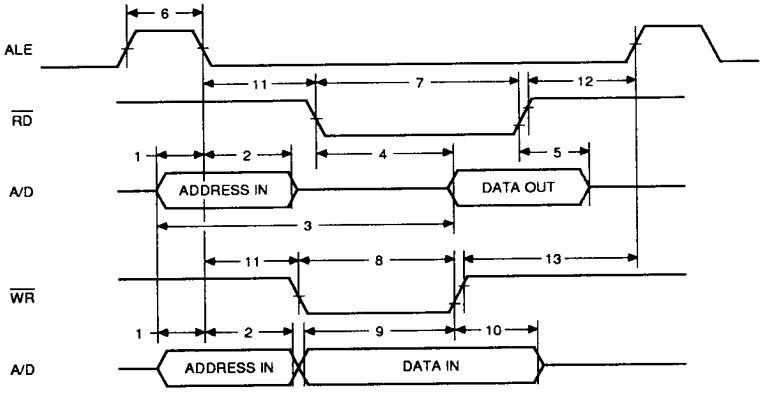


Figure 4b. Processor Bus Timing

SPECIFICATIONS (Cont.)

Modem Transmit Signals—Hz (Assume 9.8304 Crystal)

PARAMETER	CONDITIONS		NOM.	ACT.	UNITS
FSK Mod/Demod Frequencies					
Bell 103					
Answer Mark			2225	2226	Hz
Answer Space			2025	2024.4	Hz
Originate Mark			1270	1269.4	Hz
Originate Space			1070	1070.4	Hz
CCITT V.21					
Answer Mark			1650	1649.4	Hz
Answer Space			1850	1850.6	Hz
Originate Mark			980	978.34	Hz
Originate Space			1180	1181.53	Hz
Call progress monitor mode:		**MIN**	**TYP**	**MAX**	
Center frequency	ALB = 1, G5–G0 = 101111		480		Hz
Detect level (ED high) measured at RXA		–43			dBm
Reject level (ED low) measured at RXA				–48	dBm
Hysterisis		2			dB
Delay time (ED low to high)	EDC = 1.0 µF	10	15	24	ms
Hold time (ED high to low)	EDC = 1.0 µF	10	15	24	ms

DTMF Generator (Note 1)

PARAMETER	NOMINAL FREQUENCY	ALLOWABLE ERROR	ACTUAL ERROR
Row 1	697 Hz	±1%	–0.23%
Row 2	770 Hz	±1%	–0.01%
Row 3	852 Hz	±1%	–0.12%
Row 4	941 Hz	±1%	–0.39%
Column 1	1209 Hz	±1%	–0.35%
Column 2	1336 Hz	±1%	–0.93%
Column 3	1477 Hz	±1%	–0.48%
Column 4	1633 Hz	±1%	–0.91%
Guard Tones	550 Hz	±20 Hz	–2 Hz
	1800 Hz	±20 Hz	–2 Hz
Calling Tone	1300 Hz		–6 Hz
Answer Tone	2100 Hz	±15 Hz	+3.2 Hz
Calling Tone	1100 Hz	±38 Hz	–3.8 Hz
PIS Tone	462 Hz	±1.5 Hz	–0.05 Hz

SPECIFICATIONS (Cont.)

DTMF Generator (Cont.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Second Harmonic Distortion	VCC = +5 V TL2 = TL1 = TL0 = 0 Measured at TXA Pin		–40		dB
Row Output Level			–2		dBm
Column Ouput Level			0		dBm
550 Hz Guard Tone			–6		dB (Note 2)
1800 Hz Guard Tone			–9		dB (Note 2)
1300 Hz Calling Tone			–3		dBm
2100 Hz Answer Tone			–3		dBm
1100 Hz Calling Tone			–3		dBm
462 Hz PIS Tone			–3		dBm
Transmit level measured at TXA	Load = 1200 Ohms TL2 = TL1 = TL0 = 0 Squelched		–3	 –50	dBm dBm

Notes: 1: This assumes a clock of exactly 9.8304 MHz.

2: These levels are referenced to the TX signal level. When guard tones are added, the TXA level is adjusted to maintain a constant level on the line. For 1800 Hz, the adjustment is –0.97 dB; for 550 Hz, the adjustment is –1.76 dB, per the CCITT specification.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Data Mode	EDC = 1.0 µF; measured at RXA PGC = 0				
Energy detect level (ED low to high)				–43	dBm
Loss of energy detect level (ED low to high)		–48			dBm
Hysterisis		2	3		dB

Programmable Gain Controller (PGC)

Gain step size			0.75		dB
Dynamic range			47.25		dB
Response time (from change in PGC register to output of A to D converter)			1.0		ms

Filter Characteristics

Crosstalk rejection			70		dB
Power supply rejection			0		dB
DPLL Response times JAM or FRZ Fast			20 200		µs µs

APPLICATIONS INFORMATION

Applications

The SC11054 with an external control microprocessor, a telephone line interface and a suitable computer interface, can implement a complete 2400 bps Sendfax modem with a minimum of components and cost. Figure 7 shows the common portion of such a modem using the SC11054 with a telephone line interface. Sierra's SC22201, 128 byte E^2 memory is used to store default parameters and often used phone numbers. The SC11021 controller also supports a serial E^2 memory as an alternative. Figures 5 and 6 show the stand-alone and PC bus integral modems implemented with Sierra's SC11074/75 controllers. Figure 8 shows the connections for an external ROM special purpose controller using the SC11011. Figure 9 shows an RS-232C serial interface for implementing a stand-alone modem. Figure 10 shows a parallel bus interface for implementing an internal modem for an IBM PC/XT/AT compatible computer. Figure 11 shows a power supply schematic for a stand-alone modem application.

Various modem configurations can be realized by combining schematics shown in Figures 5 thru 11.

For performance evaluation, a circuit shown in Figure 12 can be used to obtain a constellation of the modem. Quality of the signal processing performed by the modem can thus be visualized by observing the constellation for various line conditions and signal to noise ratios.

Tone Detector Operation

The following circuit description clarifies the operation of Tone Detector, how it can be set up and how its output should be interpreted.

The Tone Detector works very differently from energy/carrier detect as follows:

a) Carrier/energy detect looks for the presence of energy and does not check the frequency.

b) Tone Detector is a digital timer. The input signal is passed through a Schmitt trigger with ±50mV hysteresis and the period of the output signal is checked by a digital timer to see if it falls within allowed limits. This block does not care about the energy of the signal unless it becomes so weak that it affects the period of the Schmitt-trigger output (i.e. close to hysteresis levels). The Tone Detector verifies 4 consecutive periods of signal before turning the corresponding bit "on". After this time, if one of the zero-crossings of the signal is corrupted (say, due to noise) it will not pass the period-check and the output bit will return "low" and wait for four new consecutive cycles of the tone with clean zero-crossings.

From the above explanation we see that:

1) Tone Detector and carrier/energy detect complement each other and for reliable tone detection, the output of both has to be monitored to check frequency and energy simultaneously.

2) Weak signals are more vulnerable to corruption by noise; consequently, the tone detector output may not stay steadily high, so its output should be integrated in software. In other words, if a given "tone bit" stays on at least 70% of the time within a time frame (say, within 40 msec) it should be considered present. Note that since the output of this block is updated at every 4 cycles of tone, then reading the output at shorter intervals just provides the same result.

As Figure 3 shows, for tone detect to function properly, its preceding

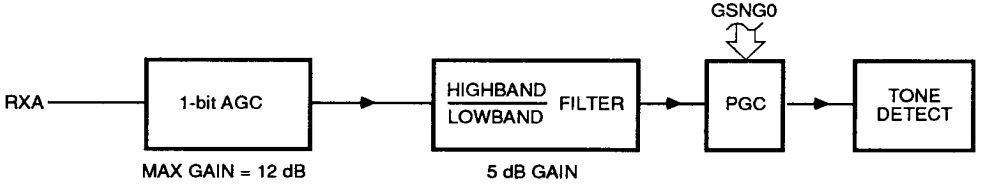


Figure 3. Tone Detector Signal Path

block has to be set up properly; i.e. Filter has to in the right band to allow passage of tone and the PGC gain has to be set up correctly to provide proper signal level to tone detect which has ±50 mV hysteresis at its input. Assuming that PGC gain code is "1F", the PGC gain will be 13.25 dB. If input level at RXA is -40dBm, the 1-bit AGC will be at its max gain and the overall gain from input pin (RXA) to tone detector input will be:

G = 12+5+13.25 = 30.25 dB
Tone Detector input = -40+30.25 = -9.75 dBm = 713 mVp-p

This is 7 times the hysteresis of Tone Detector!

So, the part should not have problems detecting -40dBm and even weaker signals if Filter and PGC are set up correctly. Reliability of detection in presence of noise can be improved by implementing the above recommendations.

Firmware

The SC11054 Sendfax modem provides all the signal processing required to dial, answer, connect, send and receive data and to send facsimile transmissions to any Group III fax machine or modem. Firmware is available from Sierra Semiconductor at no charge which works with our special controllers to perform adaptive equalization, T.30 handshake, call progress monitoring, dialing and data transmission while presenting a standard AT command set interface to the DTE. Compatible software is available from third parties for a variety of DTE environments, including MS-DOS, Windows 2 & 3, Macintosh and others. In addition, error correction and compression firmware is available, combining MNP and V.42 standards with data and Sendfax capability. Contact Sierra for details.

Power Supply Decoupling and Circuit Layout Consideration

For optimum performance at low received signal levels with low S/N ratios, it is important to use the recommended power supply decoupling circuit as shown in Figure 7.

Small inductors in series with the supplies help suppress RFI as well as improve the power supply noise rejection capability of the SC11024 . A 10 Ω, 1/4W resistor in place of, or in series with, the inductor in the SC11054 power lead has been found to be helpful in computer based products or where the power supply is particularly noisy.

The 10 µF capacitors should be a tantalum type while the 0.1 µF capacitors should have good high frequency rejection characteristics—monolithic ceramic types are recommended. It is important to locate the decoupling capacitors as close to the actual power supply pins of the SC11054 as possible. It is also recommended that the analog ground and digital ground buses be routed separately and connected at the common ground point of the power supply.

A Ferrite bead on the 5V input to the circuit board should also be considered, both from a modem performance standpoint, as well as an aid in reducing RF radiation from the phone line.

APPLICATIONS INFORMATION (Cont.)

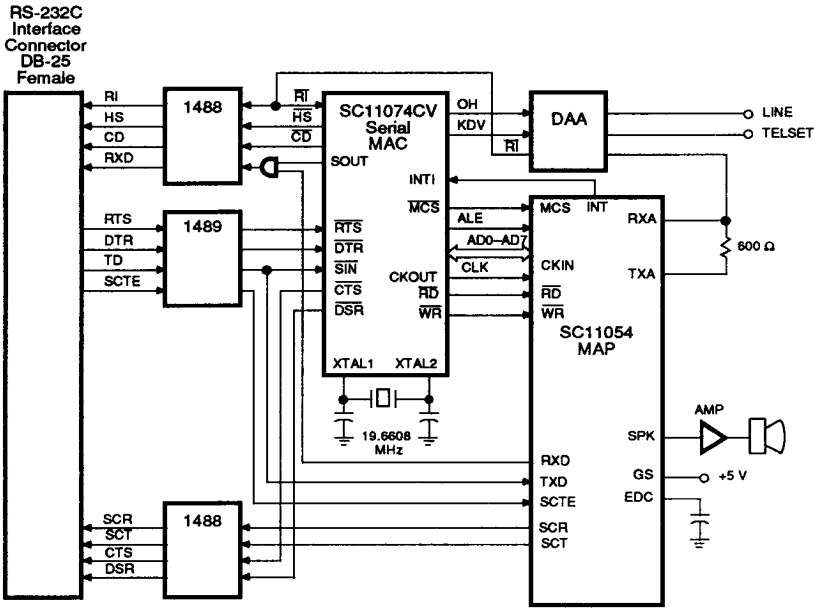


Figure 5. V22 bis Standalone Sendfax & Data Modem with Internal ROM.

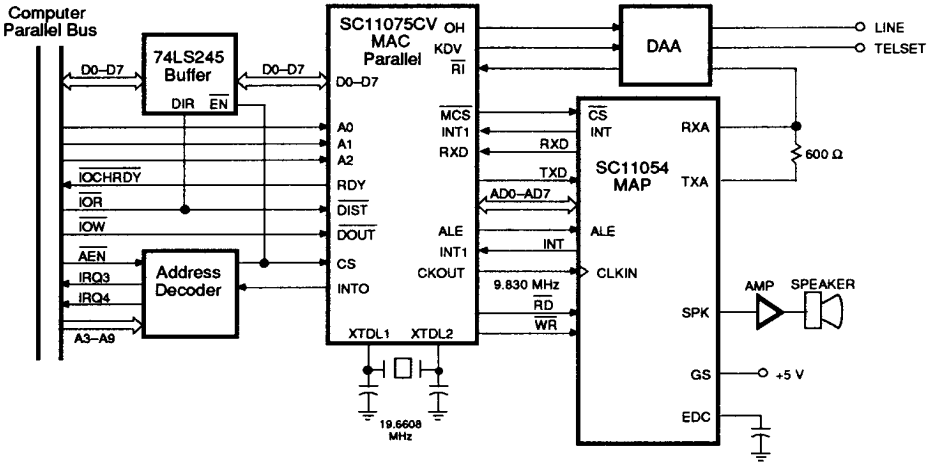
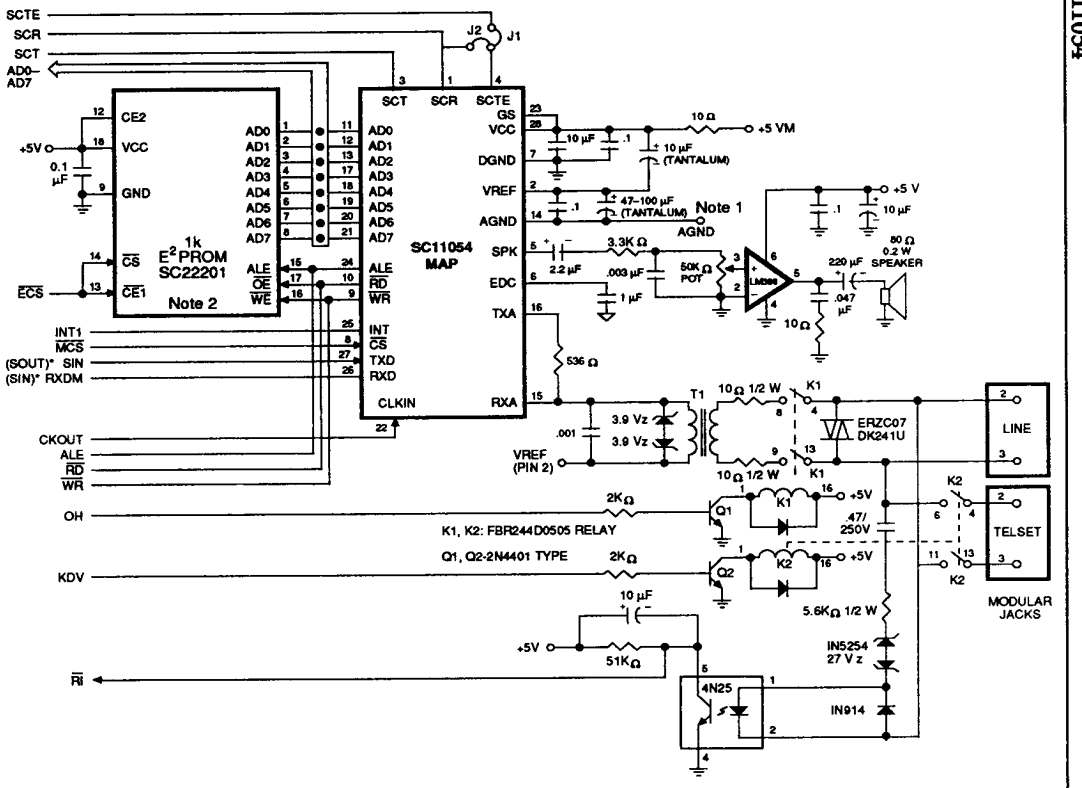


Figure 6. Internal Sendfax & Data Modem for PC Bus Applications with Internal ROM.

APPLICATIONS INFORMATION (Cont.)



Note 1: Connect analog ground directly to common of the power supply filter capacitor.

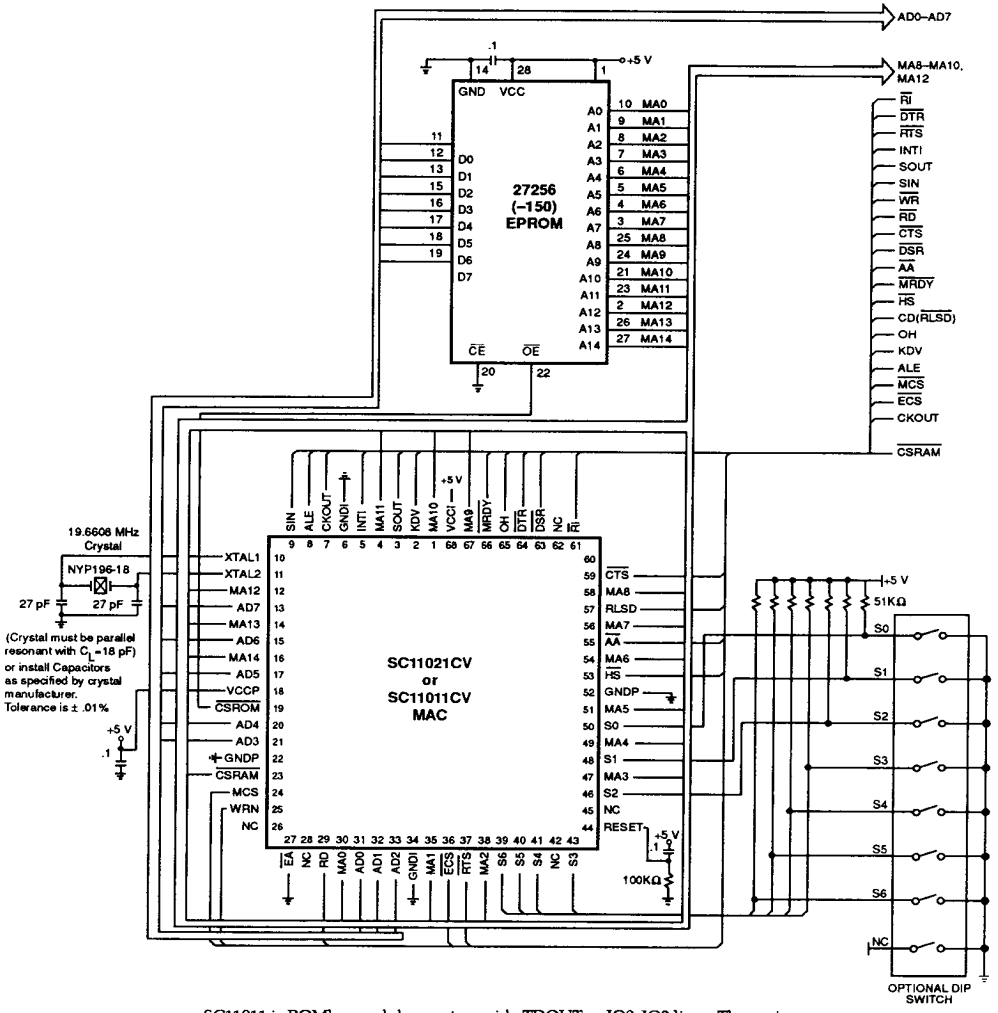
Note 2: A serial E^2 PROM may be substituted when using the SC11021 Modem Advanced Controller.

Note 3: For external clocking of the transmitter, install J1 and set bit 6 of the MCRA; omit J2.
For slave clocking of the transmitter, install J2 and set bit 6 of the MCRA; omit J1.
For normal operation, omit J1 and J2, and clear bit 6 of the MCRA.

*When used in the configuration as a parallel modem (Figure 6), connect Pin 27 of SC11054 to SOUT pin of controller and connect Pin 26 of SC11054 to SIN pin of controller.

Figure 7. Common Portion of Sendfax & Data Modem.

APPLICATIONS INFORMATION (Cont.)



SC11011 is ROMless and does not provide TDOUT or IO0–IO3 lines. These pins are "No Connect" on SC11011.
SC11021 is ROMless and can address 32k external ROM.
Consult controller data sheet for programming information.

Figure 8. Special Purpose Control Processor for Stand-Alone or Parallel Applications.

APPLICATIONS INFORMATION (Cont.)

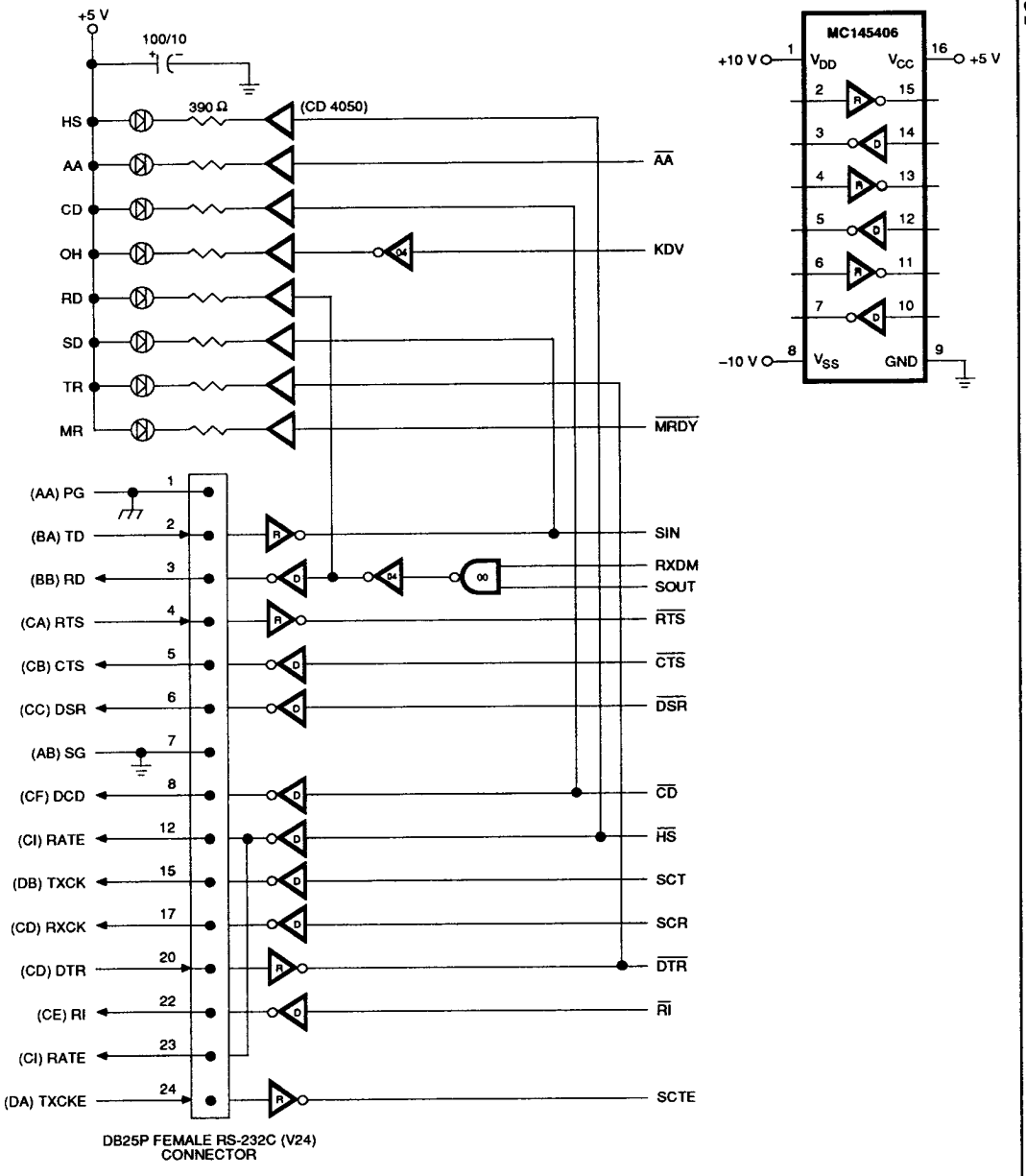


Figure 9. RS-232C Interface for Stand-Alone Modem Application.

APPLICATIONS INFORMATION (Cont.)

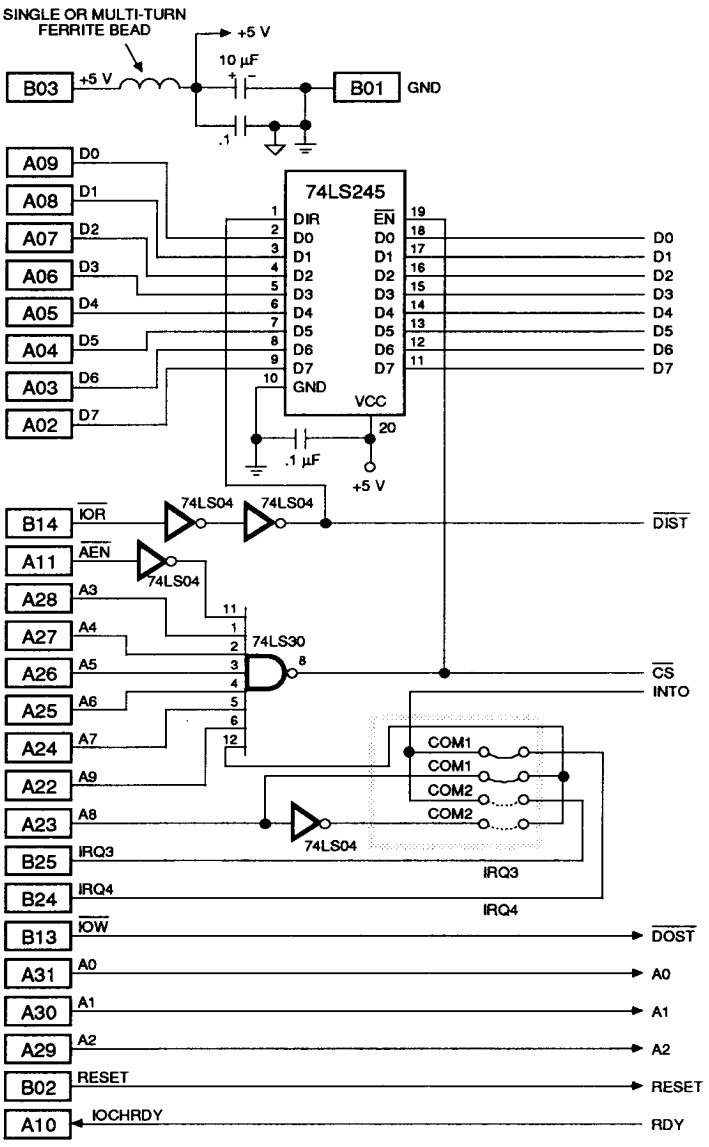


Figure 10. IBM PC/XT/AT Compatible Computer Bus Interface for SC11075 Controller of Figure 6.

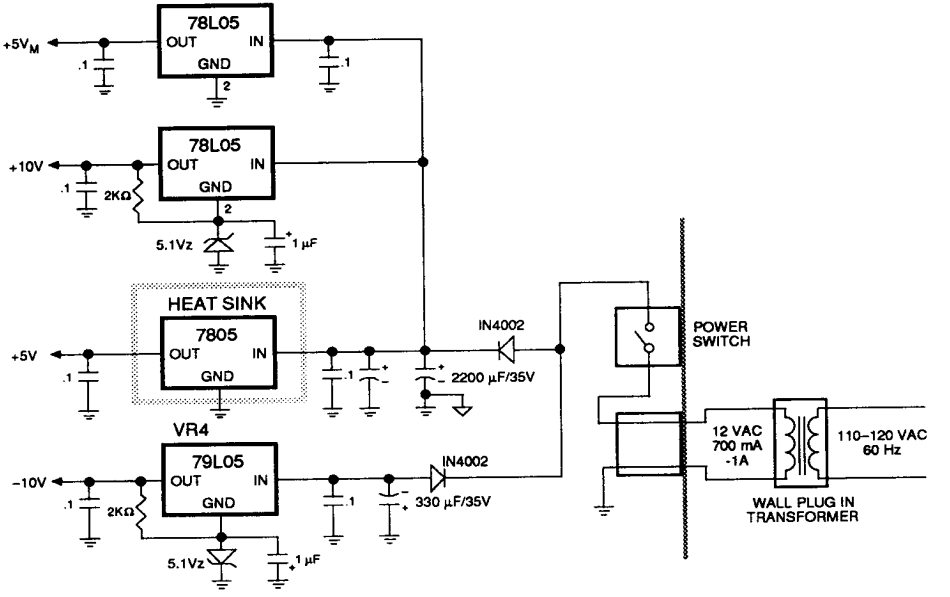


Figure 11. A Typical Power Supply for Stand-Alone Modem Application.

APPLICATIONS INFORMATION (Cont.)

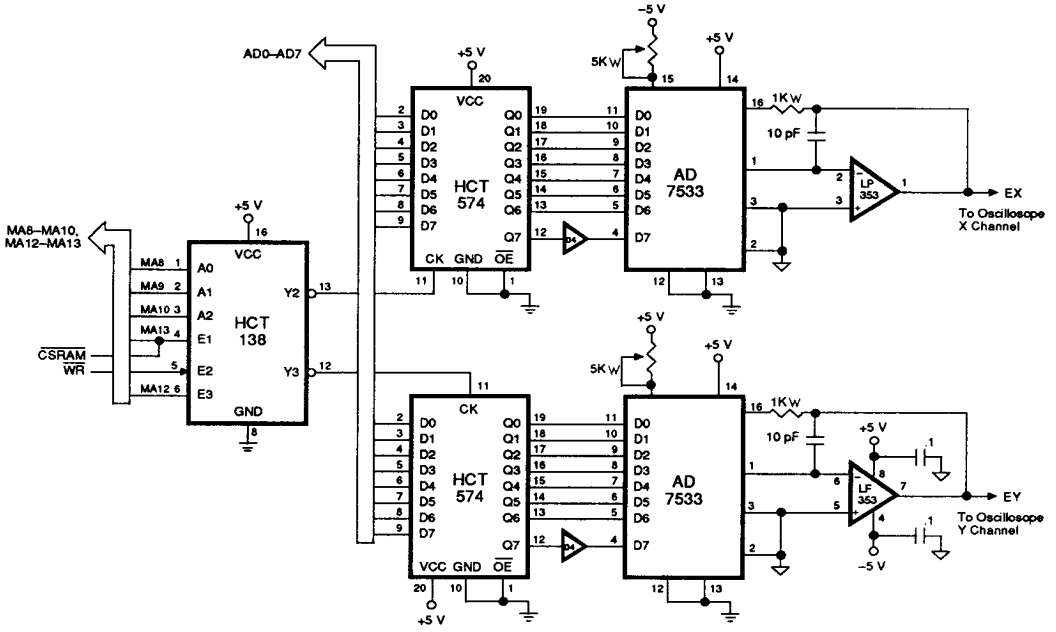


Figure 12a. Test Circuit to Generate Constellation Display.

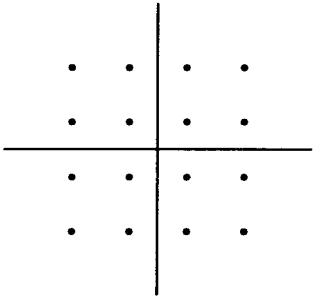


Figure 12b. Constellation for V22bis Mode Modem.