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ICs for Communications

Quad ISDN 2B1Q Echocanceller Digital Front End
Quad IEC DFE-Q

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PEF 24911 Version 1.2

Data Sheet 12.97

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1 Overview

The PEB 24911 Quad ISDN 2B1Q Echocanceller Digital Front End (Quad IEC DFE-Q) is the digital part of an optimized ISDN 2B1Q-U-Interface Line card chip set. It features 4 independent digital signal processors providing, in conjunction with the PEB 24902 ISDN Quad Analog Front End, full duplex data transmission at the U reference point according to ANSI T1.601 (1992), ETSI ETR 080 (1996) and ITU-T G.961 standards.

The PEB 24911/PEB 24902 chip set is based on the PEB 2091 IEC-Q V4.4 single chip ISDN U-transceiver. The IEC-Q V4.4 is approved by Bellcore.

The PEB 24911 comes in a M-QFP 64 package.

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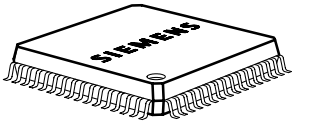
Quad ISDN 2B1Q U Transceiver PEB 24911
Quad IEC DFE-Q
Enhanced Serial Communications Controller with 8 Channels PEF 24911
ESCC8

Version 1.1 **CMOS**

1.1 Features



P-MQFP-100-2

- Full duplex data transmission and reception at the U-reference point compliant to:

  ANSI T1.601–1992, standard

  ETSI ETR 080 (1996), report

  ITU-T G.961 recommendation
- 144 kbit/s user bit rate over a two-wire subscriber loop.
- 2B1Q-block code (2 binary, 1 quaternary).
- 80-kHz symbol rate
- Activation and deactivation procedure.
- Meets transmission requirements for loop #1 through loop #15 of ANSI's 15 telephone plant test loops.
- Meets transmission requirements for loop #1 through #8 of ETSI's 8 telephone plant test loops.
- Adaptive echo cancellation.
- Adaptive equalization.
- Automatic polarity adaption.
- Clock recovery (frame and bit synchronization) in all applications.
- Automatic gain control.
- Low power consumption
- Extended temperature range (– 40...to 85 ×C) available
- U-interface propagation delay measurement
- LT-PBX mode allowing D-channel arbitration and synchronization of DECT base stations
- IOM-2 System Interface
- 4 relay driver pins per port addressable by Monitor command
- 2 status pins per port reporting to the Monitor channel
- Activation procedure with the 15 s limit disabled to cope with regenerators
- JTAG boundary scan path

Type	Ordering Code	Package
PEB 24911		P-MQFP-100-2

1.2 Logic Symbol

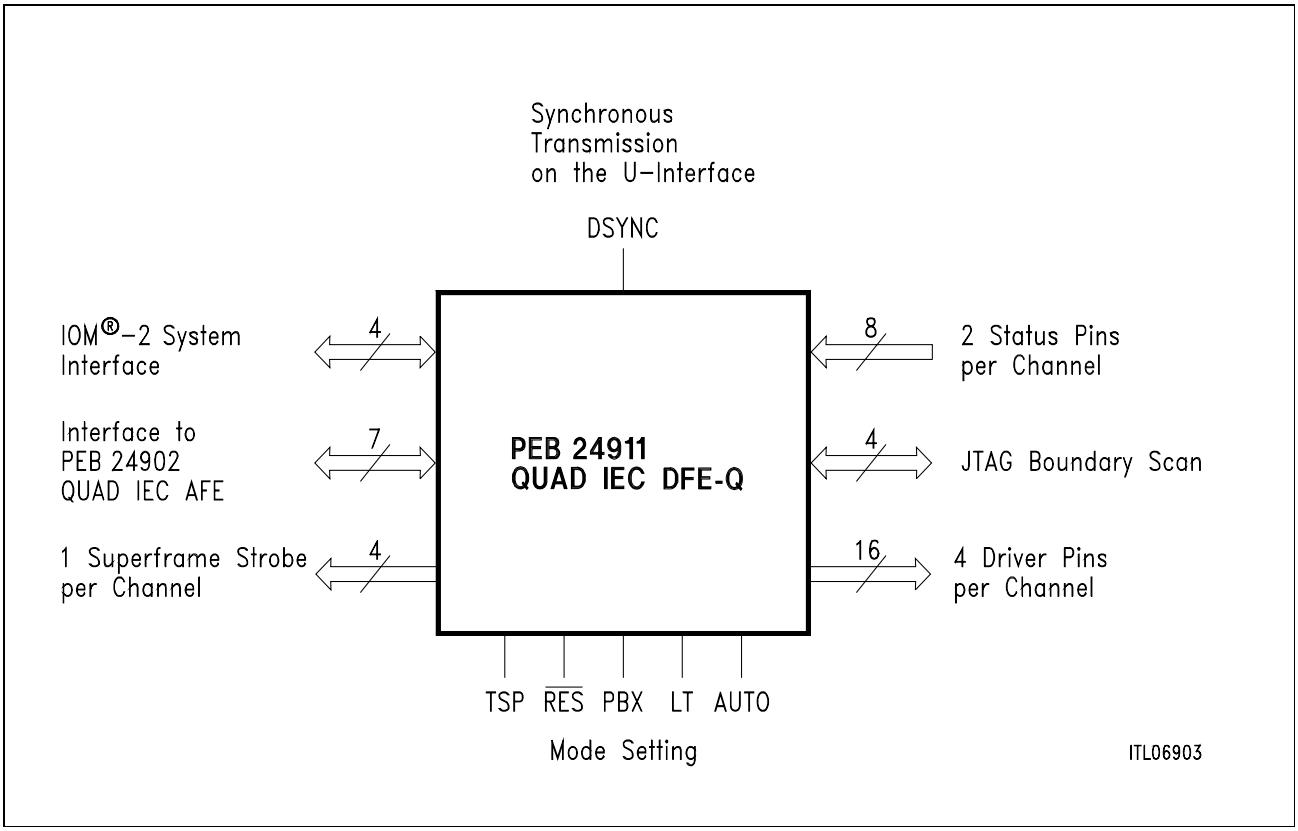


Figure 1
Logic Symbol

1.3 Pin Configuration

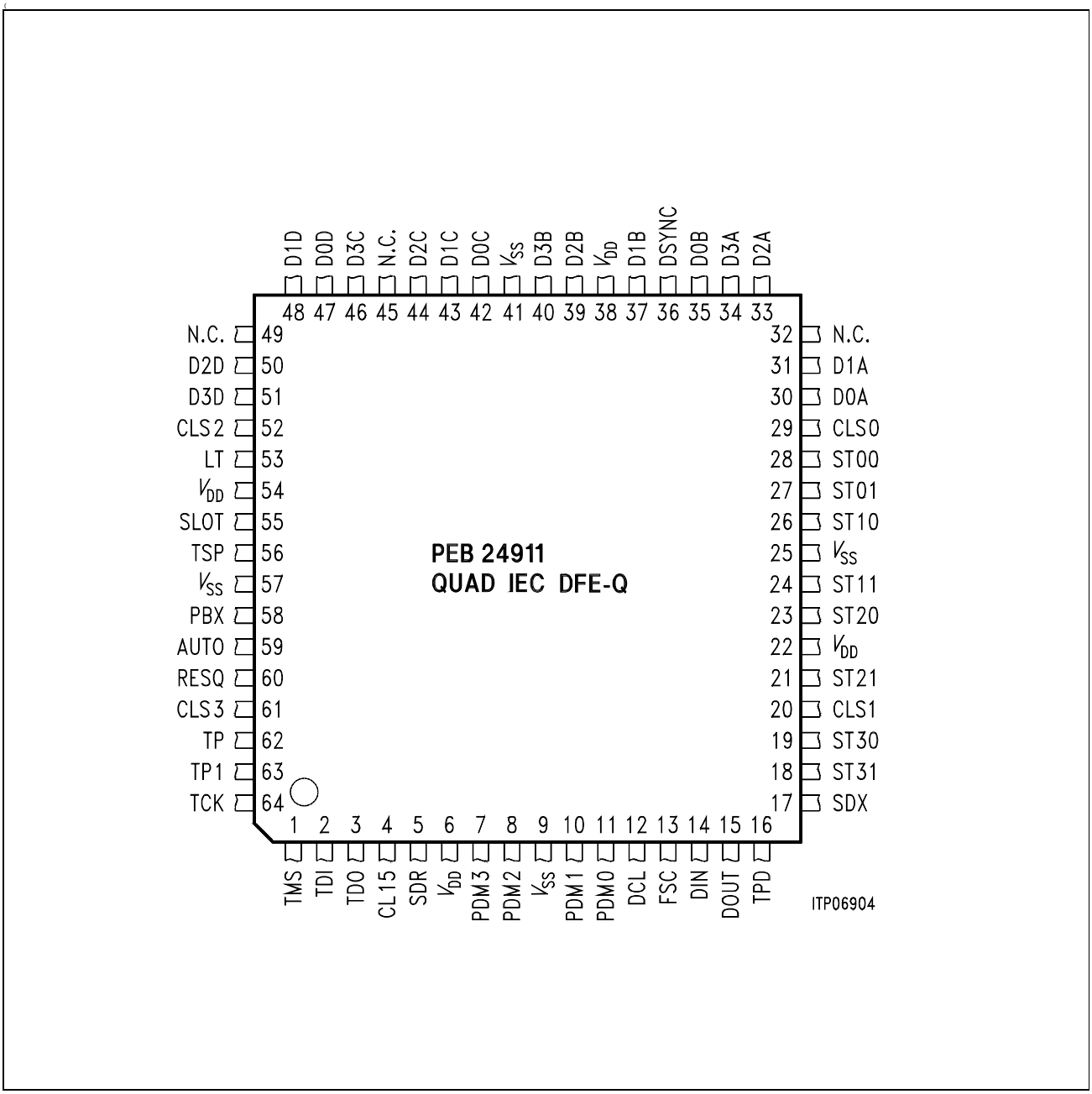


Figure 2
Pin Configuration, Top View

1.4 Pin Definitions and Functions

The following tables group the pins according to their functions. They include pin name, pin number, type, a brief description of the function, and cross-references referring to the sections in which the pin functions are discussed.

Pin No.	Symbol	Input (I) Output (O)	Description
Power Supply Pins			
6, 22, 38, 54	VDD		5V +/-5% supply voltage
9, 25, 41, 57	GND		0V
JTAG Boundary Scan			
64	TCK	I	Test Clock
1	TMS	I	Test Mode Select, internal pullup resistor
2	TDI	I	Test Data Input, internal pullup resistor
3	TDO	O	Test Data Output
IOM-2 Interface			
14	DIN	I	Data in. Input of IOM-2 data synchronous to DCL clock
15	DOUT	O Open Drain	Data out. Output of IOM-2 data synchronous to DCL clock.
13	FSC	I	Frame synchronisation clock. The start of the B1 channel in time slot 0 is marked. FSC = high for one DCL period indicates a superframe marker. FSC = high for at least two DCL periods marks standard frames.
12	DCL	I	Data clock. Clock range 2048 to 4096 kHz.
Miscellaneous Function Pins			
59	AUTO	I	Selection between auto- and transparent mode for EOC channel processing. AUTO = 1 selects automode on all ports.

Pin No.	Symbol	Input (I) Output (O)	Description
58	PBX	I	LT-PBX-mode, mode setting together with LT pin
29	CLS0	O	Pulse of 12 ms period, high time 125 µs indicating superframe on port 0
20	CLS1	O	Pulse of 12 ms period, high time 125 µs indicating superframe on port 1.
52	CLS2	O	Pulse of 12 ms period, high time 125 µs indicating superframe on port 2.
61	CLS3	O	Pulse of 12 ms period, high time 125 µs indicating superframe on port 3.
30	D0A	O	Relay driver pin of line port 0, addressable via Mon8-command within IOM channel 0/4 at bit position A (see Table **14**). Default after Pin-reset is low. C/I-code reset does not affect the state.
35	D0B	O	Relay driver pin of line port 0, addressable via Mon8-command within IOM channel 0/4 at bit position B (see Table 14). Default after Pin-reset is low. C/I-code reset does not affect the state.
42	D0C	O	Relay driver pin of line port 0, addressable via Mon8-command within IOM channel 0/4 at bit position C (see Table 14). Default after Pin-reset is low. C/I-code reset does not affect the state.
47	D0D	O	Relay driver pin of line port 0, addressable via Mon8-command within IOM channel 0/4 at bit position D (see Table 14). Default after Pin-reset is low. C/I-code reset does not affect the state.
31	D1A	O	Relay driver pin of line port 1, addressable via Mon8-command within IOM channel 0/4 at bit position A (see Table 14). Default after Pin-reset is low. C/I-code reset does not affect the state.

Pin No.	Symbol	Input (I) Output (O)	Description
37	D1B	O	Relay driver pin of line port 1, addressable via Mon8-command within IOM channel 0/4 at bit position B (see Table 14). Default after Pin-reset is low. C/I-code reset does not affect the state.
43	D1C	O	Relay driver pin of line port 1, addressable via Mon8-command within IOM channel 0/4 at bit position C (see Table 14). Default after Pin-reset is low. C/I-code reset does not affect the state.
48	D1D	O	Relay driver pin of line port 1, addressable via Mon8-command within IOM channel 0/4 at bit position D (see Table 14). Default after Pin-reset is low. C/I-code reset does not affect the state.
33	D2A	O	Relay driver pin of line port 2, addressable via Mon8-command within IOM channel 0/4 at bit position A (see Table 14). Default after Pin-reset is low. C/I-code reset does not affect the state.
39	D2B	O	Relay driver pin of line port 2, addressable via Mon8-command within IOM channel 0/4 at bit position B (see Table 14). Default after Pin-reset is low. C/I-code reset does not affect the state.
44	D2C	O	Relay driver pin of line port 2, addressable via Mon8-command within IOM channel 0/4 at bit position C (see Table 14). Default after Pin-reset is low. C/I-code reset does not affect the state.
50	D2D	O	Relay driver pin of line port 2, addressable via Mon8-command within IOM channel 0/4 at bit position D (see Table 14). Default after Pin-reset is low. C/I-code reset does not affect the state.

Pin No.	Symbol	Input (I) Output (O)	Description
34	D3A	O	Relay driver pin of line port 3, addressable via Mon8-command within IOM channel 0/4 at bit position A (see Table 14). Default after Pin-reset is low. C/I-code reset does not affect the state.
40	D3B	O	Relay driver pin of line port 3, addressable via Mon8-command within IOM channel 0/4 at bit position B (see Table 14). Default after Pin-reset is low. C/I-code reset does not affect the state.
46	D3C	O	Relay driver pin of line port 3, addressable via Mon8-command within IOM channel 0/4 at bit position C (see Table 14). Default after Pin-reset is low. C/I-code reset does not affect the state.
51	D3D	O	Relay driver pin of line port 3, addressable via Mon8-command within IOM channel 0/4 at bit position D (see Table 14). Default after Pin-reset is low. C/I-code reset does not affect the state.
53	LT	I	Mode pin, selects LT-Mode or LT-PBX-mode together with the PBX pin
60	RESQ	I	Reset of all four line ports, asynchronous signal, low active
55	SLOT	I	IOM slot selection. SLOT = 0 selects slots 0 to 3; SLOT = 1 selects slots 4 to 7
28	ST00	I	Status pin 0 of line port 0, status is passed to IOM-2 channel 0/4 via Mon8-message at bit position S_0. (See Table 14)
27	ST01	I	Status pin 1 of line port 0, status is passed to IOM-2 channel 0/4 via Mon8-message at bit position S_1. (See Table 14)
26	ST10	I	Status pin 0 of line port 1, status is passed to IOM-2 channel 1/5 via Mon8-message at bit position S_0. (See Table 14)

Pin No.	Symbol	Input (I) Output (O)	Description
24	ST11	I	Status pin 1 of line port 1, status is passed to IOM-2 channel 1/5 via Mon8-message at bit position S_1. (See Table 14)
23	ST20	I	Status pin 0 of line port 2, status is passed to IOM-2 channel 2/6 via Mon8-message at bit position S_0. (See Table 14)
21	ST21	I	Status pin 1 of line port 2, status is passed to IOM-2 channel 2/6 via Mon8-message at bit position S_1. (See Table 14)
19	ST30	I	Status pin 0 of line port 3, status is passed to IOM-2 channel 3/7 via Mon8-message at bit position S_0. (See Table 14)
18	ST31	I	Status pin 1 of line port 3, status is passed to IOM-2 channel 3/7 via Mon8-message at bit position S_1. (See Table 14)
62	TP	I	Test pin. Not available to user. Connect to GND.
63	TP1	I	Test pin. Not available to user. Connect to GND.
16	TPD	I	Test pin. Not available to user. Connect to GND.
56	TSP	I	Single pulse test mode. For activation refer to section **2.10.3.1**. When active, alternating 3.2V pulses are issued in 1.5 ms intervals. Connect to GND when not used.
36	DSYNC	I/O	DECT-Synchronize. Connects two Quad IEC DFE-Qs when performing synchronized transmission on 8 ports. Input with internal pulldown if SLOT = low; Output if SLOT = high

Interface to Analog Front End

4	CL15	I	Master Clock 15.36 MHz. All operations and the data exchange on the digital interface are based on this clock.

Pin No.	Symbol	Input (I) Output (O)	Description
11	PDM0	I	Input of the PEB 24902 Quad AFE second-order sigma-delta ADC pulse density modulated bit stream, line port 0
10	PDM1	I	Input of the PEB 24902 Quad AFE second-order sigma-delta ADC pulse density modulated bit stream, line port 1
8	PDM2	I	Input of the PEB 24902 Quad AFE second-order sigma-delta ADC pulse density modulated bit stream, line port 2
7	PDM3	I	Input of the PEB 24902 Quad AFE second-order sigma-delta ADC pulse density modulated bit stream, line port 3
5	SDR	I	Interface to the PEB24902 Quad AFE containing level information for the detection of the awake tone. The four lines are multiplexed on SDR.
17	SDX	O	Interface to the PEB24902 Quad AFE for the transmit and control data. Transmission is based on clock CL15 (15,36 MBit/sec). For each line port the following bits are exchanged: TD0, TD1, TD2: Transmit data RANGE: Range select LOOP: Analogue loop back switch PDOW: Power down/power up Synchronisation information

1.5 System Integration

The PEB 24911 Quad IEC DFE-Q is optimized to work in conjunction with the PEB 24902 ESCC8 on line modules in the central office, in the LT function of the access network or in PBX line modules. It supports the 2B1Q line code. A PLL internal to the PEB 24902 ESCC8 synchronises the 15.36 MHz master clock onto a PTT reference clock of either 8 KHz, 512 KHz or 2048 KHz. The Quad IEC DFE-Q receives this clock from the ESCC8.

The Quad IEC DFE-Q is connected to four time slots of the IOM-2 interface. The selection is done with the slot pin either to slots 0..3 (SLOT = low) or to slots 4..7 (SLOT = high).

Figure 3 illustrates the application in a 4 channel line card together with one PEB 24902 ESCC8.

Figure 4 shows an 8 channel application. One PLL generates the synchronised clock for all 4 devices. Note that the second PEB 24902 ESCC8 receives the 15.36 MHz clock in this application. It's PLL is deactivated. The clock pin (pin 26) of the second ESCC8 is tied to GND.

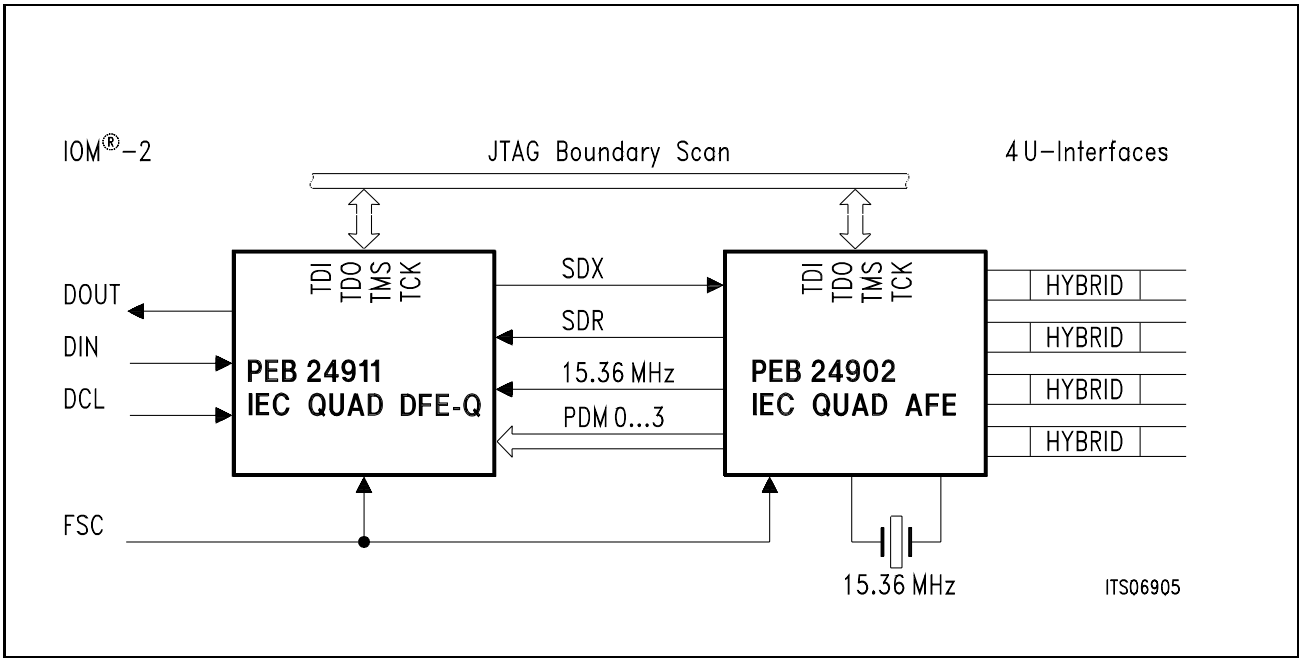


Figure 3
4 Channel LT Application

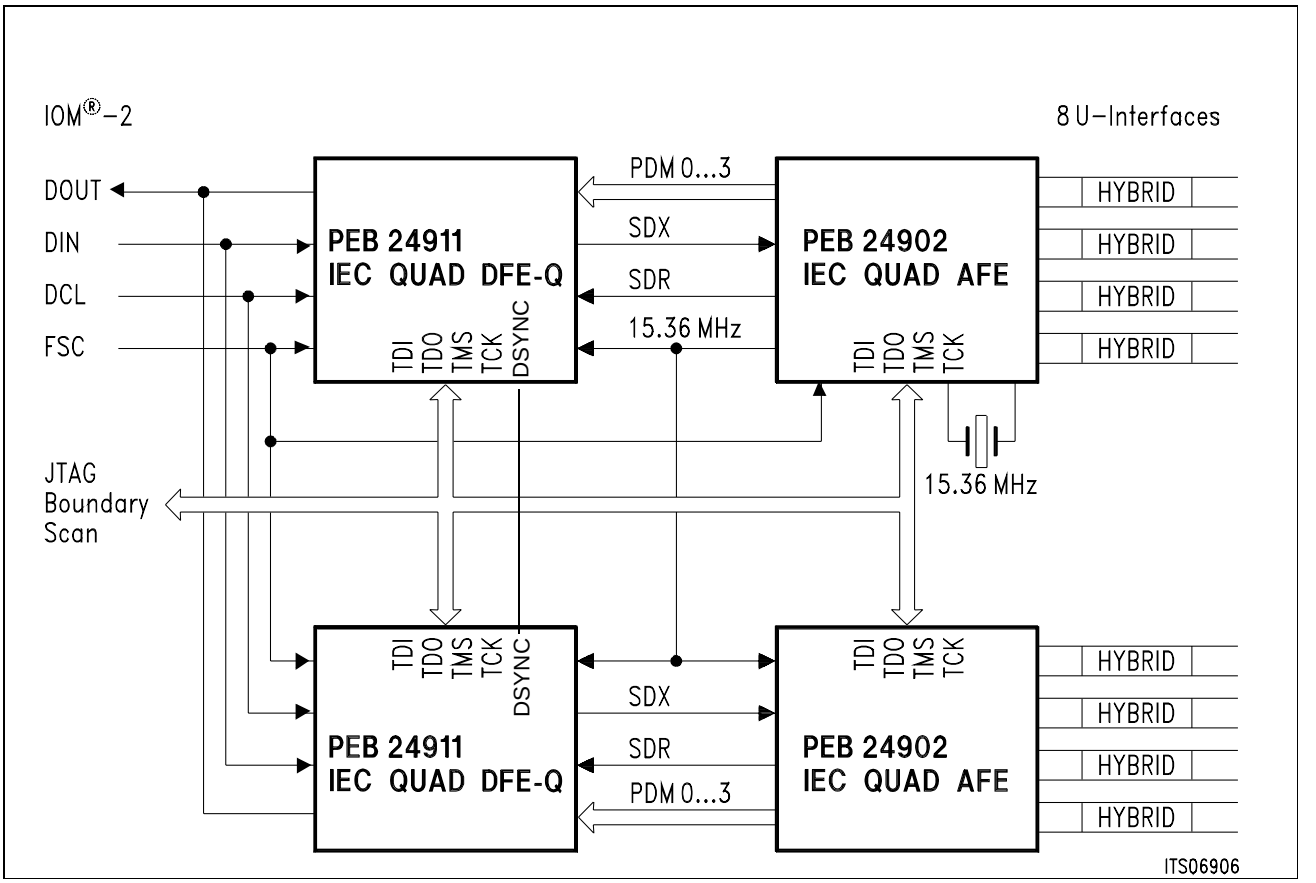


Figure 4
8 Channel LT Application

1.5.1 Application and Operational Modes

1.5.1.1 LT-Application

An LT-configuration with up to 2 Quad IEC DFE-Qs devices can be built with one PEB 2055 EPIC and two PEB 2075 IDEC. The EPIC controls the C/I-channel, the B-channel slot assignment and the MONITOR channel handling. The IDEC is a HDLC-controller for four independent D-channels.

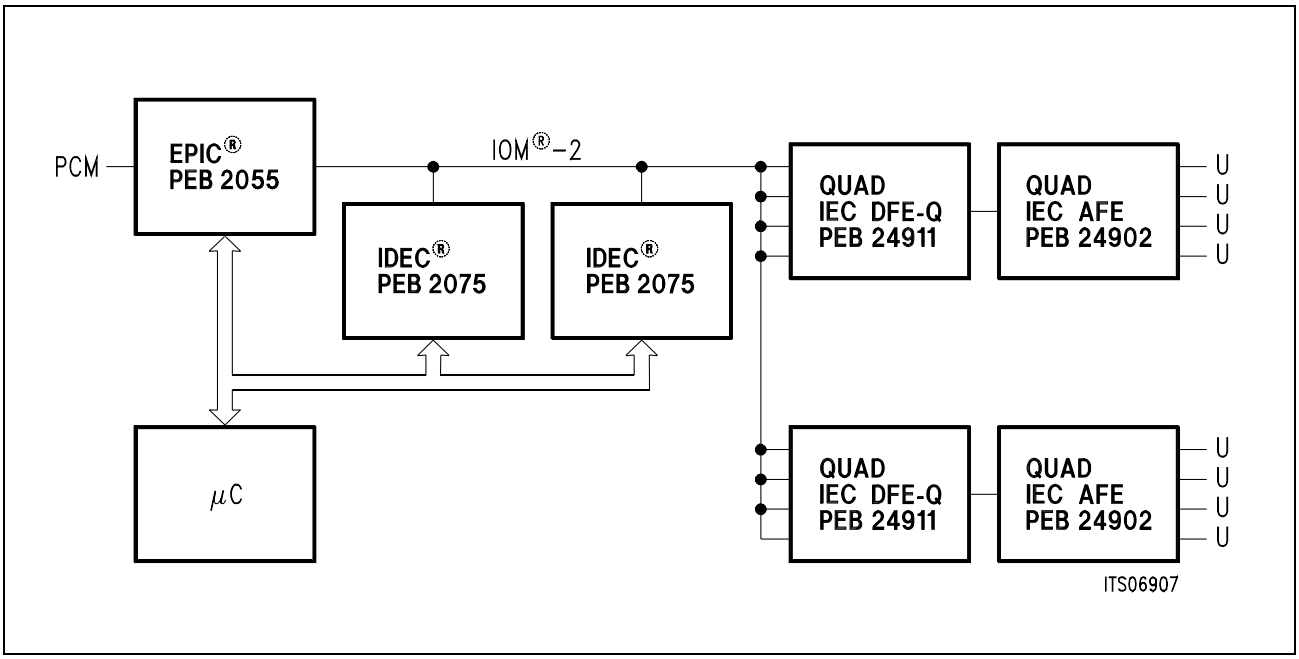


Figure 5
8 Channel LT-Application (overview)

1.5.1.2 LT-Application in PBX-Systems

The PEB 24911 Quad IEC DFE-Q can be used in PBX-Systems where an extended loop range is requested. It can replace the PEB 2096 OCTAT-P at the LT side. At the TE side, the PSB 2196 ISAC-PTE then has to be replaced by the PEB 2091 IEC-Q V5.1. This way, the Upn-Interface is replaced by a U interface providing up to 6 km of possible loop length using AWG26 lines, or up to 15km with AWG22 cable.

The Quad IEC DFE-Q allows the transfer of D-Channel arbitration information if the PEB 2091 IEC-Q V5.1 is used as NT transceiver.

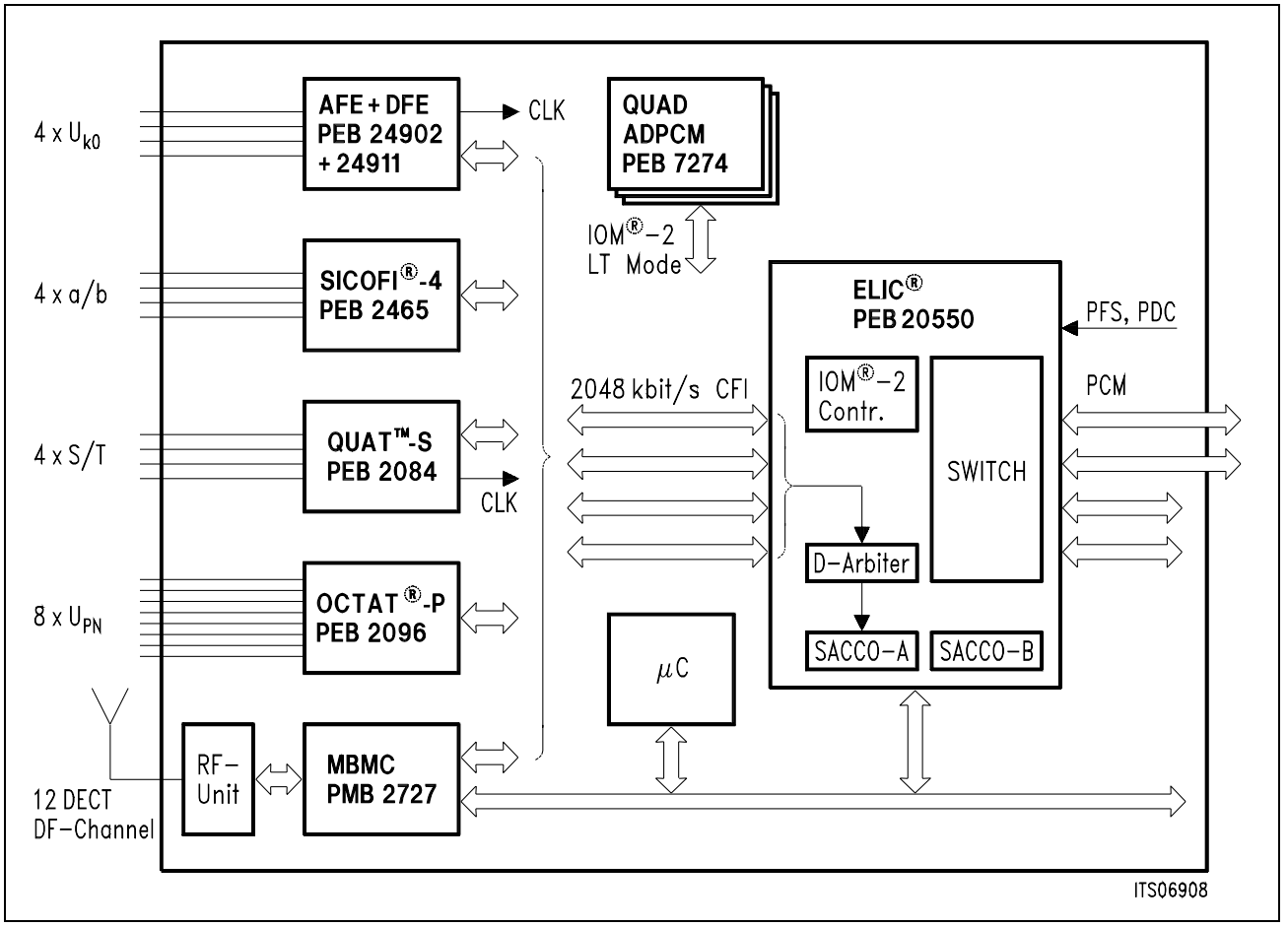


Figure 6
PBX Linecard with different Interfaces

1.5.1.3 LT-Application in 'Wireless PBX' or 'Radio in the Loop' Systems (using e.g. the DECT standard)

Synchronous data transmission on all 8 lines of two Quad IEC DFE-Q/ Quad IEC AFE sets connected to one IOM-2 interface is provided to allow opmtized use of DECT timeslots and frequencies in case cordless basestations are connected to the NT side.

The DFE-Q V1.2 also features the ability to measure the actual propagation delay of individual lines and thus makes it possible to compensate different line lenghts by external devices.

In a LT application with DECT synchronization the IOM-2 interface has to be operated at a DCL frequency of 4.096MHz, even if only one DFE-Q/AFE chip set is used. Besides the IOM-clocks (8KHz FSC, 4096KHz DCL) two supplementary clock signals, the superframe synchronization signal (SFSC) and a DECT synchronization signal have to be provided. Both clock signals are synchronous with respect to the IOM-2 clocks.

The 12ms periodic signal SFSC,which can be derived by division (factor: 96) from the 8 kHz FSC clock, is applied to the LT pin. The first negative edge at LT after HW reset will set the DFE-Q into „LT-PBX mode with DECT synchronization enabled“ (see table **1** for the different operating modes).

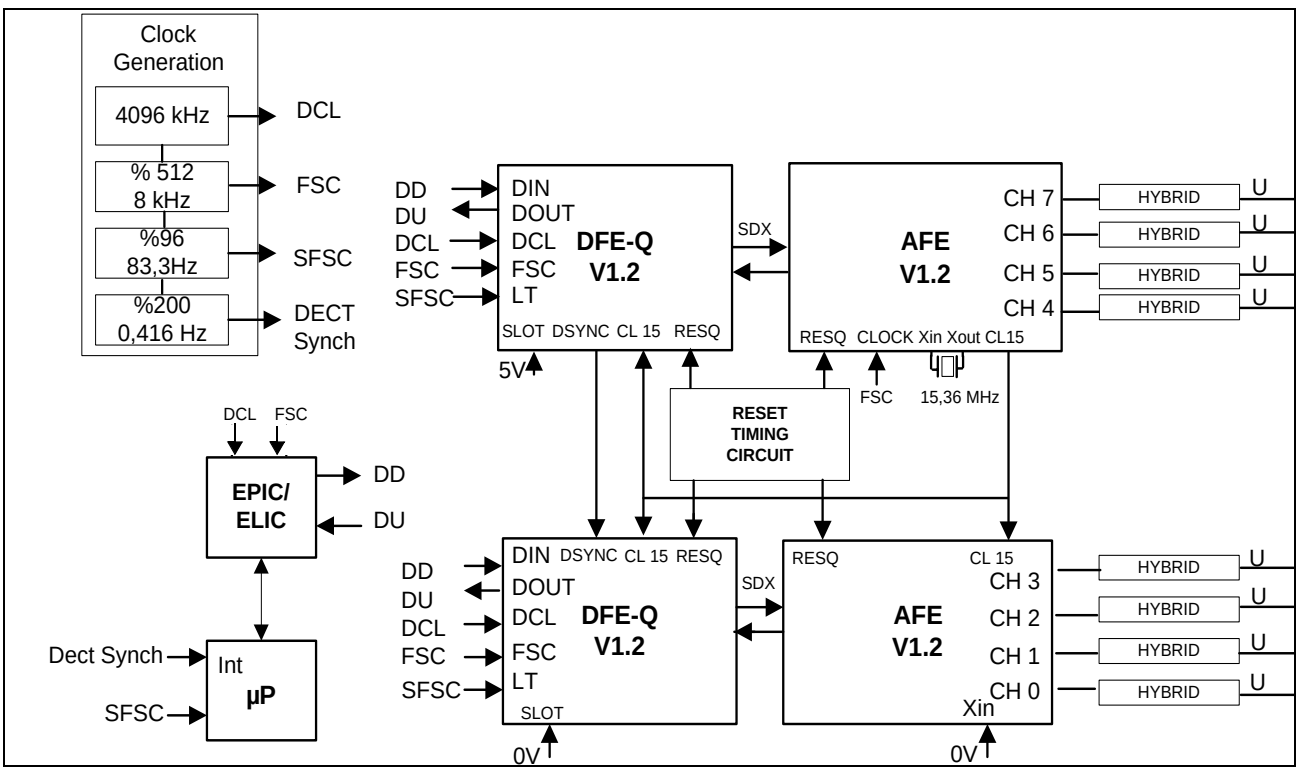


Figure 7

LT Application with Means for DECT Synchronization

The period of the DECT-sync. signal must be a common multiple of the 160ms DECT superframe and the 12ms U-superframe, e.g. 2.4s. The DECT sync. signal is used to synchronize several DECT Basestations (refer to figure **20**).

The DFE-Q with SLOT pin set to ’1’ outputs an internally generated synchronization signal at pin DSYNC that marks the point of time when the quat, frame and superframe counters are reset. In a 8 channel application the DSYNC signal is forwarded to the second DFE/AFE chip set with SLOT pin set to ’0’. In this mode the lower IOM-2

channels 0 to 3 are addressed and the DSYNC pin is automatically configured as input.

Thus it is guaranteed that after activation of all channels the quat, frame and superframe counters run synchronously resulting in aligned U frames which might be monitored by aligned CLS signals.

(Please refer to the Application Note **„A Dedicated Chip Set Features Synchronization of DECT-Basestatations Interfacing the U-Reference Point“** for a more detailed description of the system aspects)

1.5.2 Setting Operational Modes

Table 1 illustrates the effect of different mode-settings due to signals at the pins LT and PBX. There is the LT-mode as known from the PEB 2091 IEC-Q. Additionally, in the LT-PBX mode, the features mentioned in section “LT-Application in PBX-Systems” on page 19 can be enabled separately.

Table 1
Setting Operational Modes:

PBX*)	LT	Description
0	0	reserved
0	1	LT mode without DECT-synchronization, D-channel arbitration disabled
1	0	reserved
1	1	LT mode without DECT-synchronization, D-channel arbitration enabled
0	12ms periodic signal**)	LT-PBX-mode with DECT-synchronization, D-channel arbitration disabled
1	12ms periodic signal**)	LT-PBX-mode with DECT-synchronization, D-channel arbitration enabled

*) controls D-channel arbitration, ’0’ disabled, ’1’enabled

**) first negative edge enables LT-PBX-mode with DECT-synchronization

PBX= low and LT = high selects the **LT mode** as known in the PEB 2091 IEC-Q. The CLS pin of each line port issues a clock of 12 ms period which is synchronized to the corresponding superframe marker. It’s high phase is 125 µs. This pulse can be used for test purpose, e.g. to trigger an oszilloscope.

The $\overline{\text{PBX}}$-pin tied to low disables the D-channel arbitration feature. No reflection of the C/I-Codes 1000 and 1100 onto EOC-messages will be done.

Please note:

With RESQ= low no CLS signals will be available. Also when a channel is in power down state no signal will be issued at the respective CLS pin.

PBX= high and LT = high selects the **LT mode** as described above but with enabled D-channel arbitration (see chapter 2.5.1 for the D-channel arbitration procedure).

The first negative edge at LT selects the **LT-PBX mode**. It is different in one way from the LT mode: In the LT-mode, there is a delay between the IOM-slot and SDX which is not directly related to the used IOM slot. That is, incoming data of one IOM-frame leaves the Quad IEC DFE-Q at different times, depending on the IOM-slot. In LT-PBX-mode, the delay between IOM-2 and SDX is tied to the IOM-frame. That is, there is a constant time referred to the IOM frames until the data leaves the Quad IEC DFE-Q at SDX. Figure 8 illustrates the difference.

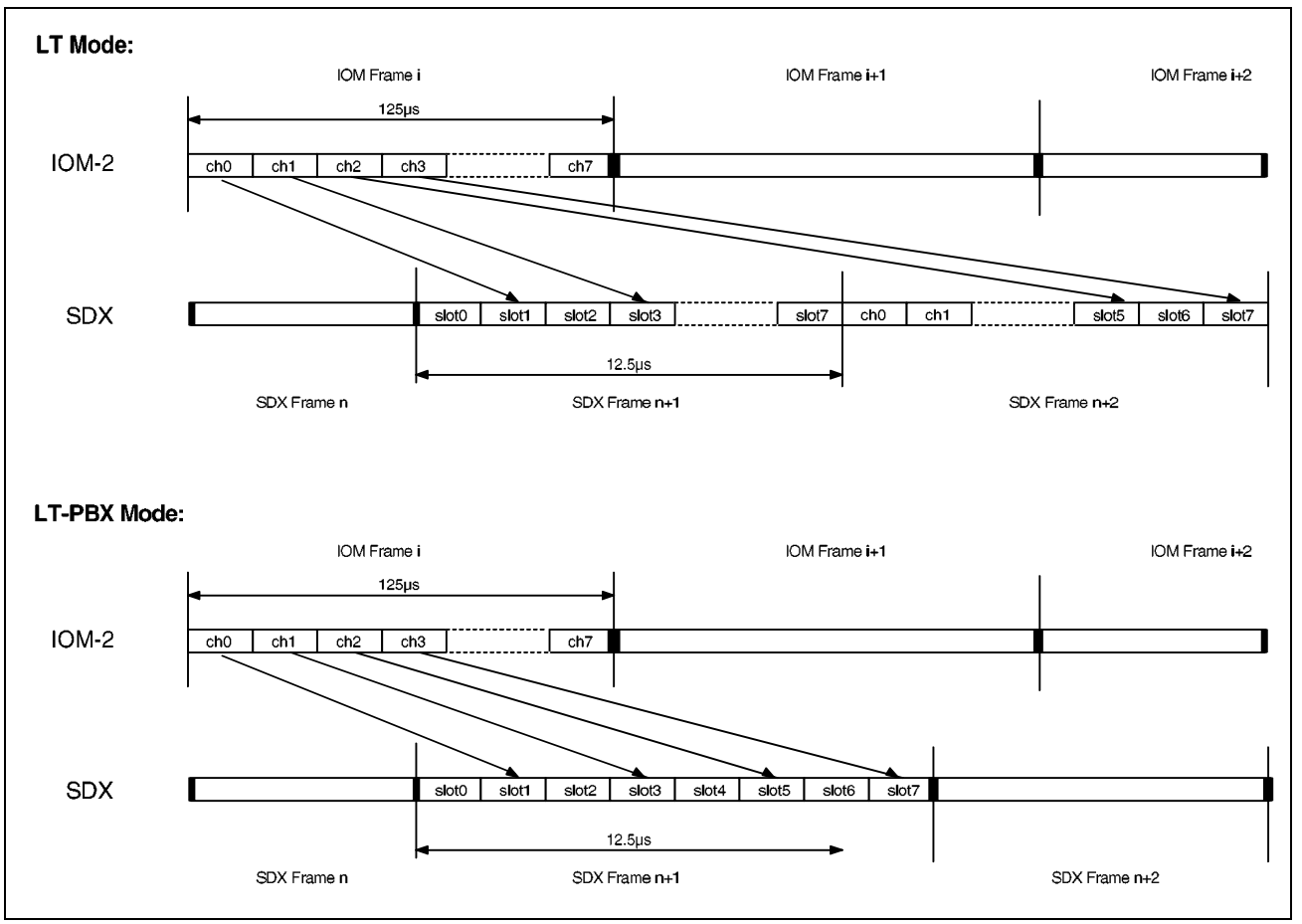


Figure 8

Delay IOM-2 <-> SDX in LT Mode and in LT-PBX Mode

In the LT-PBX-mode a periodic 12ms signal applied to the LT pin enables synchronized transmission of all U-interface signals and triggers the eoc=25h message that calls for an activation of the S/G-bit on the NT-side. Please refer to the Application note **„A Dedicated Chip Set Features Synchronization of DECT-Basestatations Interfacing the U-Reference Point“** for a more detailed information on the synchronization mechanism.

Figure **9** illustrates the LT to FSC timing (see Table 32, “LT to FSC timing,” on page 143 for detailed timing information). Please note that both signals, FSC and LT, have to be synchronous with respect to the DECT sync signal period of 2.4s (see figure 20).

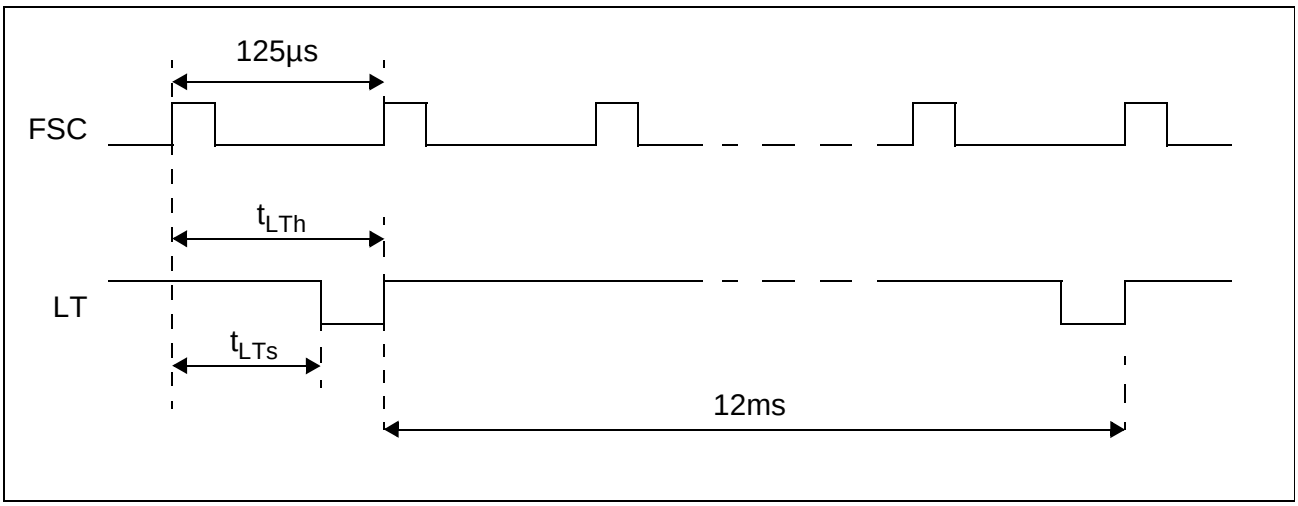


Figure 9
LT to FSC Timing

In any mode with the $\overline{LT}$-pin tied to either low or high, no signal edge will ever trigger the eoc= 25h message and the corresponding Monitor command will have no effect. That is, synchronization to the DECT sync signal is disabled.

1.6 Clock Generation

The U-transceiver has to synchronize onto an externally provided PTT-master clock. A phase locked loop (PLL) is integrated in the ESCC8 to generate the 15.36 MHz Quad IEC system clock as shown in figure **3**. A synchronized Quad IEC system clock guarantees that U-interface transmission will be synchronous to the PTT-master clock. The ESCC8 is able to synchronize onto a 8 kHz or a 2048 kHz system clock. Please refer to the PEB 24902 ESCC8 Preliminary Data Sheet for further detail on the PLL.

1.6.1 Maximum Tolerable Input Jitter on IOM-2

Figure **10** shows the maximum tolerable input jitter that is admissable on IOM-2 with respect to a BER of < 10E-7.

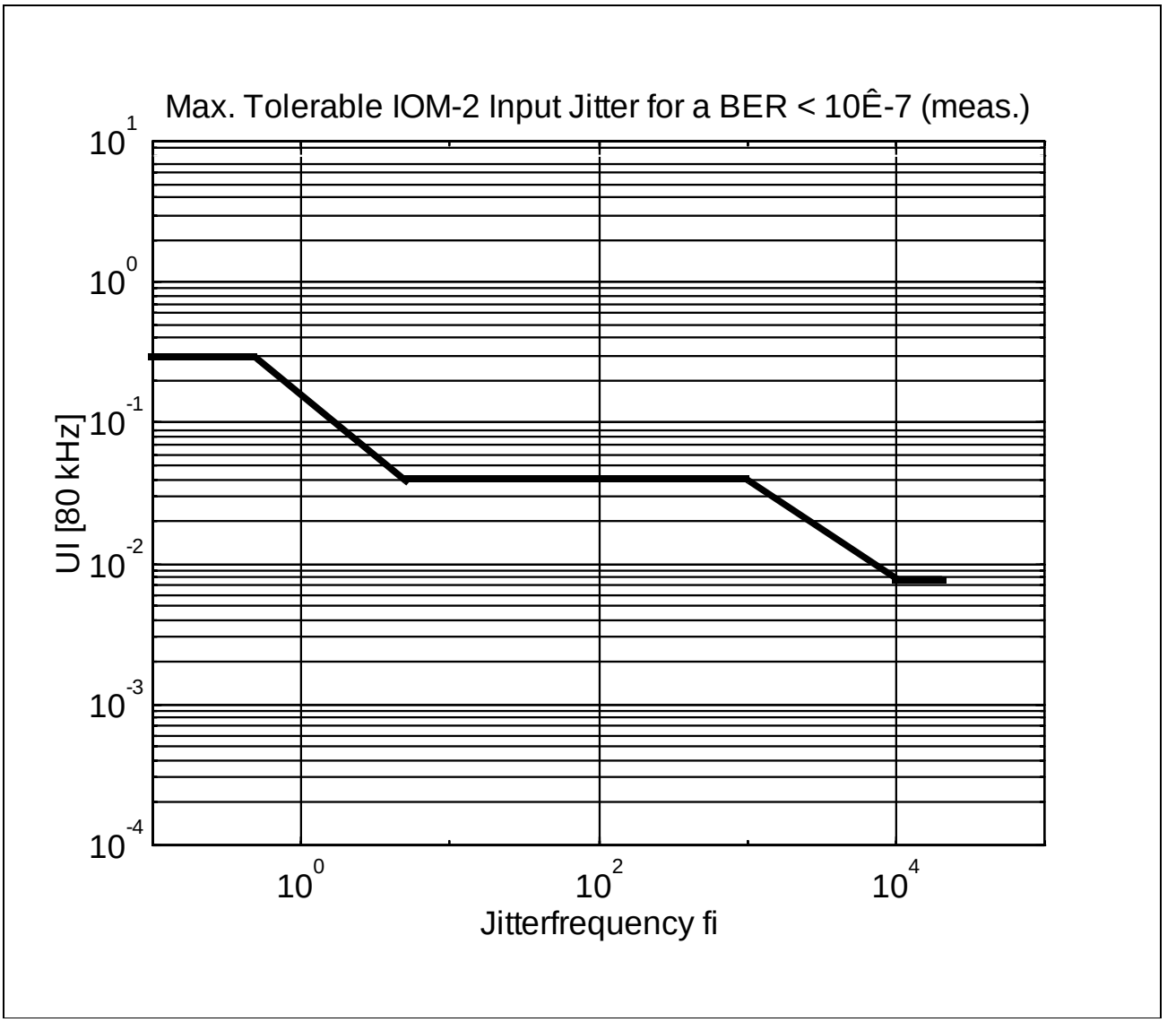


Figure 10

Max. Tolerable IOM-2 Input Jitter for a BER < 10E-7

2 Functional Description

2.1 IOM-2 System Interface

The PEB 24911 Quad IEC DFE-Q is equipped with a digital ISDN Oriented Modular (IOM-2) interface, for communication with upper layer functions, such as PEB 2075 IDEC, PEB 2055 EPIC and PEB 20550 ELIC. EPIC and ELIC represent the first switching stage towards the exchange system.

The IOM interface is a four-wire serial interface with a data clock (DCL), an 8 kHz frame synchronization clock (FSC), and one data line per direction: data downstream (DD) and data upstream (DU).

The basic channel consists of a total of 32 bits, or four octets: B1 + B2 + D (18 bits) plus 14 overhead bits for monitor and control information (activation/deactivation of OSI layer 1 and maintenance functions).

The ISDN user data rate is 144 kbit/s (B1 + B2 + D). Within one FSC period, 32 bit up to 256 bit are transmitted, corresponding to DCL frequencies ranging from 512 kHz up to to 4096 kHz.

The data is transmitted transparently synchronous and in phase in both directions over the IOM interface using time division multiplexing within the 125 µs IOM-2 interface frame. Data is transmitted at half the data clock rate (see figure **11** for the IOM-2 timing). The data clock (DCL) is a square wave signal with a duty cycle ratio of typically 1:1. Incoming data is sampled on the falling edge of the DCL-clock. The frequency is variable and can be set for values ranging from 512 kHz to 4.096 MHz.

Nominal bit rate of data (DD and DU):	256 kbit/s … 2048 kbit/s
Nominal frequency of DCL:	512 kHz … 4096 kHz
Nominal frequency of FSC:	8 kHz

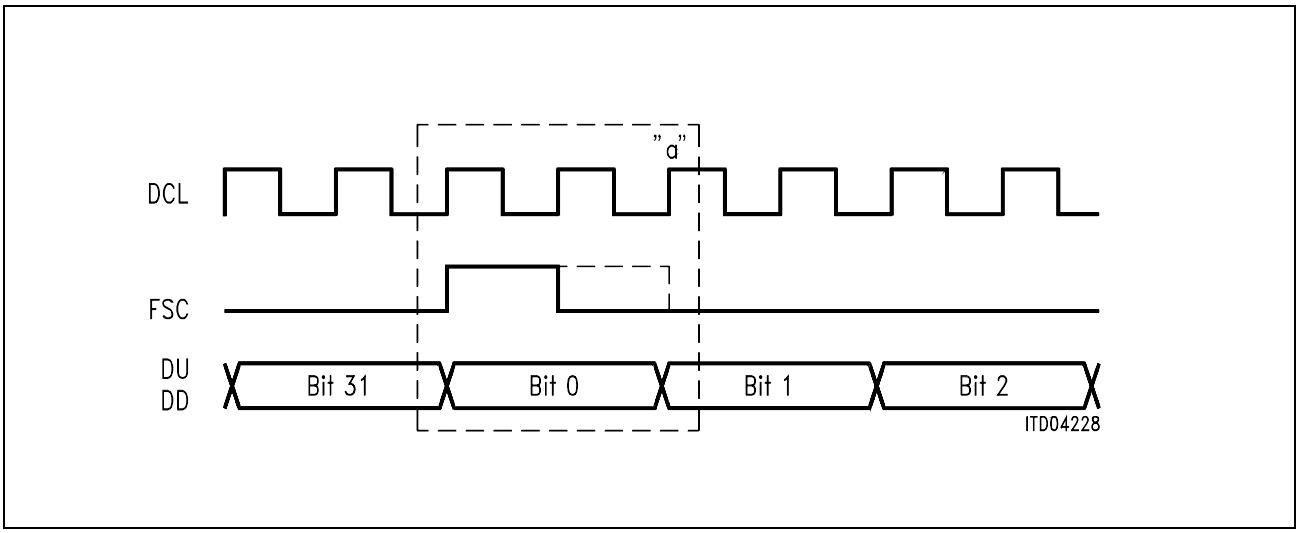


Figure 11
IOM®-2 Interface Timing (for Detail 'a' refer to Figure 52)

Figure 12 illustrates the multiplexed frame structure of the IOM-2 interface.

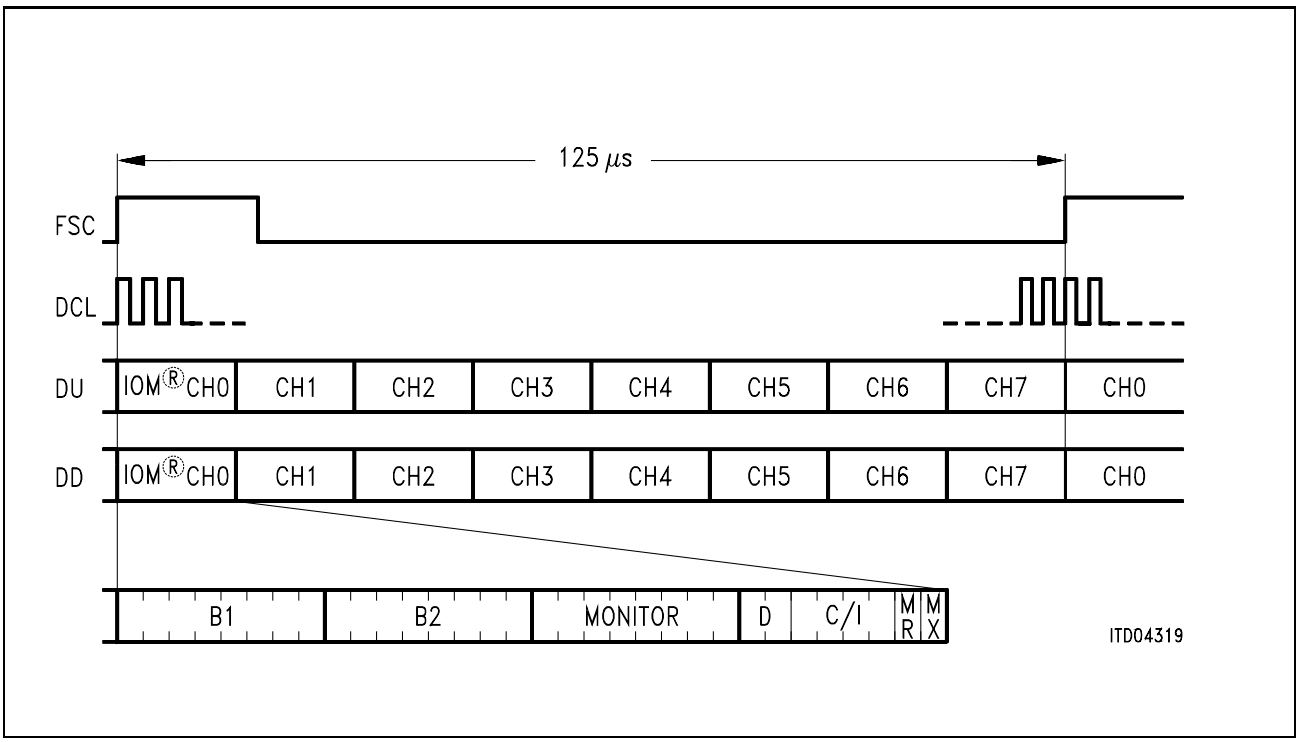


Figure 12
IOM-2 Interface

As the PEB 24911 Quad IEC DFE-Q occupies four IOM-slots, the DCL frequency must be at least 2048 KHz. The SLOT pin assigns either the IOM-slots 0 to 3 to the four

channels 0 to 3 (SLOT pin low), or it assigns the IOM-slots 4 to 7 to the channels 0 to 3 (SLOT pin high). In order to obtain synchronized transmission of either four slots in two Quad IEC DFE-Qs the DCL-Clock must be 4096 kHz.

2.1.1 Superframe Marker

It is optional to include superframe markers (lasting for one DCL-period) in every 96th “frame synchronization” signal. The remaining 95 FSC-clocks must be of at least two DCL-periods duration. If no superframe marker is to be used, all FSC high-phases need to be of at least two DCL-periods duration.

The relationship between the IOM-2-superframe marker of the slave, the U-interface, and the IOM-2-superframe marker of the master is fixed after activation of the U-interface. I.e. data inserted on LT-side in the first B1-channel after the IOM-2-slave superframe marker will always appear on the NT-side with a fixed offset, e.g. in the 5th B1-channel after the master superframe marker. After a new activation this relationship (offset) may be different.

2.1.2 IOM®-2 Command/Indicate Channel

The Control/Indicate channel (C/I-channel) is used to control the operational status of the Quad IEC DFE-Q and to issue corresponding indications. C/I-channel codes serve as the main link between the Quad IEC DFE-Q and external intelligence.

The following sections describe the operation of one single channel of the Quad IEC DFE-Q. The four channels operate completely independent.

Commands have to be applied continuously on DIN until the command is validated by the Quad IEC DFE-Q and the desired action has been initiated. Afterwards the command may be changed.

An indication is issued permanently by the Quad IEC DFE-Q on DOUT until a new indication needs to be forwarded. Because a number of states issue identical indications it is not possible to identify every state individually.

The interpretation of C/I-codes depends on the mode selected. **Table 2** shows the abbreviations used for C/I-commands and indications.

Remark:

The LTD (LT-Disable) command, which is available with the IEC-Q single channel transceiver, is no longer valid with the DFE-Q, since the DISS pin associated with the LTD command is not available with the DFE-Q. However, if a LTD command is send to the DFE-Q, it will transition unconditionally to the ’Test’ state. The receiver will not be reset.

Table 2
C/I-Abbreviations

Code	Description
AI	Activation Indication
AR	Activation Request
AR0	Activation Request with act bit = 0
ARL	Activation Request Local Loop
ARM	Activation Request Maintenance bits
ARX	Activation Request without 15 second limit
DC	Deactivation Confirmation
DR	Deactivation Request
DEAC	Deactivation Accepted
DI	Deactivation Indication
DT	Data-Through test mode
DU	Deactivation Request Upstream
EI1	Error Indication1 (error on U)
EI2	Error Indication2 (error on S/T)
EI3	Error Indication3 (timeout T1 [15sec] error on U)
FJ	Frame Jump
LSL	Loss of Signal Level on U
UAI	U-Activation Indication
UAR	U-Activation Request
RES	Reset
RES1	Reset receiver
RSY	Loss of Synchronization
PU	Power-Up
SSP	Send-Single-Pulses test mode
TIM	Timing request

Structure

4 bit wide, located at bit positions 27–30 in each time-slot.

Verification

Double last-look criterion. A new command will be recognized as valid after it has been detected in two successive IOM-frames.

Codes

Both commands and indications depend on the data direction. **Table 3** presents all defined C/I-codes. A command needs to be applied continuously until the desired action has been initiated. Indications are strictly state orientated. Refer to the state diagrams in **section 2.9** for commands and indications applicable in various states.

Table 3

Command / Indicate Codes

Code	IN	OUT
0000	DR	–
0001	RES	DEAC
0010	–	FJ
0100	RES1	RSY
0101	SSP	EI2
0110	DT	INT
0111	UAR	UAI
1000	AR	AR
1001	ARX	ARM
1010	ARL	–
1011	–	EI3
1100	–	AI
1101	AR0	LSL
1110	–	–
1111	DC	DI

AI	Activation Indication	EI3	Error Indication 3 (timeout T1 [15 s], error on U)
AR	Activation Request		
AR0	Activation Request with act bit = 0	FJ	Frame Jump [2]
ARL	Activation Request Local Loop	INT	Interrupt (set by pin “INT”)
ARM	Activation Request Maintenance bits	LSL	Loss of Signal Level on U
ARX	Activation Request without 15 sec limit	RES	Reset
DC	Deactivation Confirmation	RES1	Reset receiver
DR	Deactivation Request	RSY	Loss of Synchronization
DEAC	Deactivation Accepted	SSP	Send-Single-Pulses test mode

DI	Deactivation Indication	UAI	U-Activation Indication
DT	Data-Through test mode	UAR	U-Activation Request
EI2	Error Indication 2 (error on S/T)		

The following example illustrates the use of the C/I-channel in combination with the PEB 2055 EPIC. The device is assumed to be initialized correctly prior to starting the C/I-code transfer.

PEB 2055 and C/I-Channel Programming:

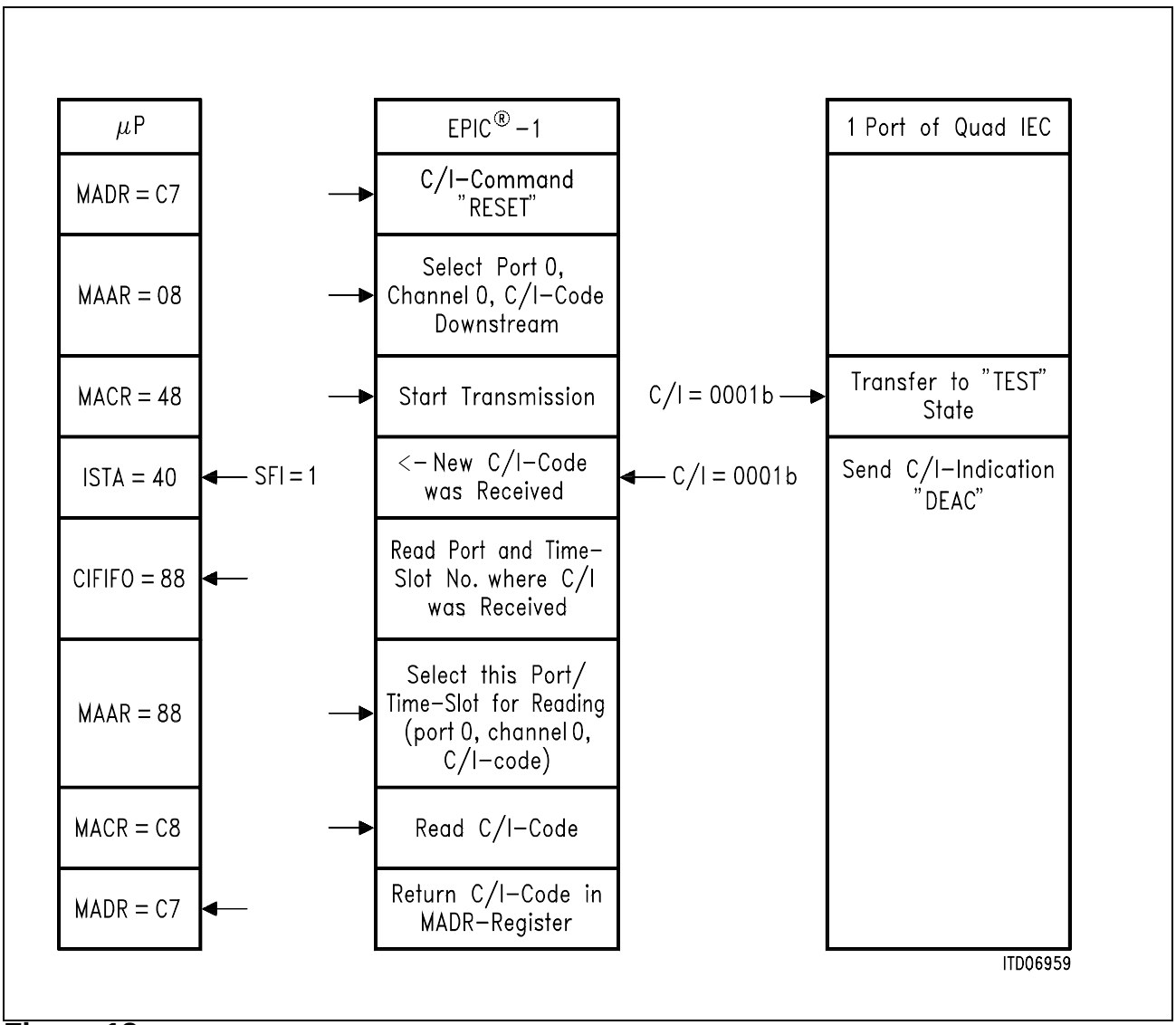


Figure 13

C/I-Channel Use with the EPIC® (all data values hexadecimal)

After the correct initialization of the EPIC, the C/I-code which is to be transmitted to the Quad IEC DFE-Q is written into the MADR-register (structure: 1 1 C/I C/I C/I C/I 1 1). With the MAAR-register the EPIC is informed where to send this C/I-code (transmission

direction, port number and time-slot number). For a description of this register please refer to the EPIC-manual, the example above sends the C/I-command to port 0, time-slot 0. MACR = 48_H starts the transmission of the command.

If a change in one of the C/I-channels was observed, an ISTA-interrupt (bit SFI) is generated. Because the user does not know in which channel the change occurred, the location needs to be read from the CIFIFO-register. This address is copied via software into address register MAAR. After having started the read operation with MACR = $C8_H$ the C/I-message can be read from MADR (structure as described earlier).

2.1.3 IOM®-2 Interface Monitor Channel

The monitor channel represents a second method of initiating and reading Quad IEC DFE-Q specific information. Features of the monitor channel are supplementary to the command/indicate channel. Unlike the command/indicate channel with an emphasis on status control, the monitor channel provides access to internal bits (maintenance, overhead) and test functions (EOC-commands, local loop-backs, block error counter and self-test).

The key characteristics of the Monitor Channel are as follows:

Modes

Auto-mode and transparent mode are available. These affect MON-0- and MON-8-messages only and will be described in the sections dealing with these monitor categories.

Structure

The structure of the monitor channel is 8 bit wide, located at bit position 17–24 in every time-slot. Monitor messages sent to the Quad IEC DFE-Q are always 2 bytes long, monitor messages returned by the Quad IEC DFE-Q are 2 or 4 bytes long depending on the command. 4 byte long return messages (internal register data) are issued via 2 messages containing 2 bytes each.

Transmission of multiple monitor bytes is specified by IOM-2 (see next section “Handshake Procedure” for details). For handshake control in multiple byte transfers, bit 31, monitor read “MR”, and bit 32, monitor transmit “MX”, of every time-slot are used.

Verification

The monitor message on DIN is considered valid only if it consists of exactly two bytes. Longer messages or single-byte messages will be discarded.

A double last-look criterion is implemented for both bytes of the monitor message. If the received bytes are not identical in the first two received frames the message will be aborted.

Codes

3 categories of monitor messages are supported by the Quad IEC DFE-Q:

– MON-0(EOC Programming)
– MON-2(Overhead Bits)
– MON-8(Local Functions)

The order of listing corresponds to the priority attributed to each category. MON-0 messages will be transmitted first, MON-8 messages last in case several messages are initiated simultaneously. The following section describes all codes of supported monitor messages

The following chapters describe the principle of monitor handshake in IOM-2, internal safe guards against blocking of the monitor channel, and features (divided into 4 categories).

2.1.3.1 Handshake Procedure

IOM-2 provides a sophisticated handshake procedure for the transfer of monitor messages. The monitor channel is full duplex and operates on a pseudo-asynchronous basis, i.e. while data transfer on the bus takes place synchronized to frame synchronization, the flow of monitor data is controlled by two bits, the MR- and MX-bits, that are assigned to each IOM-frame (on DIN and DOUT).

The monitor transmit bit (MX) indicates when a new byte has been issued in the monitor channel (active low). The transmitter postpones transmitting the next information until the correct reception has been confirmed. A correct reception will be confirmed by setting the monitor read bit (MR) to low.

Monitor data will be transmitted repeatedly until its reception is acknowledged.

Figure 14 illustrates a monitor transfer at maximum speed. The transmission of a 2-byte monitor command followed by a 2-byte Quad IEC DFE-Q-response requires a minimum of 15 IOM-2 frames (reception 7 frames + transmission 8 frames = 1.875 ms). In case the controller is able to confirm the receipt of first Quad IEC DFE-Q-response byte in the frame immediately following the MX-transition on DOUT from high to low (i.e. in frame NO. 9), 1 byte may be saved (7 frames + 7 frames).

Note: *Transmission and reception of monitor messages can be performed simultaneously by the Quad IEC DFE-Q. In the procedure depicted in* ***figure 14*** *it would be possible for the Quad IEC DFE-Q to transmitmonitor data in frames 1–5 (excluding EOM-indication) and receive monitor data from frame 8 onwards.*

M 1/2: Monitor message 1. and 2. byte
R 1/2: Monitor response 1. and 2. byte

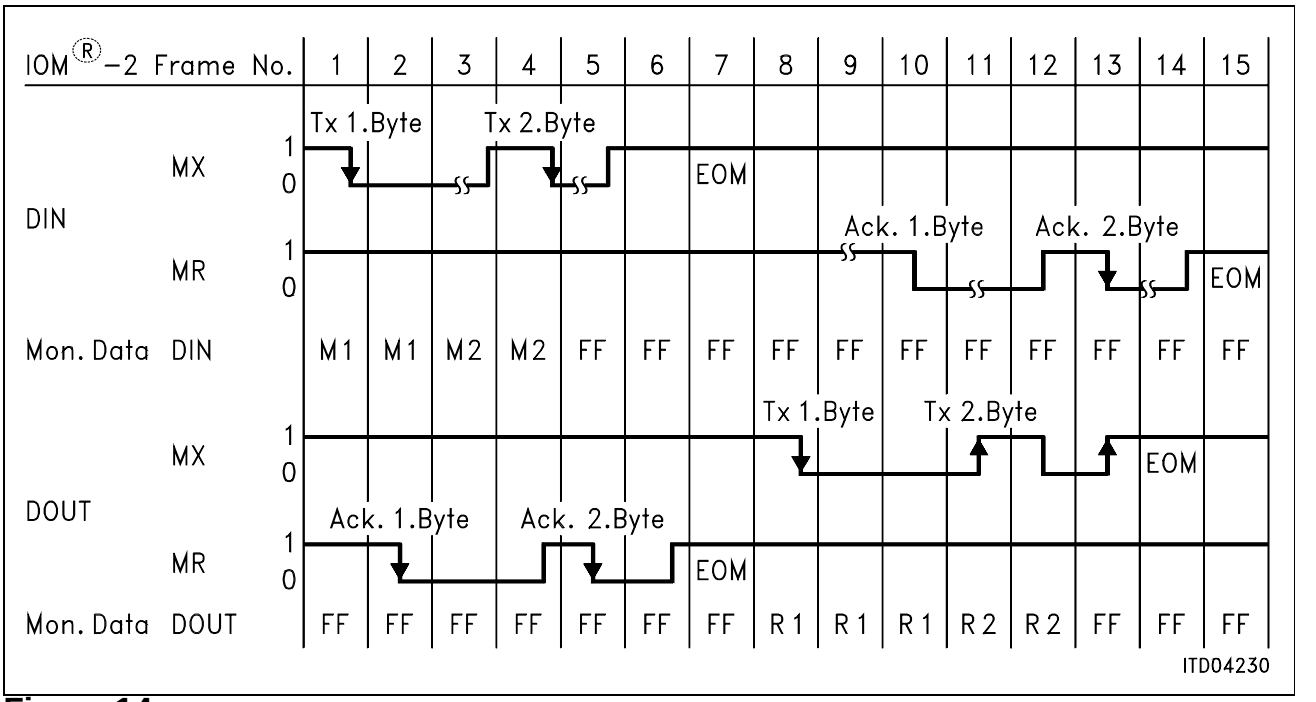


Figure 14
Handshake Protocol with a 2-Byte Monitor Message/Response

Idle State

After the bits MR and MX have been held inactive (i.e. high) for two or more successive IOM-frames, the channel is considered idle in this direction.

Standard Transmission Procedure

1. The first byte of monitor data is placed by the external controller (e.g. ICC, EPIC) on the DIN line of the Quad IEC DFE-Q and MX is activated (low; frame No. 1).
2. The Quad IEC DFE-Q reads the data of the monitor channel and acknowledges by setting the MR-bit of DOUT active if the transmitted bytes are identical in two received frames (frame No. 2 because the PEB 24911 reads and compares data already while the MX-bit is not activated).
3. The second byte of monitor data is placed by the controller on DIN and the MX-bit is set inactive for one single IOM-frame. This is performed at a time convenient to the controller.
4. The Quad IEC DFE-Q reads the new data byte in the monitor channel after the rising edge of MX has been detected. In the frame immediately following the MX-transition active-to-inactive, the MR-bit of DOUT is set inactive. The MR-transition inactive-to-active exactly one IOM-frame later is regarded as acknowledgment by the external controller (frame No. 4–5).The acknowledgment by the Quad IEC DFE-Q will always be sent two IOM-frames after the activation of a new data byte.

5. After both monitor data bytes have been transferred to the Quad IEC DFE-Q, the controller transmits “End Of Message” (EOM) by setting the MX-bit inactive for two or more IOM-frames (frame No. 5–6).
6. In the frame following the transition of the MX-bit from active to inactive, the Quad IEC DFE-Q sets the MR-bit inactive (as was the case in step 4). As it detects EOM, it keeps the MR-bit inactive (frame No. 6). The transmission of the monitor command by the controller is complete.
7. If the Quad IEC DFE-Q is requested to return an answer it will commence with the response as soon as possible. In case the “monitor time out” function is enabled it may have to postpone the answer until after the internal reset (see section Monitor Procedure Timeout for details). **Figure 14** illustrates the case where the response can be sent immediately.
   The procedure for the response is similar to that described in points 1–6 except for the transmission direction. It is assumed that the controller does not latch monitor data. For this reason one additional frame will be required for acknowledgment.
   Transmission of the 2. monitor byte will be started by the Quad IEC DFE-Q in the frame immediately following the acknowledgment of the first byte. The PEB 24911 does not delay the monitor transfer.

Transmission Abortion

If no EOM is detected after the first two monitor bytes, or received bytes are not identical in the first two received frames, transmission will be aborted through receiver by setting the MR-bit inactive for two or more IOM-2-frames. The controller reacts with EOM. This situation is illustrated in **figure 15**.

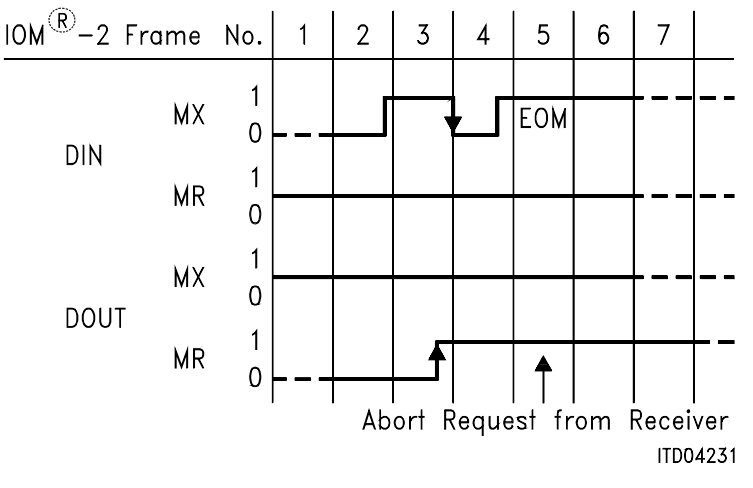


Figure 15
Abortion of Monitor Channel Transmission

Figure 16 demonstrates it with the PEB 2055 EPIC. A two-byte message is sent from the control unit to the Quad IEC DFE-Q who acknowledges the receipt by returning a two-byte long message in the monitor channel.

PEB 2055 and Monitor Channel Programming

The EPIC supports monitor transfers on a high level. Several modes are offered to support different types of monitor transfer. For communication with the Quad IEC DFE-Q, three are of special interest.

Transmit Only. This mode is required when the EPIC sends monitor messages but no confirmation is returned by the Quad IEC DFE-Q (e.g. MON8 “CCRC”).

Transmit and Receive. The EPIC transmits first and receives afterwards. Confirmations sent by the Quad IEC DFE-Q can be read (e.g. MON0 “EOC”-messages).

Searching for Active Monitor Channels. Listens to the IOM-monitor channel and reads information issued by the Quad IEC DFE-Q autonomously (e.g. MON2-messages). Nothing is transmitted by the EPIC.

The EPIC uses a FIFO for transmission and reception. The user therefore does not have to provide routines for the handshake protocol.

PEB 2055 and Monitor Channel Programming:

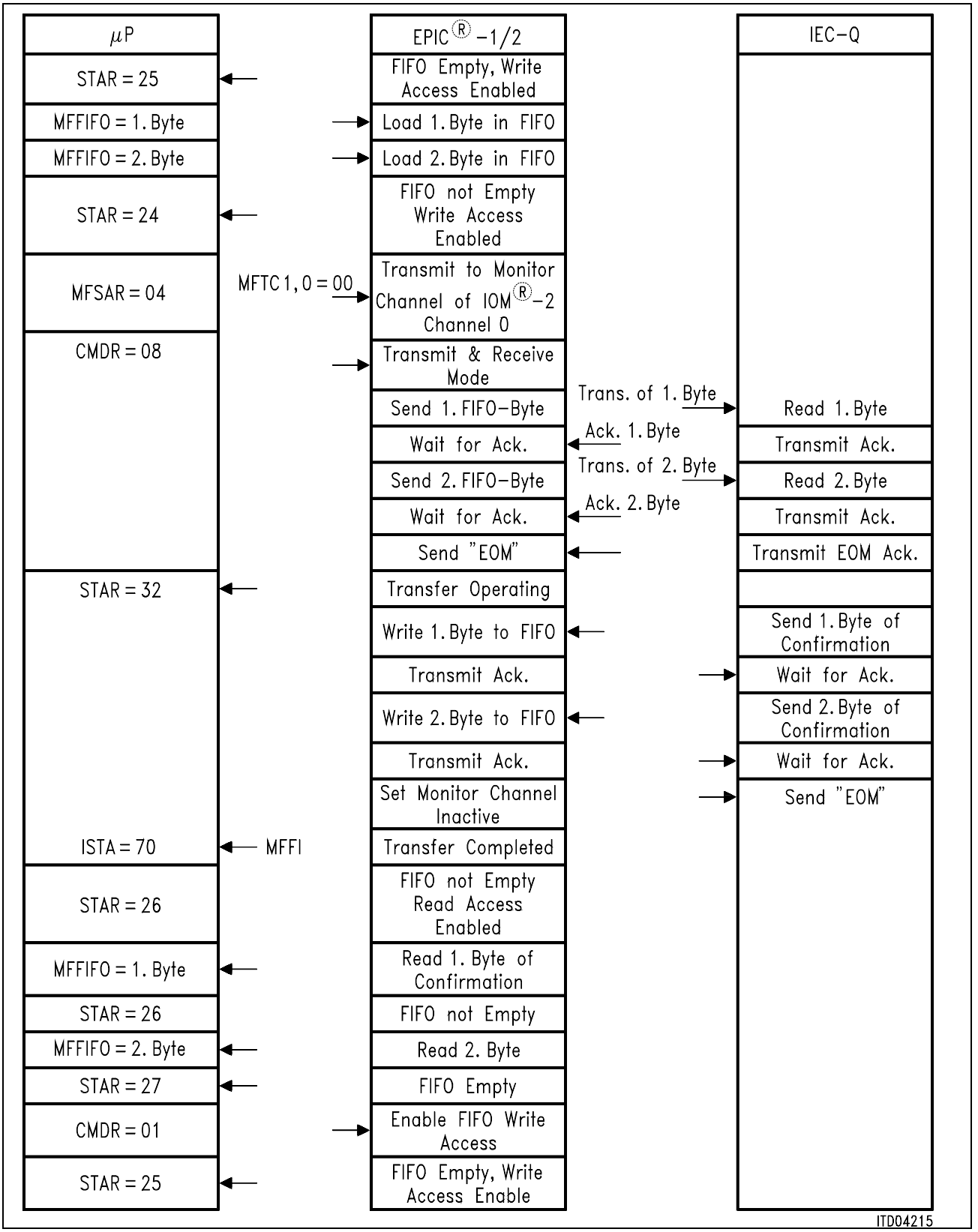


Figure 16

Monitor Channel Handling with EPIC (all data values hexadecimal)

The example of **figure 16** demonstrates the use of the EPIC in the transmit-and-receive mode.

Before programming the FIFO, it is verified that the FIFO is empty and write access is possible. All monitor data is loaded into the FIFO (two bytes), the transmission channel and mode are selected. Writing “CMDR = 08” starts transmission of the FIFO contents and enables monitor data reception. Then transmission of the first byte begins. The Quad IEC DFE-Q reacts to a low level of the MX-bit on DIN by reading and acknowledging the monitor channel byte automatically. On detection of the confirmation, the EPIC sends the next byte. After both bytes have been transmitted, the confirmation from the Quad IEC DFE-Q is read into the FIFO. After completion of the transfer an interrupt is generated. If the operation was successful, “STAR = 26” will indicate that data is loaded and the read access is enabled (in addition it is indicated that the PCM-synchronization status is correct). Following the readout of the confirmation bytes, the FIFO is cleared and the write access is selected again with the CMDR-register (“CMDR = 01”).

The handshake timing for byte transfer is handled by both devices (EPIC and Quad IEC DFE-Q) automatically.

2.1.3.2 MON-0-Command (EOC Programming)

Monitor commands supported by the PEB 24911 divide into three categories. Each category derives its name from the first nibble (4 bits) of the two byte long message. All monitor messages representing similar functions are grouped together. Commands belonging into the first category, MON-0-commands, are described in more detail in this chapter. MON-2- and MON-8-commands are discussed in the following sections.

Note: MON-1-commands as known from the PEB 2091 IEC-Q do not apply to LT mode. Therefore, they are not supported by the Quad IEC DFE-Q.

MON-0-messages are also referred to as EOC-messages (Embedded Operations Channel) because they are used to write and read the registers containing the information of the EOC-channel on the U-interface. Via the U-interface EOC-channel it is possible to exchange service of signaling information between the exchange side and the terminal side. It is important to note that MON-0-messages provide only access to the device internal EOC-registers. The insertion and extraction of a message on the U-frame is handled automatically by the EOC-processor of the device. Usage of MON-0-monitor messages therefore differs not from other MON-commands.

Nine MON-0-commands are defined and can be interpreted by the PEB 24911. MON-0-messages are issued with the highest priority, i.e. if a MON-2-, -8-message should be sent simultaneously with a MON-0 message, it is the EOC-message that will be issued first.

The structure of a MON-0-message is shown in the table below.

Table 4

MON-0-Message Structure

1. Byte		2. Byte	
0 0 0 0	A A A | 1	E E E E	E E E E
MON-0	Addr. | d/m	EOC-Code	

The following table describes the commands and messages and gives information about their use. An example illustrating the use of EOC-commands is given in **sections 2.10.1 and 2.10.2**.

Table 5

MON-0-Functions (1. Priority)

D	U	Function
LBBD		Close complete loop-back (B1, B2, D). The NT does not close the complete loop-back immediately after receipt of this code. Instead it issues the C/I-command AIL (in “Transparent” state and auto-mode) or ARL in the states “Error S/T” and “Synchronized”. This allows the downstream device to close the loop-back if desired (e.g. SBCX). If the downstream device does not close the loop a MON-8 command (LBBD) must be returned and the loop-back is closed within the PEB 24911. In addition the DISS-pin is set to (1) after reception of LBBD. This provides a possibility to perform remote power supply control.
LB1		Closes B1 loop-back in NT. All B1-channel data will be looped back within the Quad IEC DFE-Q.
LB2		Closes B2 loop-back in NT. All B2-channel data will be looped back within the Quad IEC DFE-Q.
NCC		Notify of corrupt CRC. Upon receipt of NCC the NT-block error counters (near-end only) are disabled and error indications are retained. This prevents wrong error counts while corrupted CRCs are sent (MON-8 CCRC).
RCC		Request corrupt CRC. Upon receipt the NT transmits corrupted (= inverted) CRCs upstream. This allows to test the near end block error counter on the LT-side. The far end block error counter at the NT-side is stopped and NT-error indications (MON-1) are retained.
RTN		Return to normal. With this command all previously sent EOC-commands will be released. The EOC-processor is reset to its initial state (FF_H).

Table 5

MON-0-Functions (1. Priority)

D	U	Function
H	H	Hold. Provokes no change. It may be used as a preliminary message in configurations where the acknowledgment is delayed. E.g. in a repeater configuration the NT-RP could answer with H while the EOC-acknowledgment is passed upstream. Thereby it can be avoided that the LT-control unit misinterprets the delayed ACK as a malfunction. The device issues Hold if no NT or broadcast address is used or if the d/m indicator is set to (0).
	UTC	Unable to comply. Message sent instead of an acknowledgment if an undefined EOC-command was received by the NT.
	ACK	Acknowledge. If a defined and correctly addressed EOC-command was received by the NT, the NT replies by echoing back the received command.

Auto-Mode/Transparent Mode

The use of the EOC-channel depends upon the operational mode of the Quad IEC DFE-Q and the EOC-processing mode. The user may choose between auto- and transparent mode.

It is recommended to use the transparent mode in LT-PBX mode where synchronization of cordless basestations is performed via the EOC channel.

In auto-mode all received commands will be acknowledged (NT-PBX only). If addressed correctly (000b = NT or 111b = broadcast) the NT will initiate the requested action automatically. Only EOC-messages that differ from the previously received message will be passed on to the IOM-2 interface.

In transparent mode no acknowledge and execution of requested actions is performed. A monitor message containing the most recently received command will be issued twice per superframe (every 6 ms) independently of whether the command has changed or not.

Because in both transparent and auto-mode all received EOC-commands are passed on to the IOM-2 interface via MON-0 messages, the EOC-channel may be used to transmit signaling information with user defined commands. Refer to **section 2.7** and ANSI for restrictions on user defined codes.

For a quick reference the key characteristics of the MON-0 commands are summarized on the following pages.

Function

The MON-0-commands provide access to device internal EOC-registers. Via MON-0 the EOC overhead bits of the U-interface are controlled. This access is only possible in states where the PEB 24911 transmits superframe indications (ISW). This is the case in the following states:

EC-Converged
EQ-Training
Line Active
Pend. Transparent
Transparent
S/T Deactivated

In other states the EOC-processor clamps all EOC-maintenance bits to high when EOC-bits are transmitted.

MON-0-commands may be passed at any instant and need to be transferred only once (applicable for auto- and transparent mode). Code repetition is performed within the chip by the EOC-processor.

Latching

In NT-automode all detected EOC-commands on U are latched, i.e. they are valid as long as they are not explicitly disabled with the EOC “RTN” command or a deactivation.

In transparent mode no processing and latching is performed by the chip.

Priority

MON-0-monitor messages have the highest priority of the four MON-categories available.

Modes

Auto- and transparent modes are available.

Auto-Mode

In auto-mode the “return message” reception is enabled after an EOC-command has been transmitted downstream. The activation of this function causes the Quad IEC DFE-Q to watch the EOC-channel of the U-interface and to issue a MON-0-message after an identical EOC-message has been received during three consecutive frames. Thus in auto-mode an acknowledgment of the MON-0-command is even possible if the new message is not different from the previous one.

If no MON-0-command has been transmitted downstream, a MON-0-message is issued only after the “triple-last-look” criterion is fulfilled and if this message is different from the one previously accepted (triple last look). New messages will be passed to IOM- independently of the address used, i.e. not only messages addressed with (000) or (111) but all received EOC-messages will be transmitted with MON-0-messages.

Transparent Mode

In transparent mode every 6 ms a MON-0-message containing the last received EOC-message is issued on the IOM-bus. This occurs even if no change occurred in the EOC-channel. No ’triple-last-look’ is performed before a MON-0-message is sent.

Codes

Table 6

Format of MON-0-Commands

1. Byte		2. Byte	
0 0 0 0	A A A | 1	E E E E	E E E E
MON-0	Addr. | d/m	EOC Code	

Addr: Address
– 0 = NT
– 1 … 6 = Repeater
– 7 = Broadcast

d/m: Data/Message
– 0 = Data
– 1 = Message

E: EOC Code
– 00 … FF_H = coded EOC command/indication

The following EOC-commands will be acknowledged and executed automatically in NT auto-mode if addressed correctly. The acknowledgment will be two bytes long. The first

byte indicates that a MON-0-acknowledgment is transmitted, the second byte contains the message.

Table 7

MON-0 EOC-Channel Commands and Indications

MON-0-Functions (1. Priority)			
Code Hex.	**D**	**U**	**Function**
00	H	H	Hold
50	LBBD		Close complete loop
51	LB1		Close loop B1
52	LB2		Close loop B2
53	RCC		Request corrupt CRC
54	NCC		Notify of corrupt CRC
AA		UTC	Unable to comply
FF	RTN		Return to normal
XX		ACK	Acknowledge

2.1.3.3 MON-2-Commands (Overhead Bits)

MON-2-indications are used to transfer all overhead bits except those representing EOC- and CRC-bits. Starting with the ACT-bit, the order is identical to the position of the bits at the U-interface.

The first MON-2-message is issued immediately after reaching “Line Active” state. Thereby the control system is informed about the initial U-interface status after a successful activation.

Later MON-2-messages will only be sent if a change of system status has occurred. No MON-2-messages are issued while CRC-violations are detected (refer to **section 2.7.2.2** for verification algorithm). This prevents the system of being overloaded by faulty monitor indications.

Table 8

MON-2 Command Structure

1. Byte		2. Byte
0 0 1 0	M41 M51 M61 M42	M52 M62 M43 M44 M45 M46 M47 M48
MON-2	Overhead Bits	Overhead Bits

The meaning of bits M41-M48 depends upon the transmission direction (LT –> NT or NT –> LT) and the mode.

The overhead bits are grouped by the three control mechanisms responsible for setting and resetting the bits.

Control via Quad IEC DFE-Q:

– ACT (Activation bit) The ACT-bit is part of the start-up sequence and is used to indicate layer 2 to be ready for communication. In this case it is set to (1).

– DEA (Deactivation bit) The DEA-bit is used by the network side during deactivation. By setting DEA to (0), the network informs the NT of its intention to turn-off.

– CSO (Cold Start Only) The CSO-bit signals the network side whether the NT is only capable of being started via cold start. If the NT may be activated with a cold start procedure only, the CSO-bit is set to (1).

– UOA (Partial Activation) The UOA-bit is used by the network side to inform the NT that only the U-interface shall be activated (S-interface remains deactivated according to CNET-specification). If the UOA-bit is set to (0), only the U-interface will be activated.

– SAI (S Activity Indicator) The SAI-bit informs the LT-side about the state of the S-interface. With the S-interface deactivated (i.e. C/I-commands TIM or DI received), the SAI-bit is set to (0). Additionally the SAI-bit is used (with SAI = (1)) in a terminal initiated activation (when before only U was activated) to request complete NT-activation.

– FEBE (Far-End Block Error) The FEBE-bit is used to inform the opposite U-interface station that the transmitted data could not be received free of errors. The device sets the FEBE-bit to (0) if errors were observed. Each time a FEBE = (0) is detected, the count of the internal far-end block error counter will be incremented. Additionally it is possible to control the FEBE-

Control via MON-Commands:

– FEBE (Far-End Block Error) Quad IEC DFE-Q controlled commands. Additionally it is possible to set the FEBE bit to (0) for one single U-superframe with the MON-8 message “SFB”.

For a quick reference the key characteristics of the MON-2 commands are summarized on the following pages.

Function

The MON-2-structure is used to transfer all maintenance bits except EOC- and CRC-information. These 12 overhead bits are passed in the same order as defined for the U-interface. The first bit after the address bit corresponds to the “ACT” bit, bit D0 from the second byte is user defined.

Latching

– Transmission on U (data from DIN):– latched
– Reception from U (data on DOUT):– non-latched

Priority

MON-2-monitor messages have the second highest priority of the three MON-categories available.

Modes

The operation of MON-2-indications is identical in auto- and transparent modes. Via the MON-8 “PACE” command bit D1, SAI/UOA, can be controlled with a MON-2-command.

In repeater modes all overhead bits are controlled with MON-2-commands.

Codes

Table 9

Format of MON-2-Messages

1. Byte		2. Byte
0 0 1 0	D_{11} D_{10} D_9 D_8	D_7 D_6 D_5 D_4 D_3 D_2 D_1 D_0
MON-2	Overhead Bits	Overhead Bits

D0 … 11: Overhead bits

These bit positions in the MON-2-message correspond to the following overhead bits:

Table 10
MON-2 and Overhead Bits

Position MON-2/U	NT –> LT		LT –> NT		Repeater (LT / NT)	
	Bit	Control	Bit	Control	Bit	Control
D11/M41	ACT	DFE-Q	ACT	IEC-Q	ACT	MON-2
D10/M51	1	MON-2	1	MON-2	1	MON-2
D9/M61	1	MON-2	1	MON-2	1	MON-2
D8/M42	PS1	Pin 21 (NT)	DEA	IEC-Q	PS1/ DEA	MON-2
D7/M52	1	MON-2	1	MON-2	1	MON-2
D6/M62	FEBE	DFE-Q	FEBE	IEC-Q	FEBE	MON-2
D5/M43	PS2	Pin 22 (NT)	1	MON-2	PS2/1	MON-2
D4/M44	NTM	MON-1 (NT)	1	MON-2	NTM/1	MON-2
D3/M45	CSO	DFE-Q	1	MON-2	CSO/1	MON-2
D2/M46	1	MON-2	1	MON-2	1	MON-2
D1/M47	SAI	DFE-Q/ MON-2	UOA	IEC-Q/ MON-2	SAI/ UOA	MON-2
D0/M48	1	MON-2	1	MON-2	1	MON-2

Control via Quad IEC DFE-Q

– ACT (Activation bit). ACT = (1) –> Layer 2 ready for communication
– DEA (Deactivation bit). DEA = (0) –> LT informs NT that it will turn off
– CSO (Cold Start Only). CSO = (1) –> NT-activation with cold start only

– UOA (U-Only Activation).	UOA = (0) –> U-activation only
– SAI (S Activity Indicator).	SAI = (0) –> S-interface is deactivated
– FEBE (Far-end Block Error).	FEBE = (0) –> Far-end block error occurred

Transmission on U-Interface

– In the transmit direction (on DIN), only the undefined bits market with binary “1” may be controlled by making use of a MON-2-message.
– All overhead bits are set to binary “1” when leaving a power-down state. No further processing is performed by the Quad IEC DFE-Q.

Reception on U-Interface

– In the receive direction (on DOUT), the overhead bits of the last two U-interface superframes are compared and a MON-2-message defining all 12 bits is issued if a difference between both was found on at least one single bit other than the “FEBE” bit. Therefore a MON-2-message is sent not more often than once per superframe (12 ms interval).
– In order to notify the controller of the initial system status, one MON-2-message is issued immediately after reaching the “Line Active” state.

2.1.3.4 MON-8 Commands (Local Functions)

Local functions are controlled via MON-8-commands. MON-8-commands have the lowest priority. The following tables give an overview of structure and features of commands belonging to this category.

Table 11
MON-8 Command Structure

1. Byte		2. Byte
1 0 0 0	r | 0 0 0/1	D7 D6 D5 D4 D3 D2 D1 D0
MON-8	Register Addr.	Local Command (Msg./Data)

Table 12

MON-8-Functions (4. Priority)

LT		Function
D	**U**	**Local Commands**
PACE		Partial Activation Control External. With the PACE-command issued at the NT-side, the Quad IEC DFE-Q will ignore the actual status of the received UOA-bit and behave as if the UOA-bit is set to (1). If issued at LT-side, the actual status of the SAI-bit is ignored and the device works as if SAI = (1) is received. After issuing PACE the UOA/SAI-bits can be controlled by MON-2-commands.
PACA		Partial Activation Control Automatic. PACA enables the device to interpret and control the UOA- and SAI-bits automatically (NT- and LT-side respectively). Partial activation and deactivation in NT-PBX mode is therefore possible. The Quad IEC DFE-Q is automatically reset into this mode in the states “Test”, “Receive Reset” and “Tear Down”.
CCRC		Corrupt CRC. This command causes the device to send inverted (i.e. corrupted) CRCs. Corrupted CRCs are used to test block error counters (see section 2.10.2).
NORM		Return to Normal. The NORM-command resets the device into its default mode, i.e. loops are resolved and corrupted CRCs are stopped. In NT-mode it is only used in transparent mode.
RBEN		Read Near-End Block Error Counter. The value of the near-end block error counter is returned and the counter is reset to zero. The maximum value is $FF_{H.}$
RBEF		Read Far-End Block Error Counter. The value of the far-end block error counter is returned and the counter is reset to zero. The maximum value is $FF_{H.}$
	ABEC	Answer Block Error Counter. The value of the requested block error counter is returned (8 bit).
SETD		Set status of D-pins. Four driver pins can be set to either low or high.
RST		Read Status pins. The logic state of two Status pins is requested
	AST	Answer Status pins. Answer to command RST. Also issued without request on change of either one of the ST pins
RPDU		Read Propagation Delay on U-interface
	APDU	Answer propagation delay on U-interface
BSYN		Synchronize base stations. Only in LT-PBX mode. Issues EOC-message "25h" after falling edge on LT-pin
RID		Read Identification. Request for device identification.
	AID	Answer identification. The IEC Quad DFE will reply with the ID $8004_{H.}$

Table 12
MON-8-Functions (4. Priority)

LT		Function
D	U	Local Commands
SFB		Set FEBE Bit to 0

For a quick reference the key characteristics of the MON-8 commands are summarized on the following pages.

Function

MON-8-commands are used to implement local functions like reading coefficients and block error counters as well as for controlling the power controller interface and test functions.

MON-8-commands may be passed at any time and need to be transferred only once.

Latching

Latched commands must be disabled explicitly with the “NORM” command.

– internal transfer commands (RCOE, RBEN/F, RPFC, WCI, RCI, RID)– non latching
– test and activation control commands (PACE, PACA, CCRC, LB1/2, LBBD)– latching

Priority

MON-8-indications have the lowest priority of the three MON-categories available.

Code

Table 13
Format of MON-8-Messages

1. Byte		2. Byte
1 0 0 0	r | 0 0 ls	D_7 D_6 D_5 D_4 D_3 D_2 D_1 D_0
MON-8	Register Addr.	Local Command (Message/Data)

r:	Register address	– 0 = local function register – 1 = internal register
ls:	Least significant bit	depends on the command (refer to **table 14**)
$D_{0...7}$	Local command	– 00 … FF_H = local function code – 00 … FF_H = internal register address

The following local commands are defined. If a response is expected, it will comprise 4 bytes (2 messages a 2 bytes) if the value of an internal coefficient is returned, and 2 bytes in all other cases.

In a two-byte response the first byte will indicate that a MON-8 answer is transmitted, the second byte contains the requested information. This procedure is repeated for a four-byte transfer (MON-8, Info 1, MON-8, Info 2).

Table 14

MON-8-Local Function Commands

1.Byte	2.Byte	MON-8-Functions (4. Priority)		
r ls	Code (Bin)	D	U	Function
1000 0 00 0	1011 1110	PACE		Partial Activation Control External
1000 0 00 0	1011 1111	PACA		Partial Activation Control Automatic
1000 0 00 0	1111 0000	CCRC		Corrupt CRC
1000 0 00 0	1111 1111	NORM		Return to Normal
1000 0 00 0	1111 1011	RBEN		Read Near-end Block Error Counter
1000 0 00 0	1111 1010	RBEF		Read Far-end Block Error Counter
1000 0 00 0	r r r r r r r r		ABEC	Answer Block Error Counter
1000 0 00 1	0111 DCBA	SETD		Set status of D-pins D, C, B, A
1000 0 00 1	0000 0000	RST		Read Status pins
1000 0 00 1	XXXX XXS_1S_0		AST	Answer Status pins S_1, S_0
1000 0 00 1	1000 0000	RPDU		Read Propagation Delay on U-Interface

1000 1 aa a	aaaa aaaa		APDU	Answer Propagation Delay on U-Interface
1000 0 00 1	0010 0101	BSYN		Synchronize base stations
1000 0 00 0	0000 0000	RID		Read Identification
1000 0 00 0	0000 0100		AID	Answer Identification. The Quad IEC DFE-Q will reply with the ID 8004_H
1000 0 00 0	1111 1001	SFB		Set FEBE-Bit to (0)
1000 1 00 0	cccc cccc	RCOEF		Read Coefficient
1000 1 00 0 1000 1 10 0	bbbb bbbb bbbb bbbb		DCOEF	Data Coefficients, 2 bytes Data bits $D_{0 \ldots 7}$, 1. byte Data bits $D_{8 \ldots 15}$, 2. byte

Notes: *a … apropagation delay value*
b … binternal coefficient value
c … cinternal coefficient address
r … rresult from block error counter

2.2 Interface to the Analog Front End

The interface to the PEB 24902 ESCC8 is a serial interface at the pins SDX and SDR. On SDX and SDR transmit and receive data is exchanged as well as control information for the start-up procedure. The ADC output from the ESCC8 is transferred to the Quad IEC DFE-Q on the signals PDM0..PDM3. The timing of all signals is based on the 15.36 MHz clock which is provided by the ESCC8.

The transmit data, powerup/down, range function and analog loopback are transferred on SDX, and the level status on SDR for all line ports. Eight time slots contain the data for up to eight line ports. The Quad IEC DFE-Q uses four of them. Table **15** shows the assignment of the IOM-2 channels to the time-slots on SDX/SDR and the assignment of the time-slots to the line ports.

Table 15
Assignments of IOM Channels to Time-Slots on SDX/SDR and Line Ports

IOM-2 Channel No.	Time-Slot No.	Line Port No.
0/4	1	0
1/5	3	1
2/6	5	2
3/7	7	3

The allocation of these time slots is done by the nineth time slot, a 24 bit synch. word on SDX, that consists of all ZEROs. The other time slots with transmission data start with a ONE. Therefore the first ONE after 24 subsequent ZEROs is the first bit of time slot no. 0. This information is also used to determine the status of synchronisation of the digital interface after reset.

Cross-references:
2.1 **Commands in Different MON-Categories**
2.1.3.4 **MON-8-Codes**
2.7 **Overhead Bits on U-Interface**
2.8 **Control Procedures Involving UOA/SAI**

2.2.1 Frame structure

The 192 available bits during a 80 kHz period (related to the 15.36 MHz clock) are divided into the 9 slots of which 8 slots are 21 bits long used for data transmission. The status on SDR is synchronized to SDX. Each time slot on SDR carries the corresponding LD bit during the last 20 bits of the slot.

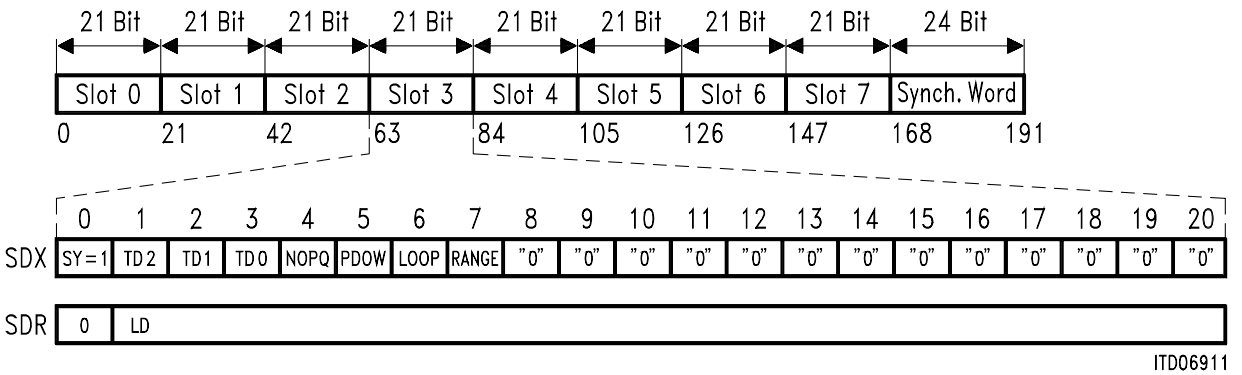


Figure 17
Frame Structure on SDX and SDR

The data on SDX is transmitted from the Quad IEC DFE-Q to the ESCC8:

NOPQ: The no-operation-bit is set to ZERO if none of the control bits (PDOW, RANGE and LOOP) shall be changed. The control bits on SDX then are set to ZERO to reduce digital cross-talk to the analog signals. The values of the control bits of the assigned line port are latched by the ESCC8.

The NOPQ bit is set to ONE if at least one of the control bits shall be changed. In this case all control bits are transmitted with their current values.

PDOW: If the PDOW bit is set to ONE, the assigned line port is switched to power down otherwise it is switched to power up.

RANGE: RANGE = ONE activates the range function of the ESCC8, otherwise the range function is deactivated. "Range function activated" refers to high input levels as they occur at short loop lengths.

LOOP: LOOP = ONE activates the loop function of the ESCC8, i.e. the analog loop is closed. Otherwise the line port of the ESCC8 is in normal operation.

SY: First bit of the time slots with transmission data. For synchronisation and bit allocation on SDX and SDR, SY is set to ONE.

"0": reserved bit. Reserved bits are currently not defined and set to ZERO. Some of these bits may be used for test purposes or can be assigned a function in later versions.

The data on SDR is transmitted from the ESCC8 to the Quad IEC DFE-Q:

LD: The input signal at the U-interface is evaluated by the Quad IEC AFE. If the signal amplitude reaches the wake-up level, the LD bit toggles with the signal frequency. If the signal at the U-interface is below the wake-up level, the LD-bit is tied at either low or high.

The 2B1Q data is coded with the bits TD2, TD1, TD0. The ESCC8 will transmit the quarternary pulses according to the following table:

Table 16
Coding of the 2B1Q data

2B1Q Data	TD2	TD1	TD0
0	1	don´t care	don´t care
– 3	0	0	0
– 1	0	0	1
+ 3	0	1	0
+ 1	0	1	1

2.3 Driver Pins

Each channel has access to four Driver output pins. The logic state of all Driver outputs belonging to one channel is set with a MON-8 command. The MON-8 command SETD, given in the IOM-2 time slot assigned to channel *i* sets the state of the pins DiA, DiB, DiC, and DiD as given by the bits of the last nibble of the command.

The state of the Driver pins is not affected by any software reset. The state of all four pins on all four channels after hardware reset is „low“.

Cross-reference: **Table 14 MON-8-Local Function Commands**

2.4 Reading Status Pins

Each channel owns two status pins, who’s logical value is reported in the Monitor channel. The status of the pins ST00 and ST01 is issued as MON-8 message AST in the Monitor channel of channel 0. The pins ST10 and ST 11 report to channel 1, the pins ST 20 and ST 21 report to channel 2 and the pins ST30 and ST 31 report to channel 3. Any change at one of the two pins causes a Monitor message to be issued automatically giving the state of both status pins. Additionally, the Quad IEC DFE-Q will issue the state of the two pins by the same Monitor message upon request with the command RST. The STxy pins have to be tied to either VDD or GND, if not used.

Note that changes of the status information occurring within a period of less than 10 IOM-2 frames might be discarded.

Cross-reference: **Table 14 MON-8-Local Function Commands**

2.5 PBX Application

This section describes special issues for D-Channel arbitration together with the PEB 20550 ELIC and for the synchronization of cordless base stations using the DECT standard. Figure **6** presents a PBX linecard with different line interfaces. All digital line interface transceivers behave compatibly.

2.5.1 D-Channel Arbitration

In order to facilitate the simultaneous serving of multiple D-channels with one HDLC-controller, e. g. using the ELIC, the PEB 24911 uses the EOC-Channel of the Uko interface to forward the stop/go information to the terminal. A 6 ms cycle time is possible. As there is no bit in the U-interface frame structure reserved for this application, the EOC-channel is used to transmit the information. The function is as follows:

In LT-PBX-Mode, a C/I-command 1000b (AR) triggers the transmission of the associated EOC message 27_H to the NT side in the next available half superframe. This will only be done once. The PEB 2091 IEC-Q V5.1 translates this message into a continuous series of "1" on the S/G-bit of the IOM-2 channel structure indicating that the D-channel access is not provided. As soon as the C/I-code AR is switched to the C/I-code 1100b (AI), the EOC-message 25_H is sent to the NT-side and the S/G-bit will be set to "0" indicating access permission to the D-channel. Figure 18 illustrates the relation of C/I-code at DIN of the LT-side and the S/G-bit at the NT-side.

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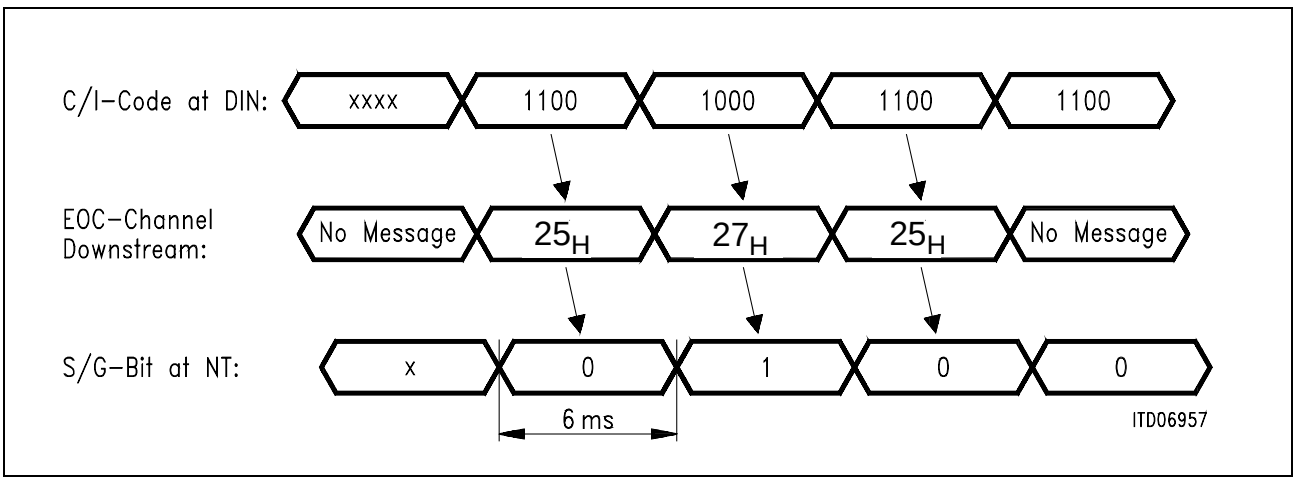


Figure 18
Passing D-channel arbitration to the Terminal via the EOC channel

This behavior is compatible to the operation of the PEB2096 OCTAT-P, except the fact, that the OCTAT-P can set the S/G bit in 0.5ms intervals and the Quad IEC DFE-Q only in 6 ms intervals. Note however, that the PEB 2091 IEC-Q v5.1 at the NT side provides a method to safely assign the HDLC-controller to the terminal before it actually sends the

HDLC-frame to the line module. Hence, complete D-channel arbitration is provided. Refer to the PEB 2091 IEC-Q Delta Sheet for version 5.1 for a detailed description.

Note that after a C/I code 1000b (AR) or 1100b(AI) has been applied the DFE-Q needs at least a period of 7 IOM-frames for further processing of the D-channel arbitration commands. During this time no Monitor commands should be issued.

If maintenance functions are to be executed, care has to be taken about the continuation of the D-Channel arbitration. Note however, that the Monitor channel and the EOC-channel are only occupied during the edges of the according C/I-command changes. Hence, there will be room for the use of the Monitor channel. An edge towards either CI 1100b or 1000b immediately will abort any Monitor command at DIN and send an abort request at DOUT.

2.5.2 Controlling DECT-basestations

The PEB 24911 provides additional features for the use together with terminals which control cordless telephones. These are

- constant propagation delay from IOM-2 to U-interface and vice versa
- synchronized transmission on all line ports connected to one IOM interface
- synchronization of DECT base stations by transmission of a sync-event via the EOC channel
- propagation delay measurement of the U transmission line

2.5.2.1 Synchronization of DECT-base stations

Similar to the D-channel arbitration procedure the DFE-Q V1.2 provides a control mechanism that allows to determine the S/G bit setting within the IOM-2 frame on the NT side. In case of DECT synchronization, the sync. process is initiated by the MON-8 command BSYN (8125_H) which enables the transmission of the snyc. pattern 25_H via the EOC channel on U. When the reception of the MON-8 message is completed and acknowleged by the MR-bit (EOM), the DFE-Q issues the associated EOC message 25_H simultaneously on all enabled channels as soon as a negative edge at the LT pin is detected (see figure **19**).

The PEB 2091 IEC-Q v5.1 - if programmed appropriately in TE mode- will interprete this EOC message such, that 4 "1" bits will appear at the S/G-bit followed by 44 "0" bits. These 48 IOM-frames constitute a period of 6 ms.

In order to get synchronized to the DECT frame care has to be taken with respect to the point of time when the BSYN command is issued. With means of a microcontroller the issue of the MON-8 message can be controlled in such a way that with the first falling edge at pin LT after a positive clock edge of the DECT Sync the EOC message 25_H is propagated to the NT side. Figure **20** illustrates the interdependency of the associated clock signals and the triggering of the appropriate MON-8/ EOC message.

Note that it has to be ensured that the Monitor channel is in idle state in downstream direction, i.e. there should be no other Monitor channel activity before the BSYN command is applied to the DFE-Q. Moreover, proper processing of the BSYN command is only guaranteed, if a recovery time of at least 8 IOM frames is met after a negative edge at the LT pin has occurred. Moreover the echo of an issued eoc= 25H command has to be received before a new eoc command may be sent

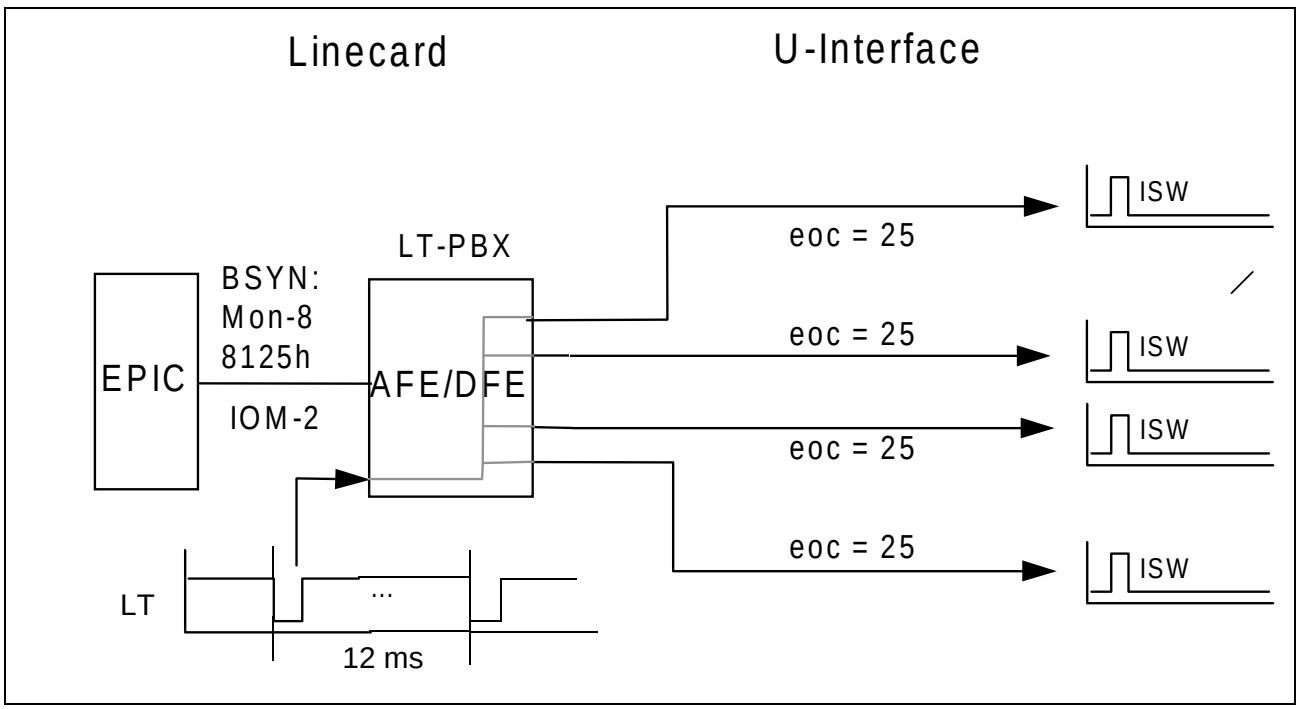


Figure 19
DECT synchronization procedure

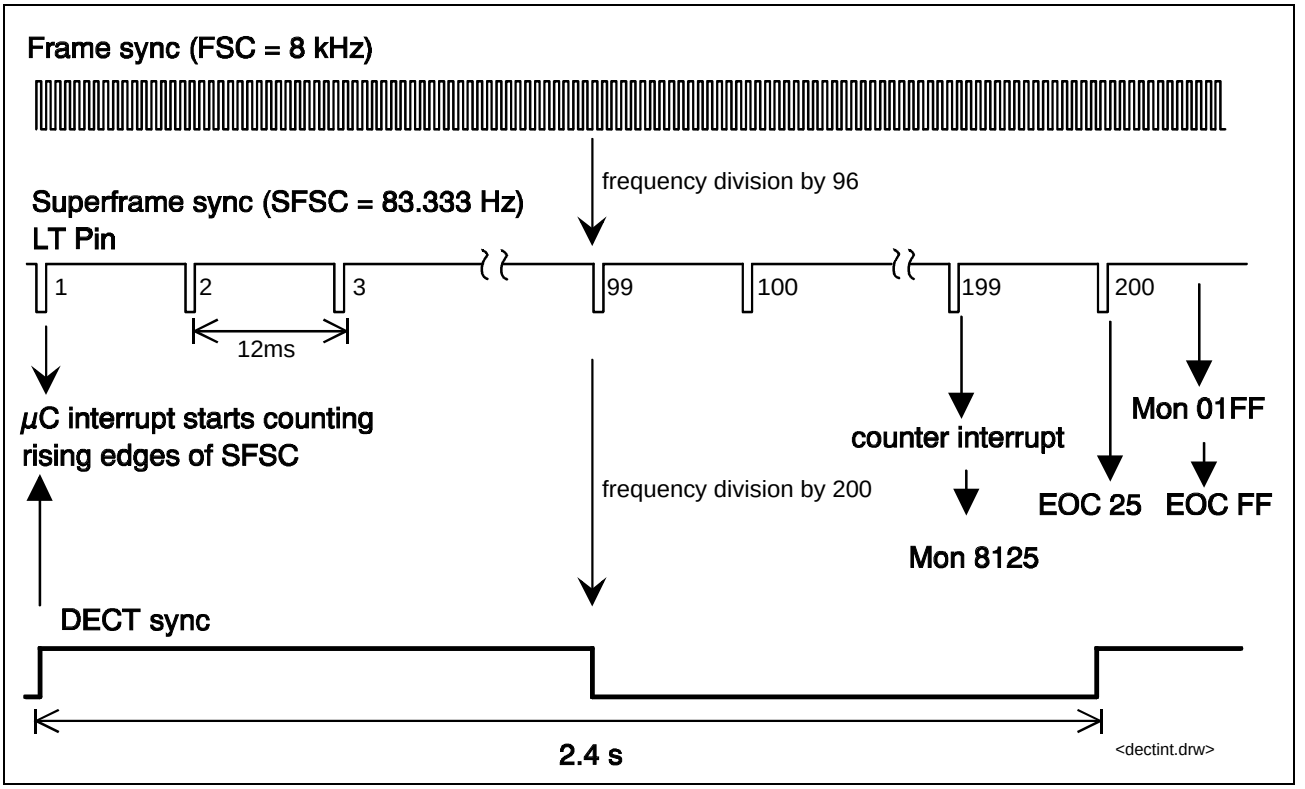


Figure 20
Synchronization of cordless basestation using the EOC-channel

2.5.2.2 Propagation delay measurement

The propagation delay can be requested with the MON-8 command RPDU (Request Propagation Delay on U) and will be issued as MON-8 Message. The propagation delay that is measured is the time between the transmission of the U-frame at the LT-side and the reception of the associated U-frame at the LT side after the data have been looped and issued by the NT-device (see figure **21**).

The propagation delay value is updated every 1.5ms (duration of 1 U basic frame) during normal operation. Transmitting it to the terminal allows to adopt an appropriate delay in the base station in order to synchronize signal flow on the air interface.

The Monitor message giving the delay is of the format 1000 $1z_{10}z_9z_8\ z_7$ .. z_0. Bits z_{10} to z_0 give the binary coded roundtrip delay in 260ns resolution.

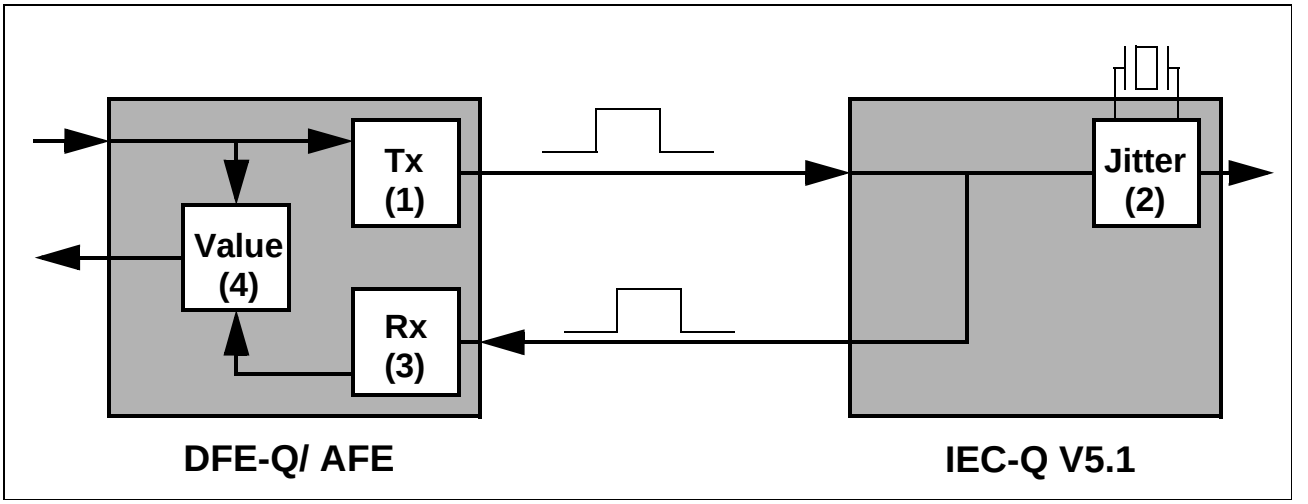


Figure 21
Propagation delay measurement from LT to NT

For further information about the conversion of the binary result in microseconds and information about tolerances (1,2,3,4 in figure Figure 21) that have to be considered please refer to the application note „A Dedicated Chip Set Features Synchronization of DECT Basestations Interfacing the U-Reference Point“.

The measurement is possible while the Quad IEC DFE-Q state machine is in the transparent states. That is, during transmission of data, the measurement can be repeated to cope with delay variations which may occur due to a temperature shift of the line.

2.6 Reset

There are two different ways to apply a reset,

– either as a hardware reset by setting pin RESQ to low
– or as a software reset via the ' C/I= RES' command

Hardware Reset

A hardware reset affects all four line ports and is executed in the following way:

As long as no DCL clock is applied, the reset impulse is stored. Triggered by the first DCL clock edge the hardware reset is then carried out and lasts for max. 4 IOM frames after the RESQ signal has been deactivated again.

With respect to the interface to the Analog Front End, to the driver output pins and to the propagation delay measurement function. However, the hardware reset takes effect immediately and is not controlled by the DCL clock.

Software Reset

A software reset has only effect on the addressed line port and the corresponding status pins. Therefore status changes will be lost during a SW reset. The remaining line ports, the interface to the Analog Front End, the driver output pins and the propagation delay measurement logic are not affected.

Power-on-Reset

When applying power to the Quad DFE-Q V1.2 an internal power-on-reset sets the device in an initial state. A reset pulse is generated, if V_{DD} raises above the POR threshold (see table **17** for the POR threshold).

Starting **from a V_{DD} voltage of below 50mV** the DFE-Q V1.2 behaves during power-up as version 1.1. In this case a power-on-reset is generated for any rising V_{DD} slopes minor than 5V/2ns. The POR function is enabled again as soon as V_{DD} drops below 50mV (see table **17**).

Table 17

Parameters for POR activation (starting from below 50mV)

Parameter	Limit Values			Unit
	min.	typ.	max.	
Maximum V_{DD} slope			5V/2ns	
POR enable threshold	50			mV

Even if the supply voltage starts **from a V_{DD} voltage of above 50mV and below 1.0V** the DFE-Q V1.2 guarantees now proper POR function but with the restriction that the rising V_{DD} slope has to be minor 5V/4µs.
With these initial parameters the POR function is enabled again if the supply voltage V_{DD} drops below 1.0V for a minimum period of 80ns (see figure **22** and table **18**).

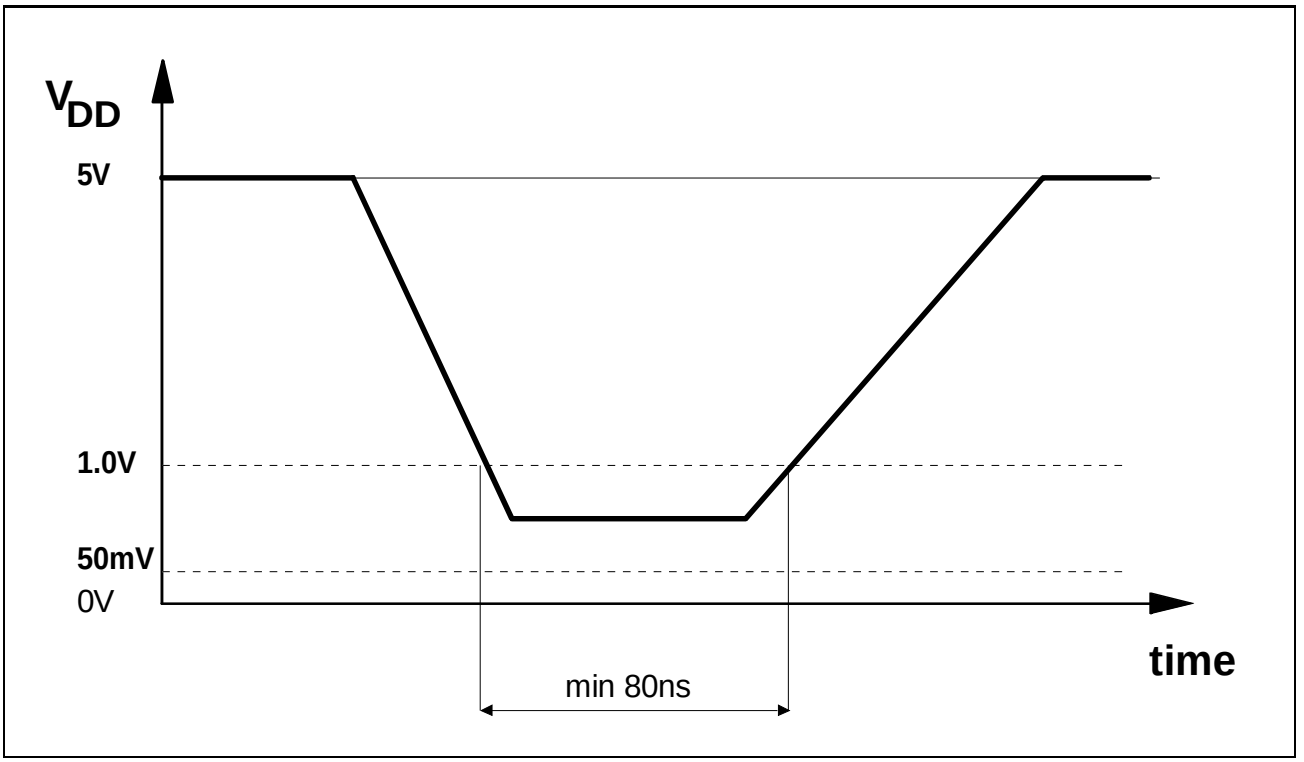


Figure 22
Power-on-reset behaviour of the DFE-Q V1.2 after V_{DD} collapse

Table 18
Parameters for POR activation (starting from 50mV< V_{DD}< 1.0V)

Parameter	Limit Values			Unit
	min.	typ.	max.	
Maximum V_{DD} slope			5V/4µs	
POR enable threshold	1.0			V
V_{DD} -below-1V-time	80			ns

2.7 U Interface

The U-interface establishes the direct link between the exchange and the terminal side. It consists of two copper wires. The ESCC8 uses four differential outputs (AOUT, BOUT) and four differential inputs (AIN, BIN) for transmission and reception. These differential signals are coupled via four hybrids and four transformers to the four two-wire U-interfaces. The nominal peak values of ± 3 correspond to a 3.2 Vpp chip output and 2.5 Vpp on the U-interface.

Direct access to the U-interface is not possible. 2B + D user data can be inserted and extracted via the IOM-2 interface. Control of maintenance bits is partly possible with IOM-2 monitor messages and power controller interface pins. The remaining maintenance bits are fully controlled by the Quad IEC DFE-Q itself and allow no external influence (e.g. CRC-checksum).

2.7.1 Frame Structure/Timing

Transmission over the U-interface is performed at a rate of 80 kBaud. The code used is reducing two binary informations to one quaternary symbol (2B1Q) resulting in a total of 160 kbit/s to be transmitted. 144 kbit/s are user data (B1 + B2 + D), 16 kbit/s are used for maintenance and synchronization information.

Data is grouped together into U-superframes of 12 ms each. The beginning of a new superframe is marked with an inverted synchronization word (ISW). Each superframe consists of eight basic frames (1.5ms) which begin with a standard synchronization word (SW) and contain 222 bits of information. The structure of one U-superframe is illustrated in figure **23**.

ISW	**1. Basic Frame**	**SW**	**2. Basic Frame**	**. . .**	**SW**	**8. Basic Frame**
<---			12 ms			--->

Figure 23
U-Superframe Structure

(I) SW **(Inverted) Synch Word** **18 Bit (9 Quat)**	**12 × 2B + D** **User Data** **216 Bits (108 Quat)**	**M1 – M6** **Maintenance Data** **6 Bits (3 Quat)**
<---	1,5 ms	--->

Figure 24
U-Basic Frame Structure

Table 19

U-Frame Structure

		Framing	2B + D	Overhead Bits (M1 – M6)					
	Quat Positions	1 – 9	10 – 117	118 s	118 m	119 s	119 m	120 s	120 m
	Bit Positions	1 – 18	19 – 234	235	236	237	238	239	240
Super Frame #	Basic Frame #	Sync Word	2B + D	M1	M2	M3	M4	M5	M6
1	1	ISW	2B + D	EOCa1	EOCa2	EOCa3	ACT/ ACT	1	1
	2	SW	2B + D	EOCd m	EOCi1	EOCi2	DEA / PS1	1	FEBE
	3	SW	2B + D	EOCi3	EOCi4	EOCi5	1/ PS2	CRC1	CRC2
	4	SW	2B + D	EOCi6	EOCi7	EOCi8	1/ NTM	CRC3	CRC4
	5	SW	2B + D	EOCa1	EOCa2	EOCa3	1/ CSO	CRC5	CRC6
	6	SW	2B + D	EOCd m	EOCi1	EOCi2	1	CRC7	CRC8
	7	SW	2B + D	EOCi3	EOCi4	EOCi5	UOA / SAI	CRC9	CRC 10
	8	SW	2B + D	EOCi6	EOCi7	EOCi8	AIB / NIB	CRC11	CRC12
2,3…									
						LT- to NT dir. >	/	< NT- to LT dir.	

– ISW Inverted Synchronization Word (quad): – 3 – 3 + 3 + 3 + 3 – 3 + 3 – 3 – 3
– SW Synchronization Word (quad): + 3 + 3 – 3 – 3 – 3 + 3 – 3 + 3 + 3
– CRC Cyclic Redundancy Check
– EOC Embedded Operation Channel

a = address bit
d/m = data / message bit
i = information (data / message)

– ACT Activation bit — ACT = (1) –> Layer 2 ready for communication
– DEA Deactivation bit — DEA = (0) –> LT informs NT that it will turn off
– CSO Colt Start Only — CSO = (1) –> NT-activation with cold start only
– UOA U-Only Activation — UOA = (0) –> U-only activated
– SAI S-Activity Indicator — SAI = (0) –> S-interface is deactivated
– FEBE Far-end Block Error — FEBE = (0) –> Far-end block error occurred
– PS1 Power Status Primary Source — PS1 = (1) –> Primary power supply ok

– PS2 Power Status Secondary Source	PS2 = (1) –> Secondary power supply ok
– NTM NT-Test Mode	NTM = (0) –> NT busy in test mode
– AIB Alarm Indication Bit	AIB = (0) –> Interruption (according to ANSI)
– NIB Network Indication Bit	NIB = (1) –> no function (reserved for network use)

Out of the 222 information bits 216 contain 2B+D data from 12 IOM-frames, the remaining 6 bits are used to transmit maintenance bits. Thus 48 maintenance bits are available per U-superframe. They are used to transmit two EOC-messages (24 bit), 12 overhead bits and one checksum (12 bit).

The function of EOC and overhead bits has already been discussed in connection with monitor messages. The next two sections describe how these bits are transmitted on the U-interface. Section “Cyclic Redundancy Check” describes the third group of maintenance bits, the cyclic redundancy checksum.

2.7.2 Embedded Operations Channel (EOC)

The embedded operations channel is used to transfer data from the exchange to the terminal side and vice versa without occupying B- or D-channels. It is used to transmit diagnostic functions and signaling information.

EOC-data is inserted into the U-frame at the positions M1, M2 and M3 thereby permitting the transmission of two complete EOC-messages within one U-superframe.

Access to the embedded operations channel is only possible via the EOC-processor and the monitor channel in IOM-2. With a MON-0-command a complete EOC-message (address field, data/message indicator and information field) can be passed to the NT side.

For a quick reference the key characteristics of the EOC channel are summarized on the following lines:

Function

EOC-data is inserted into the U-frame at the positions M1, M2 and M3 thereby permitting the transmission of two complete EOC-messages (2×12 bits) within one U-superframe.

An EOC-processor on the chip is responsible for the correct insertion and extraction of EOC-data on the U-interface. The EOC-processor can be programmed via auto- or transparent mode selection to implement automatic verification, acknowledgment and execution of EOC-commands (auto-mode). In states where no U-superframe is transmitted all EOC-bits on the U-interface are clamped to high.

Latching

Latching of diagnostic and loop-back functions is performed in auto-mode only. Latched functions are resolved with the RTN-command.

Modes

The EOC-processor of the Quad IEC DFE-Q can operate in auto- and transparent modes. The differences between the two modes available were already described in **section 2.1**. Features of auto- and transparent mode are therefore only briefly discussed here.

Auto-Mode

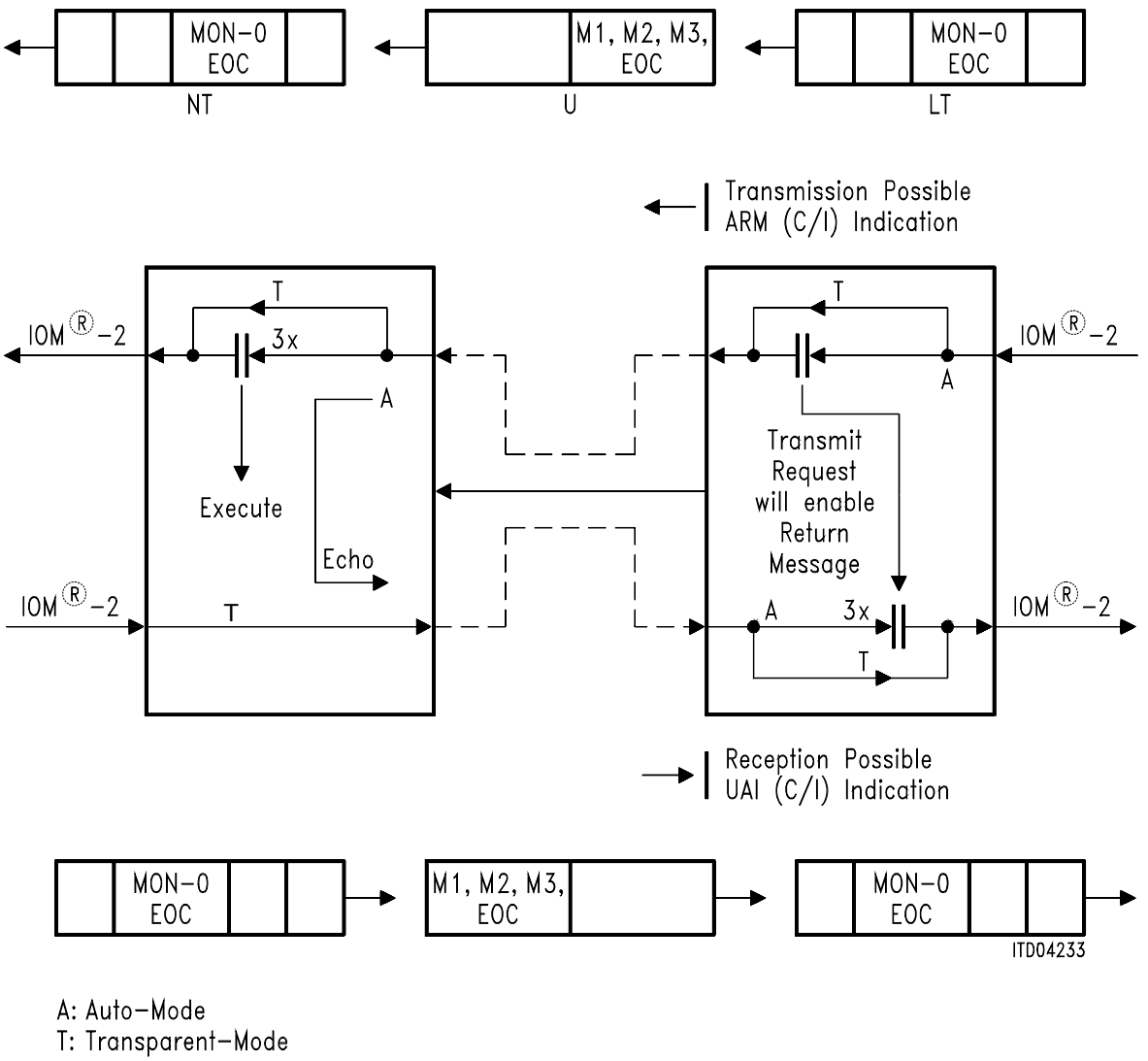
In auto-mode the EOC-processor will work as follows:

– Triple-last-look verification on EOC-messages
– Verified EOC-data will only be accepted if it is different to the previously accepted data
– Accepted new data is forwarded to the IOM-2-monitor channel
– Transmission of new EOC-data enables the reception of a return message even if no change in the EOC-channel has occurred

Transparent Mode

In transparent-mode the EOC-processor will work as follows:

– No verification on EOC-messages



– All received EOC-data is forwarded directly to the monitor channel (6 ms interval)

Figure 25

EOC-Procedure in Auto- and Transparent Mode

Codes

The EOC contains an address field, a data/message indicator and an eight-bit information field.

With the address field the destination of the transmitted message/data is defined. Addresses are defined for the NT, 6 repeater stations and broadcasting.

The data/message indicator needs to be set to (1) to indicate that the information field contains a message. If set to (0), numerical data is transferred to the NT. Currently no numerical data transfer to or from the NT is required.

From the 256 codes possible in the information field 64 are reserved for non-standard applications, 64 are reserved for internal network use and eight are defined by ANSI for diagnostic and loop-back functions. All remaining 120 free codes are available for future standardization. The eight ANSI defined functions are described in detail in **section 2.1.3.2** MON-0.

Table 20
Supported EOC-Commands

EOC						
Address Field			**Data/ Message Indicator**	**Information**	**O (rigin) D (estination)**		**Message**
a1	**a2**	**a3**	**d/m**	**i1 i2 i3 i4 i5 i6 i7 i8**	**LT**	**NT**	
0	0	0	x				NT
1	1	1	x				Broadcast
0 1	0 1	1 0	x				Repeater stations No. 1 – No. 6
			0				Data
			1				Message
			1	0 1 0 1 0 0 0 0	O	D	LBBD
			1	0 1 0 1 0 0 0 1	O	D	LB1
			1	0 1 0 1 0 0 1 0	O	D	LB2
			1	0 1 0 1 0 0 1 1	O	D	RCC
			1	0 1 0 1 0 1 0 0	O	D	NCC
			1	1 1 1 1 1 1 1 1	O	D	RTN
			1	0 0 0 0 0 0 0 0	D/O	O/D	H
			1	1 0 1 0 1 0 1 0	D	O	ACK

2.7.2.1 Overhead Bits

The positions M4 and M6 in the U-superframe is reserved for overhead bits. These bits are used to communicate status and maintenance functions between the transceivers. The meaning of a bit position is dependent upon the direction of transmission (upstream/ downstream) and the operation mode (repeater or NT/LT).

For details regarding single bits please refer to table Table 19 and the cross-references listed below.

Cross-references: **2.1.3.3** **MON-2-Commands**

2.7.2.2 Cyclic Redundancy Check

An error monitoring function is implemented covering the 2B + D and M4 data transmission of a U-superframe by a Cyclic Redundancy Check (CRC).

The computed polynomial is:

$$G(u) = u^{12} + u^{11} + u^3 + u^2 + u + 1$$

(+ modulo 2 addition)

The check digits (CRC bits CRC1, CRC2, …, CRC12) generated are transmitted in the U-superframe. The receiver will compute the CRC of the received 2B + D and M4 data and compare it with the received CRC-bits generated by the transmitter.

A CRC-error will be indicated to both sides of the U-interface, as a NEBE (Near-end Block Error) on the side where the error is detected, as a FEBE (Far-end Block Error) on the remote side. In case both values are not identical, the FEBE bit is set to (0) in order to indicate that transmission errors had occurred and will be placed in the next available U-superframe transmitted to the originator.

Table 21 shows this relationship.

Table 21
CRC in Superframes

LT –> NT Superframe				
… Z	A	B	C	D
…	1 2 3 4 5 6 7 8	1 2 3 4 5 6 7 8	1 2 3 4 5 6 7 8	1 2 3 4 5 6 7 8
…	CRC(Z), FEBE(–1)	CRC(A), FEBE(0)	CRC(B), FEBE(1)	CRC(C), FEBE(2)

NT –> LT Superframe				
…0	1	2	3	4
…	1 2 3 4 5 6 7 8	1 2 3 4 5 6 7 8	1 2 3 4 5 6 7 8	1 2 3 4 5 6 7 8
…	CRC(0), FEBE(Y)	CRC(1), FEBE(Z)	CRC(2), FEBE(A)	CRC(3), FEBE(B)

----------> Time

Far-end or near-end error indications increment the corresponding block error counters of exchange and terminal side.

It is not possible to access the CRC-checksum. Hence the user cannot read or write the checksum values.

Figure 26 illustrates the CRC-process.

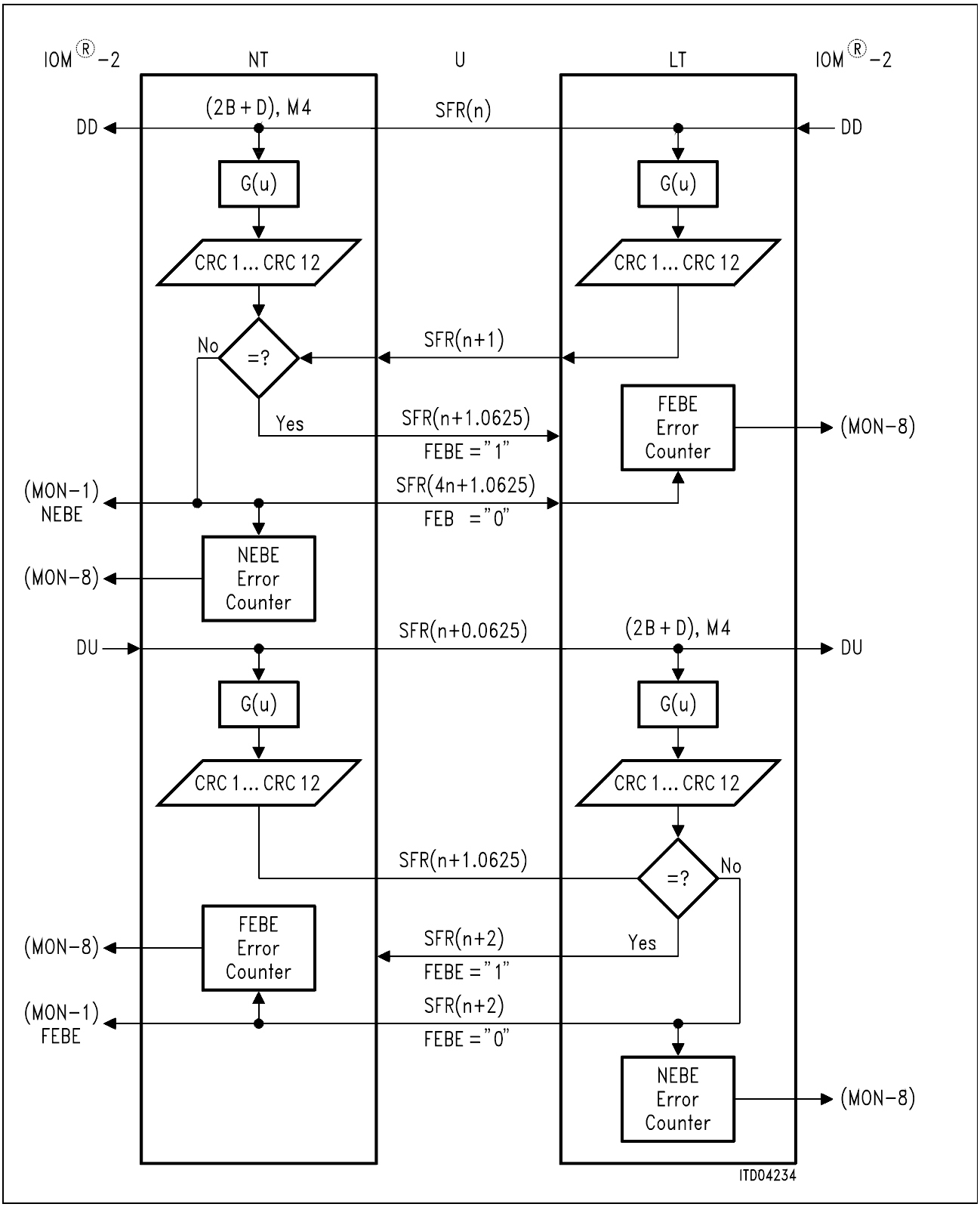


Figure 26 CRC-Process

2.7.2.3 Scrambler/Descrambler

The scrambling algorithm provided by ANSI T1.601 ensures that no sequences of permanent binary 0s or 1s are transmitted. In the receiver the scrambled signal is reconstructed with a descrambling algorithm. The scrambling/descrambling process is controlled fully by the Quad IEC DFE-Q. No influence can be taken by the user. Note that the scrambling algorithm can not be switched off nor by passed.

The algorithms used for scrambling and descrambling in LT- and NT-modes are described in **figure 27**. When Loopback #1 is applied, the descrambling is done with the NT-Mode algorithm.

Note that one wrong bit decision in the receiver automatically leads to at least three bit errors. Whether all of these are recorded by a bit error counter depends on wether all faulty bits are part of the monitored channels or not.

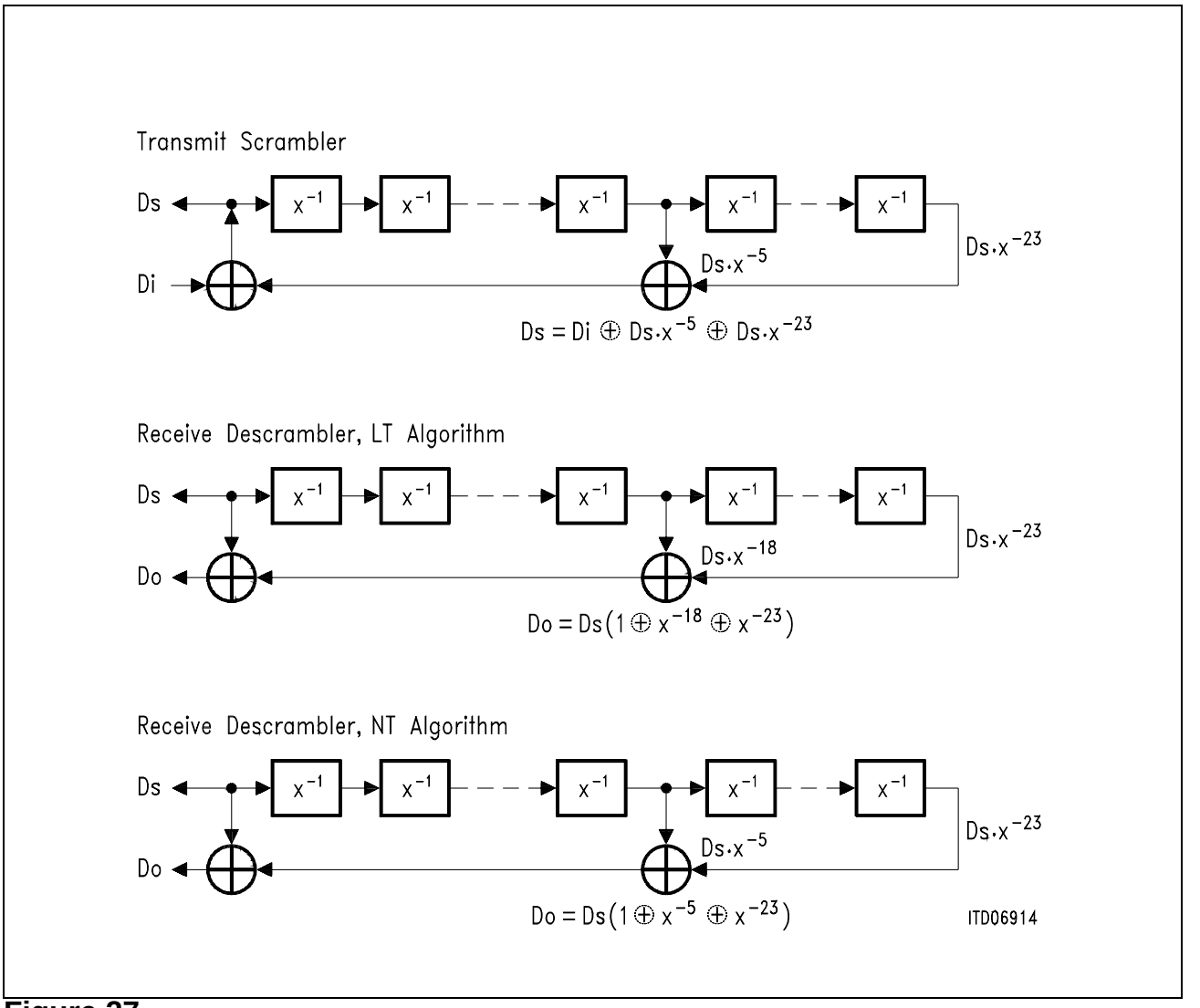


Figure 27
Scrambler / Descrambler Algorithms

2.8 Control Procedures

Control procedures describe the commands and messages required to control the PEB 24911. The DEF-Q V1.2 is designed to meet the newest standards of ANSI and ETSI regarding status control. This chapter shows the user how to activate and deactivate the device under various circumstances and illustrates the interaction between the stations involved.

Two types of start-up procedures are supported by the Quad IEC DFE-Q: cold starts and warm starts.

Cold starts are performed after a reset and require all echo and equalizer coefficients to be recalculated. This procedure typically is completed after 1-7 seconds depending on the line characteristic. Cold starts are recommended for activations where the line characteristic has changed considerably since the last deactivation.

A **warm start** procedure uses the coefficient set saved during the last deactivation. It is therefore completed much faster (maximum 300 ms). Warm starts are however restricted to activations where the line characteristic has not changed significantly since the last deactivation.

Both start-up procedures differ only in the fact that the device has been transferred into the TEST state prior to activation. Activation initialization and procedure is in both cases identical. The following sections thus apply to both warm and cold start-ups.

The following table explains all U-interface signals used in the following sections as defined by ANSI.

Table 22
U-Interface Signals

Signal	Synch. Word (SW)	Superframe (ISW)	2B + D	M-Bits
NT-Modes (NT –> LT)				
TN [1)]	± 3	± 3	± 3	± 3
SN0	no signal	no signal	no signal	no signal
SN1	present	absent	1	1
SN2	present	absent	1	1
SN3	present	present	1	normal
SN3T	present	present	normal	normal
LT-Modes (LT –> NT)				
TL [1)]	± 3	± 3	± 3	± 3

Signal	Synch. Word (SW)	Superframe (ISW)	2B + D	M-Bits
SL0	no signal	no signal	no signal	no signal
SL1	present	absent	1	1
SL2	present	present	0	normal
SL3 [2)]	present	present	0	normal
SL3T	present	present	normal	normal
Test Mode				
SP [3)]	no signal	no signal	± 3	no signal

Notes: *[1)] Alternating ± 3 symbols at 10 kHz*

[2)] Must be generated by the exchange

[3)] Alternating ± 3 single pulses of 12.5 ms duration spaced by 1.5 ms

2.8.1 Complete Activation Initiated by LT

	NT IOM-2		LT IOM-2		
<———	C/I DC	(1111_B)	CI/DC	(1111_B)	<———; Initial state is “Deactivated”
———>	C/I DI	(1111_B)	C/IDI	(1111_B)	———>;
<———	C/I PU	(0111_B)	**C/I AR**	**(1000_B)**	**<–––––**; Start activation
<———	C/I DC	(1111_B)	C/I AR	(1000_B)	———>; Activation proceeds
			C/I ARM	(1001_B)	———>; :
<———	C/I AR	(1000_B)	C/I UAI	(0111_B)	———>; :
–––––>	**C/I AI**	**(1100_B)**			; Confirm that terminal is ; active
<———	C/I AI	(1100_B)	C/I AI	(1100_B)	———>; Activation complete

Figure 28 depicts the procedure if the activation has been initiated by the exchange side.

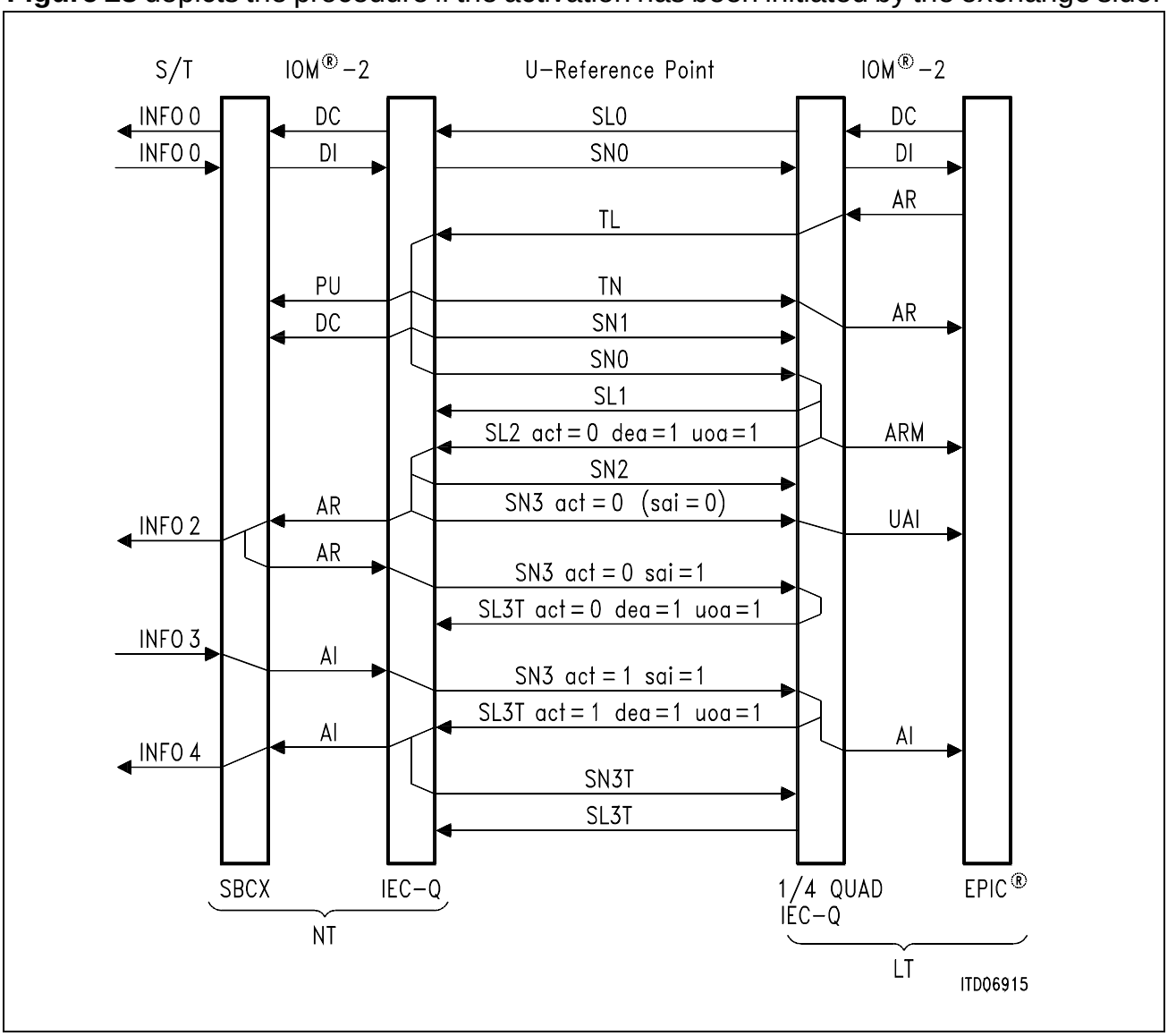


Figure 28
Complete Activation Initiated by LT

Instead of the command AR, ARX can be used to initiate the activation. In that case, the 15 sec timer (T1) is disabled. No error EI3 will occur, if the activation was not successful.

2.8.2 Activation with ACT-Bit Status Ignored by the Exchange Side

The LT ignores the ACT-bit transmitted upstream from the NT if the LT-activation has been initiated with AR0 instead of AR. Because the activation with AR0 is performed with the UOA-bit set to “0”, initially only a partial activation is started. By setting UOA=1 via a MON2 message the S-interface is activated as well.

	NT IOM-2		LT IOM-2		
<———	C/I DC	(1111_B)	C/I DC	(1111_B)	<———; Initial state is “Deactivated”
———>	C/I DI	(1111_B)	C/I DI	(1111b)	———>;
			C/I AR0	**(1101_B)**	**<–––––**; Start activation
<———	C/I PU	(0111_B)	C/I AR	(1000_B)	———>; Activation proceeds with
<———	C/I DC	(1111_B)	C/I ARM	(1001_B)	———>; UOA = 0
			C/I UAI	(0111_B)	———> ;
			MON8 PACE ($80\ BE_H$)		**<–––––**; Enable control of UOA-bit
			MON2 UOA ($2F\ FF_H$)		**<–––––**; and set UOA = 1
<———	C/I AR	(1000_B)			
–––––>	**C/I AI**	**(1100_B)**			; Confirm that terminal is ; active
<———	C/I AR	(1000_B)	C/I UAI	(1100_B)	———>; ACT-bit status ignored
			C/I AR	**(1000_B)**	**<–––––**; Enable ACT-bit evaluation
<———	C/I AI	(1100_B)	C/I AI	(1100_B)	**–––––**>; Activation complete
			C/I AR0	**(1101_B)**	**<–––––**; Disable ACT-bit evaluation
<———	C/I AR	(1000_B)	C/I UAI	(0111_B)	———>; ACT-bit status ignored

Activation with C/I-command “AR0” forces the state machine into the state “Line Active” independently of the ACT-bit status transmitted upstream from the network. Activation may be completed after the ACT-bit evaluation has been enabled with C/I-command “AR”.

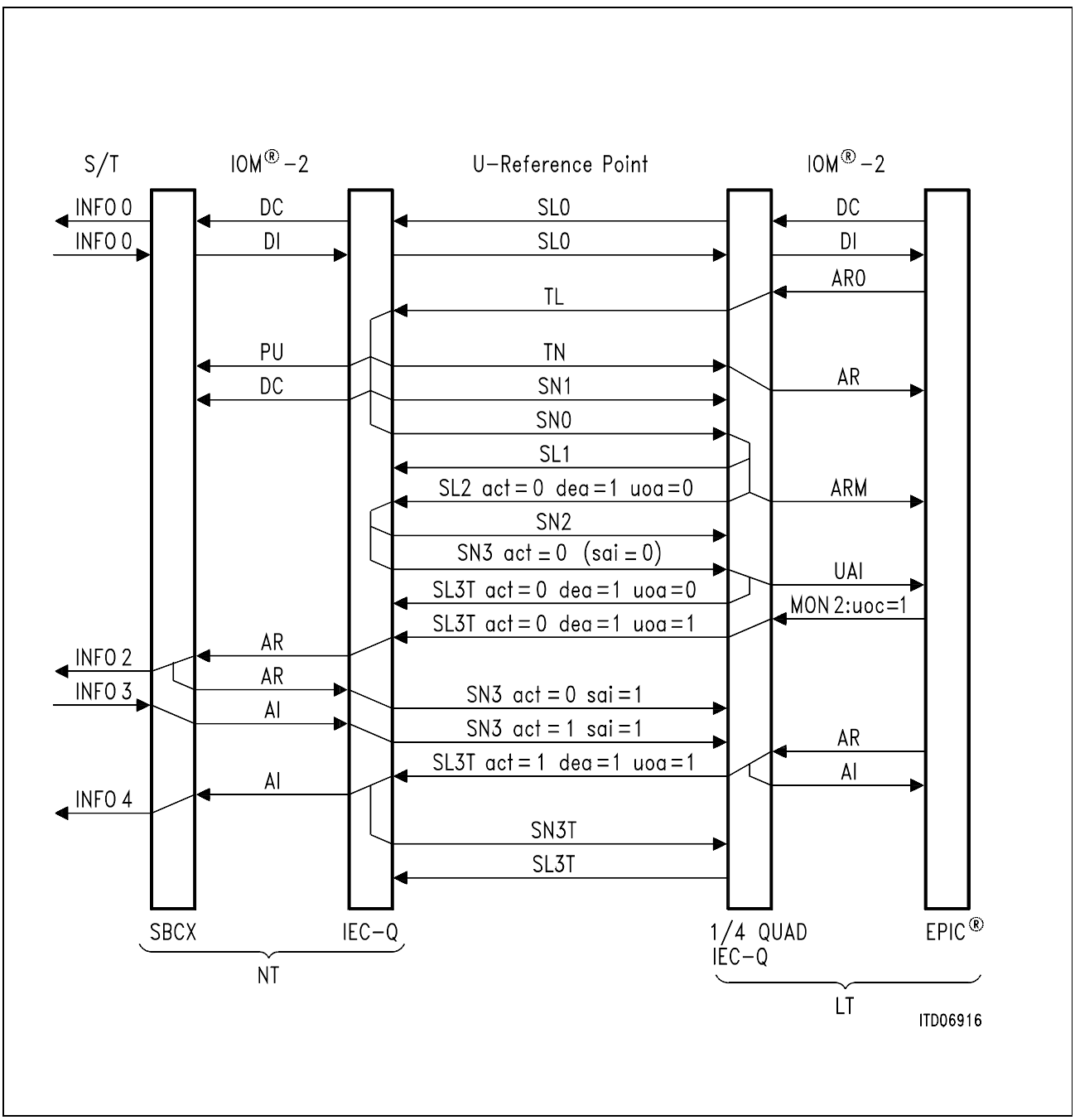


Figure 29

Activation with ACT-Bit Status Ignored by the Exchange

2.8.3 Complete Activation Initiated by TE

When initiating an activation from the terminal side, the LT must be in the “DEACTIVATED” state. For a TE initiated activation to be successful the downstream LT C/I-code must be DC. This is not the case if the “DEACTIVATED” state has been entered from the “TEST” state (the last code is DR in this case).

	NT IOM-2		LT IOM-2		
<———	C/I DC	(1111_B)	C/I DC	(1111_B)	<———; Initial state is “Deactivated”
———>	C/I DI	(1111_B)	C/I DI	(1111_B)	———>
–––––>	**C/I TIM** [1]	**(0000_B)**			; Start IOM-clocks
<———	C/I PU	(0111_B)			; DFE-Q is in power-up
–––––>	**C/I AR**	**(1000_B)**			
–––––>	**TIM release** [2]				; Start activation
<———	C/I DC	(1111_B)	C/I AR	(1000_B)	———>; Activation proceeds
			C/I ARM	(1001_B)	———>; :
<———	C/I AR	(1000_B)	C/I UAI	(0111_B)	———>; :
–––––>	**C/I AI**	**(1100b)**			; Confirm that terminal is ; active
<———	C/I AI	(1100_B)	C/I AI	(1100_B)	———>; Activation complete

Notes: [1] *For the PEB 2070 TIM is requested with register SPCR = 80_H*
[2] *For the PEB 2070 TIM release is requested with register SPCR = 00_H*

Figure 30 depicts the procedure if the activation has been initiated by the terminal side.

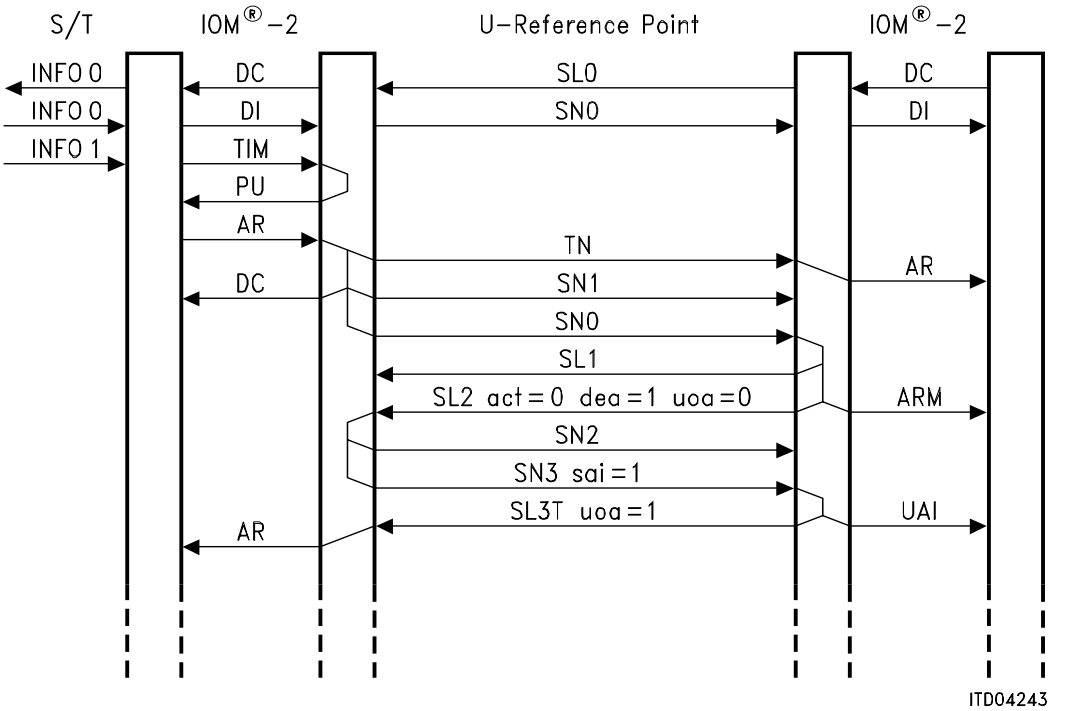


Figure 30
Complete Activation Initiated by TE

2.8.4 Activation Attempt Initiated by NT in NT-Auto-Mode

In IEC-Q Version 4.3 and following versions the NT-auto-mode has been additionally implemented. In this mode the NT IEC-Q will start one single activation attempt after leaving the “TEST” state, i.e. after being resetted. In case the LT is in the condition where it can be activated, activation proceeds as described in the previous section.

The example below illustrates the procedure if the LT refuses to acknowledge the activation attempt.

	NT IOM-2		LT IOM-2			
<------	C/I DR	(0000_B)	C/I DEAC	(0001b)	------>	; Both side in “TEST” state
------>	**C/I RES**	**(0001_B)**	**C/I RES**	**(0001b)**	**<------**	;
------>	**C/I DI**	**(1111_B)**				“TEST” state left for 1. time
<------	C/I DC	(1111_B)				NT activation attempt failes,
<------	C/I EI1	(0100_B)				because LT in “TEST”
<------	C/I DR	(0000_B)				state.
<------	C/I DC	(1111_B)				

2.8.5 Complete Deactivation

Deactivating the U-interface can be initiated only by the exchange. A deactivation can be started when the device is in the states ’LINE ACTIVE’, ’PEND. TRANSPARENT’ or ’TRANSPARENT’ or ’S/T DEACTIVATED’.

	NT IOM-2		LT IOM-2			
			C/I DR	(0000_B)	<------	; Start deactivation
<------	C/I DR	(0000_B)	C/I DEAC	(0001_B)	------>	; Deactivation proceeds
			C/I DI	(1111_B)	------>	; Deactivation complete on ; LT
------>	C/I DI	(1111_B)				; Power down NT
<------	C/I DC	(1111_B)				; Deactivation complete on ; NT

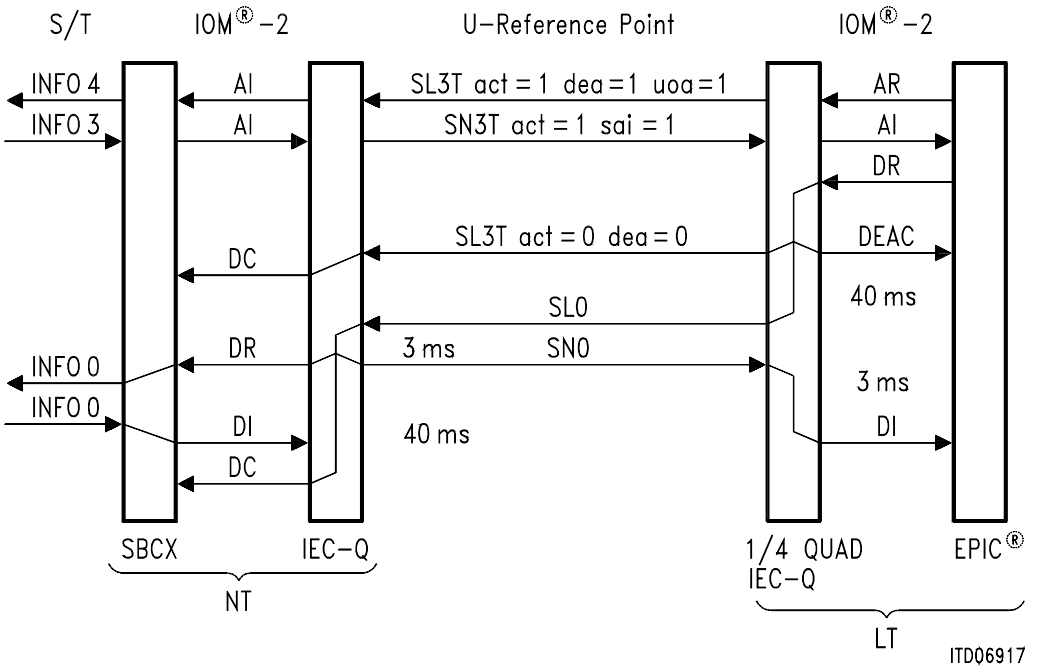


Figure 31
Complete Deactivation

2.8.6 Partial Activation (U Only)

Activating the U-interface only partially is a requirement specified by the CNET. The S-interface remains deactivated.

When activating partially from the LT-side, the exchange has two options:

First, in case the C/I-command DC is not issued after the partial activation is complete, the exchange has to issue AR (see **section 2.8.8 case 1**) before a terminal initiated complete activation request is accepted. This allows the exchange to retain full control, even in case of terminal initiated activation requests.

Secondly the exchange can issue DC after UAI has been received. This allows the terminal to activate the S-interface independently of the exchange (see **section 2.8.8 case 2**). In this case the exchange has no control of the S-interface activation procedure.

	NT IOM-2		LT IOM-2			
<------	C/I DC	(1111_B)	C/I DC	(1111_B)	<------	; Initial state is “Deactivated”
------>	C/I DI	(1111_B)	C/I DI	(1111_B)	------>	
			C/I UAR	**(0111_B)**	**<------**	; Start partial activation
<------	C/I PU	(0111_B)	C/I AR	(1000_B)	------>	; Activation proceeds
<------	C/I DC	(1111_B)	C/I ARM	(1001_B)	------>	; :
			C/I UAI	(0111_B)	------>	; Partial activation complete
			[C/I DC	(1111_B)]	<------	; Exchange retains no ; control of S-interface ; activation

The NT IEC-Q is in the “Synchronized 1” state (see IEC-Q v4.3 User’s Manual 02/95 page 175) after a successful partial activation. IOM-2-clocks DCL and FSC are issued. On DOUT the C/I-message “DC” as well as the LT-user data is sent.

While the C/I-messages “DI” (1111b) or “TIM” (0000b) are received on DIN at the NT, the IEC-Q Vers. 4.3 will transmit “SAI” = (0) upstream. Any other code results in “SAI” = (1) to be sent. On the U-interface the signal SN3 (i.e. 2B + D = (1)) will be transmitted continuously regardless of the data on DIN.

The LT will transmit all user data transparently downstream (signal SL3T). In case the last C/I-command applied to DIN was “UAR”, the LT retains activation control when an activation request comes from the terminal (confirmation with C/I = “AR” required, see section **2.8.8** case 1). With C/I “DC” applied on DIN, TE initiated activations will be completed without the necessity of an exchange confirmation (section **2.8.8** case 2).

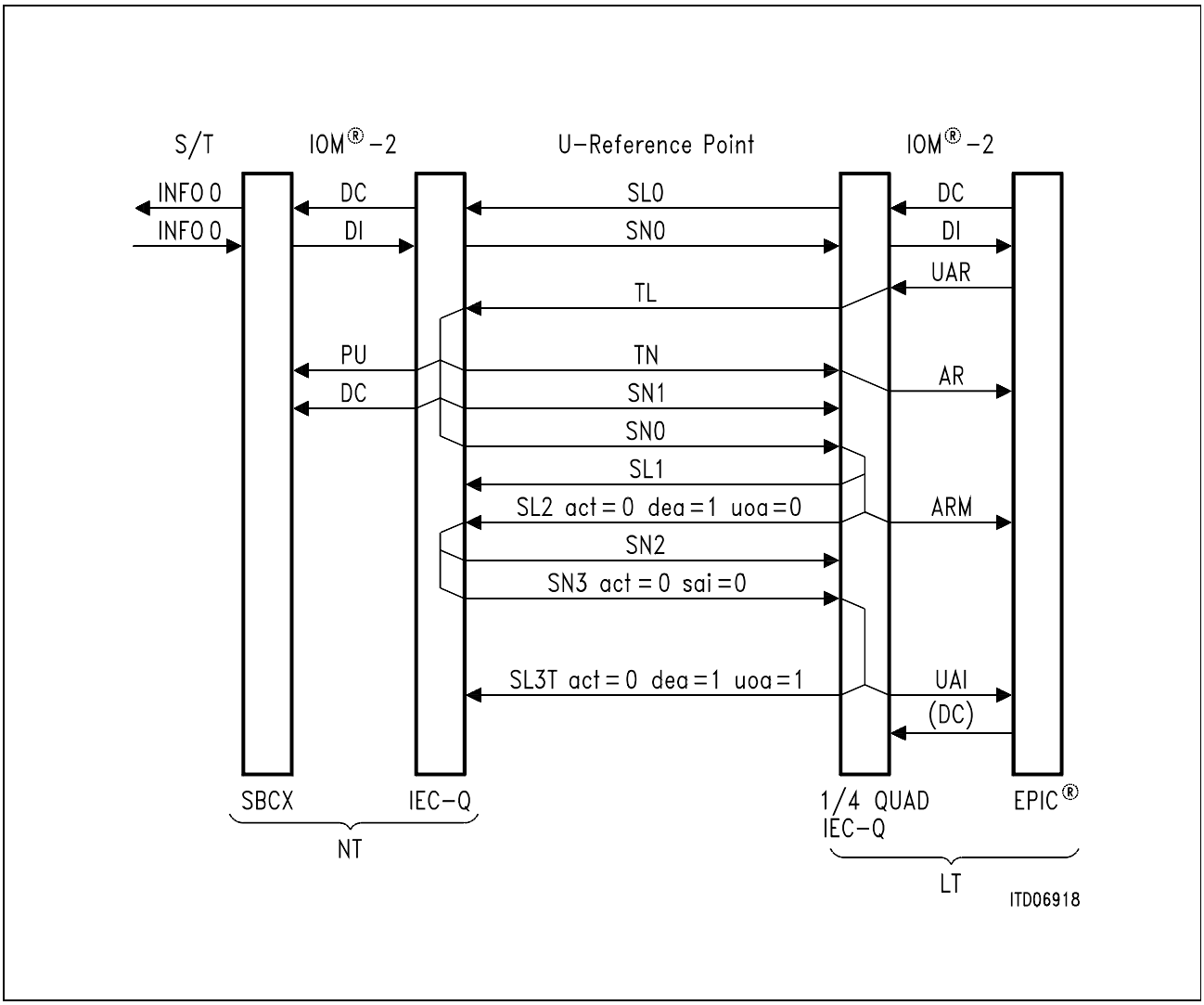


Figure 32
U Only Activation

2.8.7 Complete Activation Initiated by LT with U Active

When U is already active, the S-interface can be activated either by the exchange or the terminal. The first case is described here, the second in the next section.

	NT IOM-2		LT IOM-2			
<------	C/I DC	(1111_B)	C/I UAR [DC]		<------	; U only is activated
------>	C/I DI	(1111_B)	C/I UAI	(0111_B)	------>	; [exchange retains ; no control]
			C/I AR	**(1000_B)**	**<------**	; Start complete activation
<------	C/I AR	(1000_B)				
------>	**C/I AR**	**(1100_B)**				
			C/I AR	(1000_B)	------>	; Activation proceeds
------>	**C/I AI**	**(1100_B)**				; Confirm that terminal is ; active
			C/I UAI	(0111_B)	------>	
<------	C/I AI	(1100_B)	C/I AI	(1100_B)	------>	; Activation complete

The S-interface is activated from the exchange with the command “AR”. Bit “UOA” changes to (1) requesting S-interface activation.

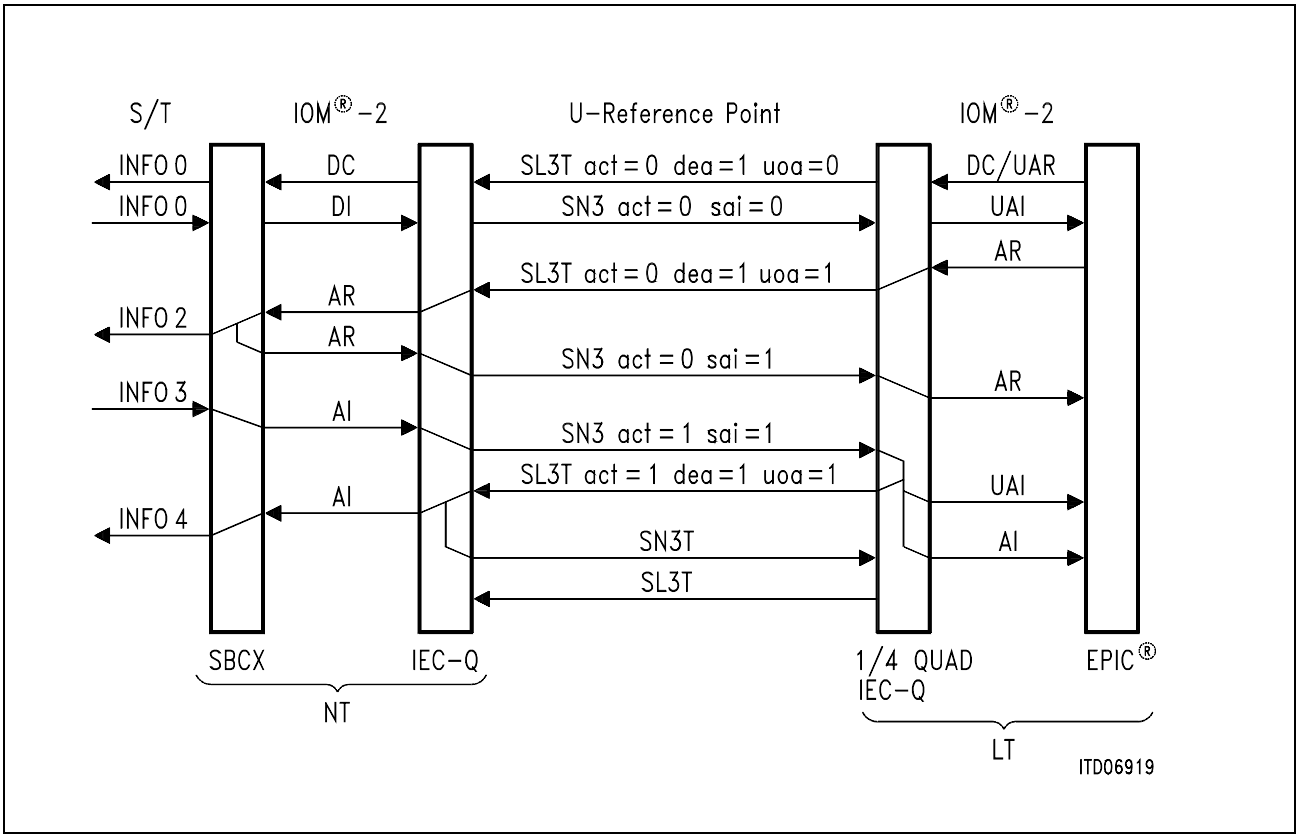


Figure 33
LT Initiated Activation with U-Interface Active

2.8.8 Complete Activation Initiated by TE with U Active

When the terminal requests to activate the S-interface (U-interface already active) two cases can occur:

In the first case the exchange has retained control over the S-interface activation. Then S-activation can proceed only after the explicit permission by the exchange with AR. This situation is discussed in this section under “case 1”.

In the second case the exchange is not requested to send AR in order to continue activation. This situation is described in “case 2” of this section.

The terminal recognizes no difference between the two types, the procedure on NT-side consequently is identical in both cases.

Case 1 (controlled by exchange)

	NT IOM-2		LT IOM-2			
<------	C/I DC	(1111_B)	C/I UAR	(0111_B)	<------	; U only is activated
------>	C/I DI	(1111_B)	C/I UAI	(0111_B)	------>	
------>	**C/I AR**	**(1000_B)**				; Terminal requests ; activation
			C/I AR	(1000_B)	------>	; Exchange is notified of ; request
			C/I AR	**(1000_B)**	**<------**	; Exchange permits ; S-activation
<------	C/I AR	(1000_B)				
------>	**C/I AI**	**(1100_B)**				; Confirm that terminal is ; active
			C/I UAI	(0111_B)	------>	
<------	C/I AI	(1100_B)	C/I AI	(1100_B)	------>	; Activation complete

Case 2 (no control by exchange)

	NT IOM-2		LT IOM-2			
<------	C/I DC	(1111_B)	C/I DC		<------	; U only is activated
------>	C/I DI	(0011_B)	C/I UAI	(0111_B)	------>	
------>	**C/I AR**	**(1000_B)**				; Terminal requests ; activation
			C/I AR	(1000_B)	------>	; Exchange is notified of
<------	C/I AR	(1000_B)				; proceeding S-activation
------>	**C/I AI**	**(1100_B)**				; Confirm that terminal is ; active
			C/I UAI	(0111_B)	------>	
<------	C/I AI	(1100_B)	C/I AI	(1100_B)	------>	; Activation complete

The TE initiates complete activation with INFO 1 leading to “SAI” = (1). Case 1 requires the exchange side to acknowledge the TE-activation by sending C/I = “AR”, Case 2 activates completely without any LT-confirmation.

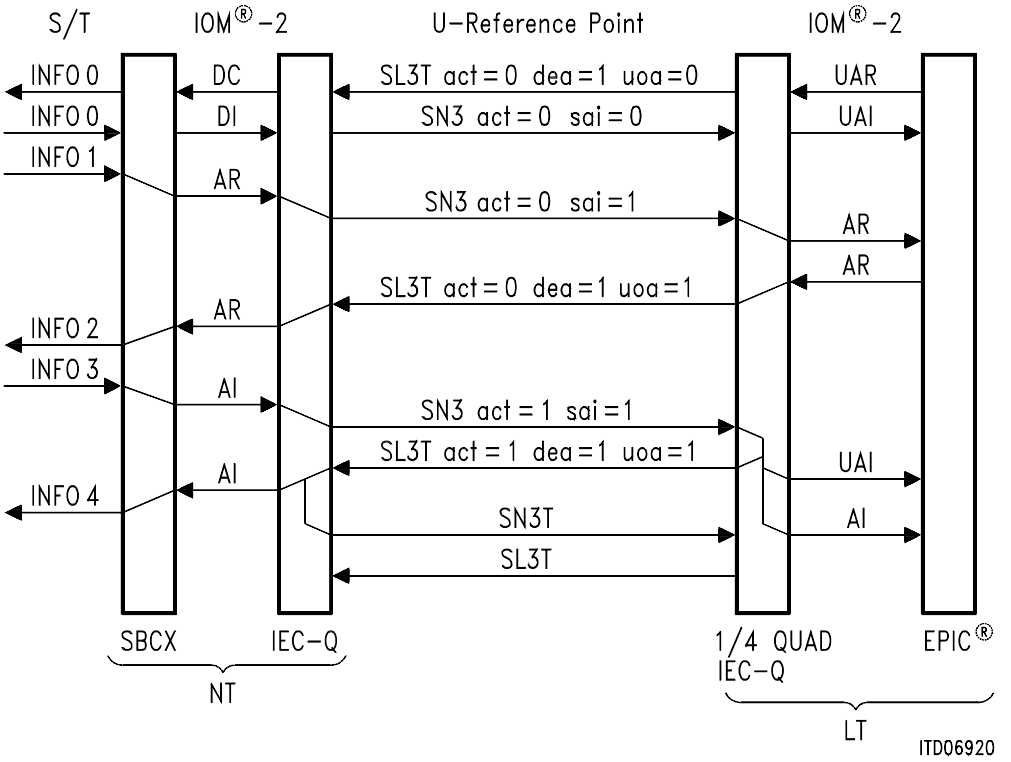


Figure 34

TE-Activation with U Active and Exchange Control (case 1)

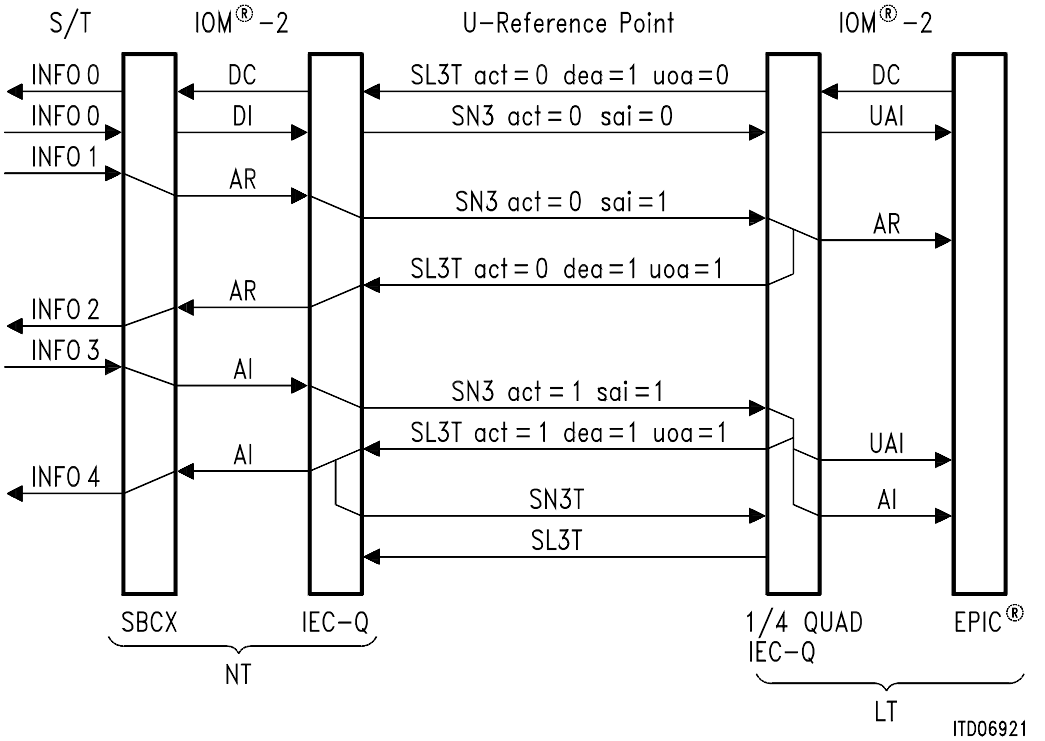


Figure 35
TE-Activation with U Active and no Exchange Control (case 2)

2.8.9 Deactivating S/T-Interface Only

The following shows the procedure for deactivating the S-interface only while leaving the U-interface active.

	NT IOM-2		LT IOM-2		
<------	C/I AI	(1100_B)	C/I AI	(1100_B)	------> ;Initial state: layer 1 activated
------>	C/I AI	(1100_B)	C/I AR	(1000_B)	<------
<------	C/I DR	(0000_B)	**C/I UAR**	**(0111_B)**	**<------** ; Deactivate S-interface only
------>	**C/I DI**	**(1111_B)**	C/I UAI	(0111_B)	------> ; S-interface is deactivated
<------	C/I DC	(1111_B)	[C/I DC	(1111_B)]	<------ ; Exchange retains no control

Deactivation of the S-interface only is initiated from the exchange by setting the “UOA” bit = (0).

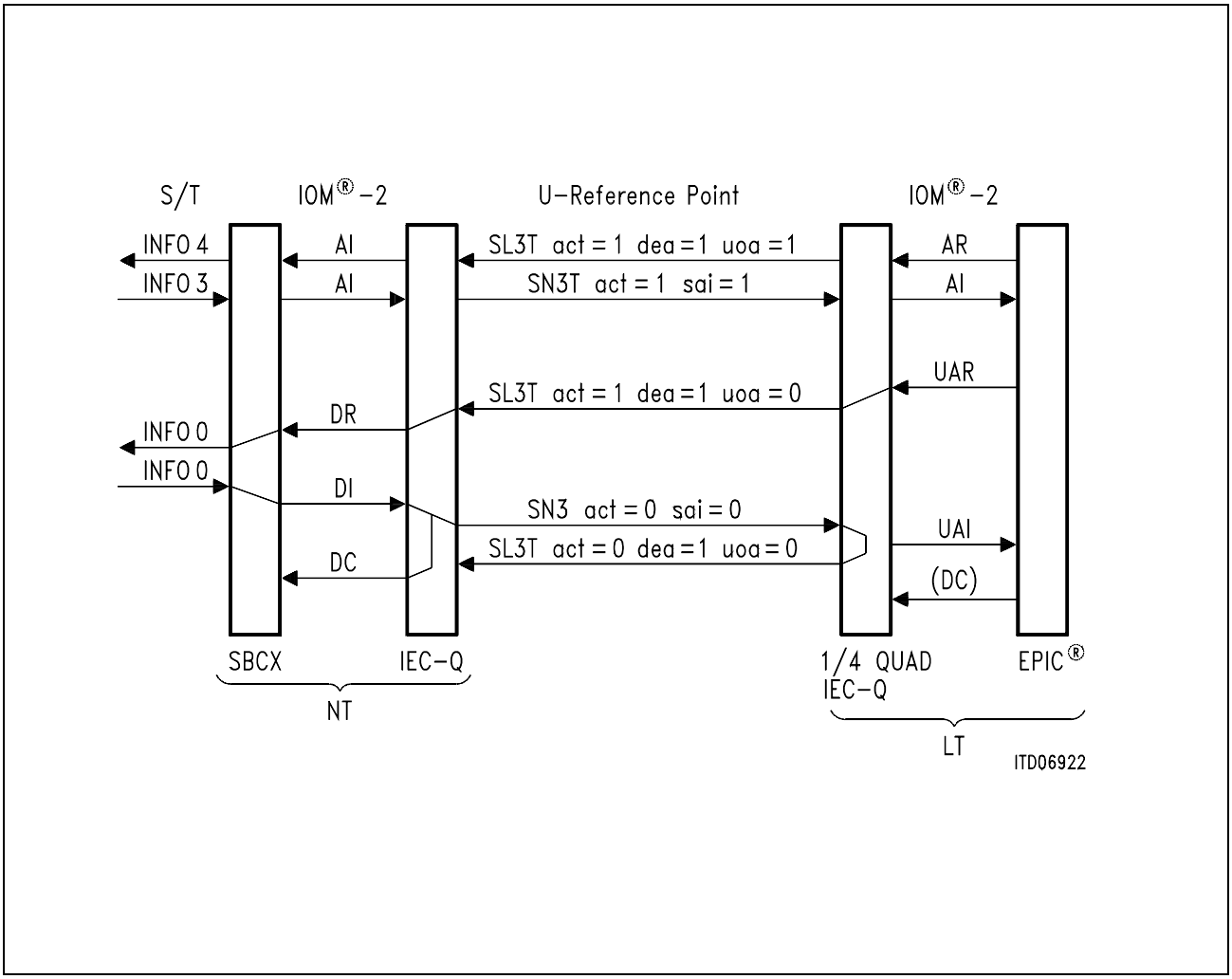


Figure 36
Deactivation of S/T Only

2.8.10 Activation Initiated by LT with Repeater

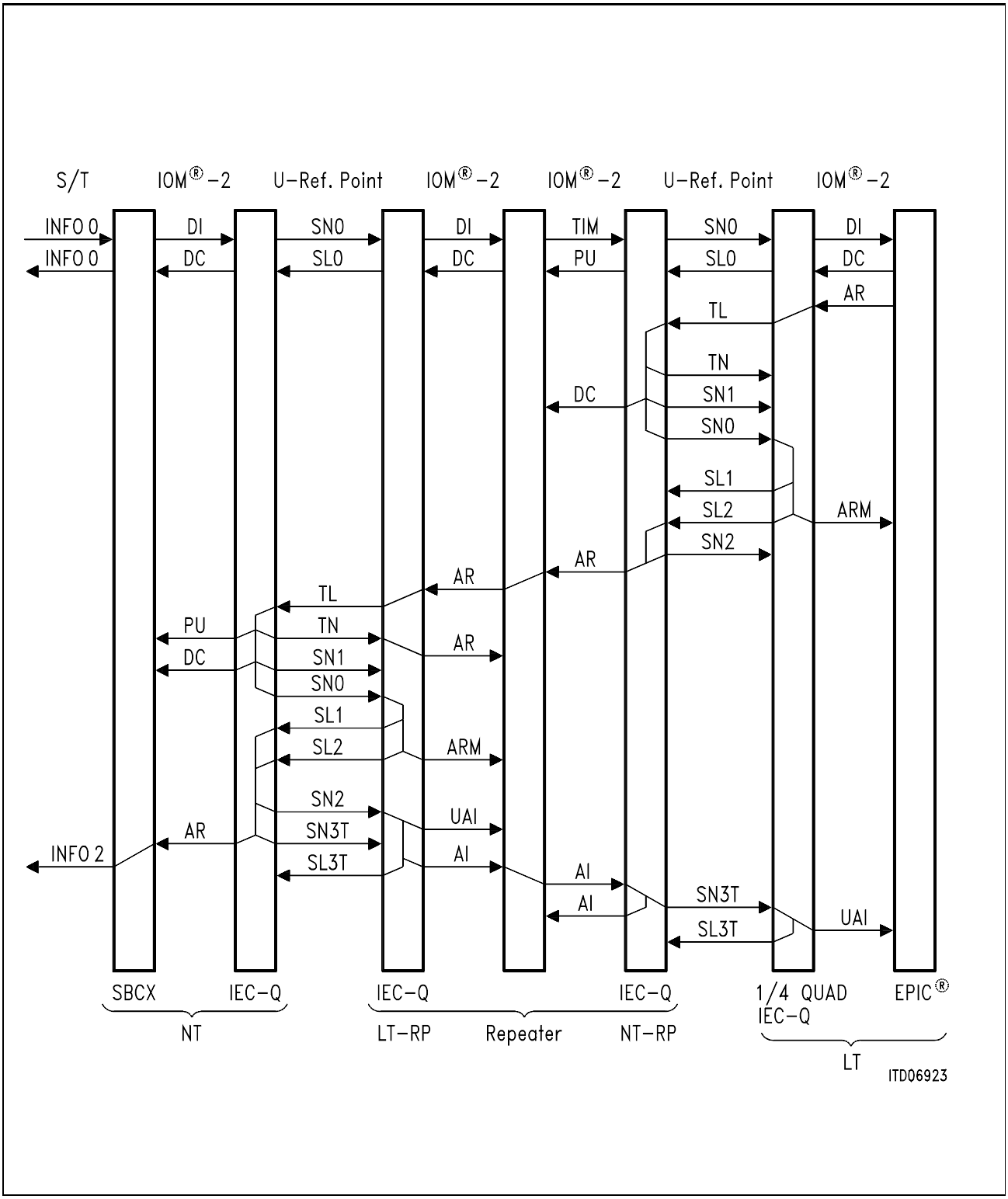


Figure 37
Activation with Repeater Initiated by LT

2.8.11 Activation Initiated by TE with Repeater

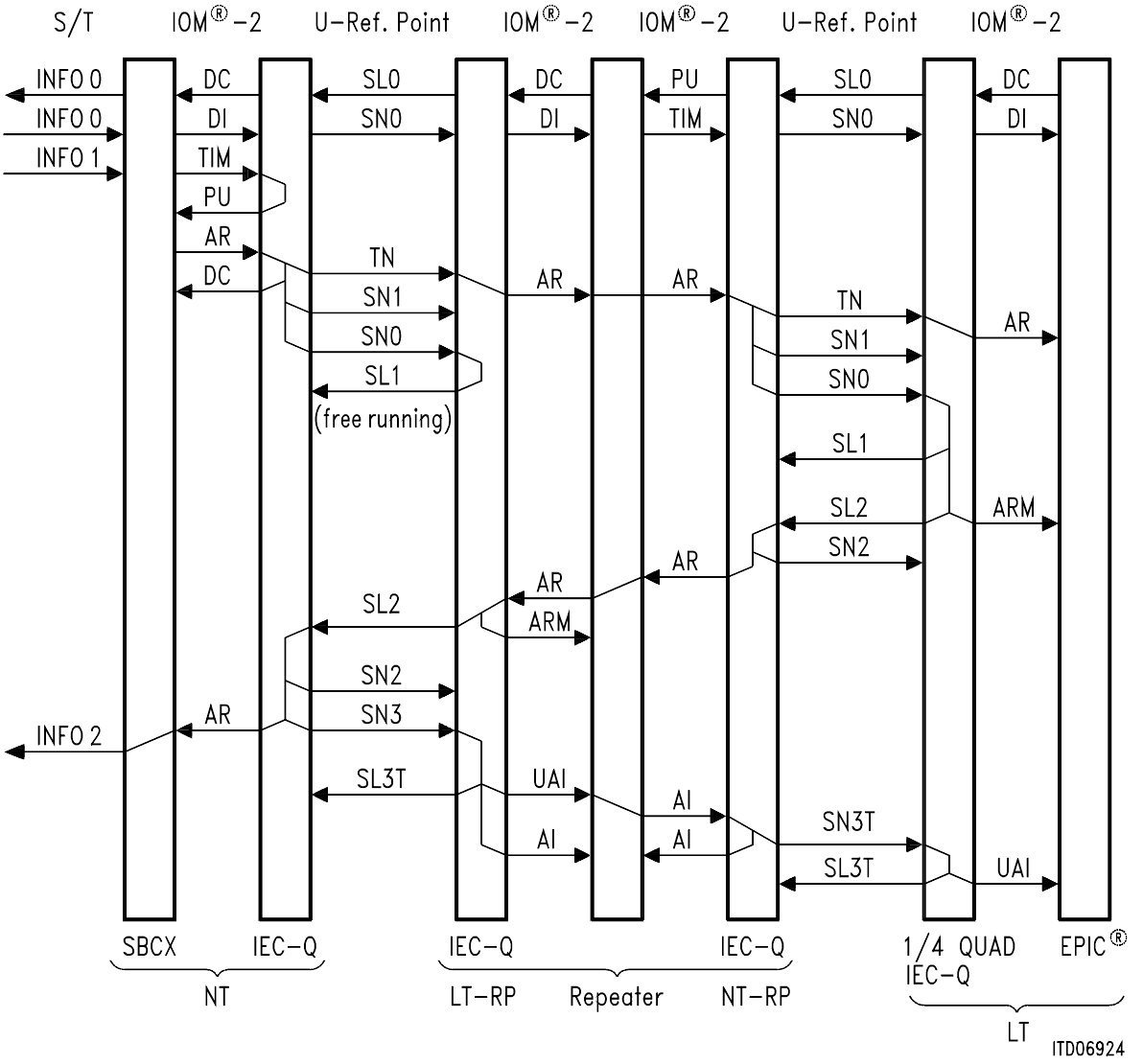


Figure 38
Activation with Repeater Initiated by TE

2.8.12 Loss of Synchronization / Signal at Repeater

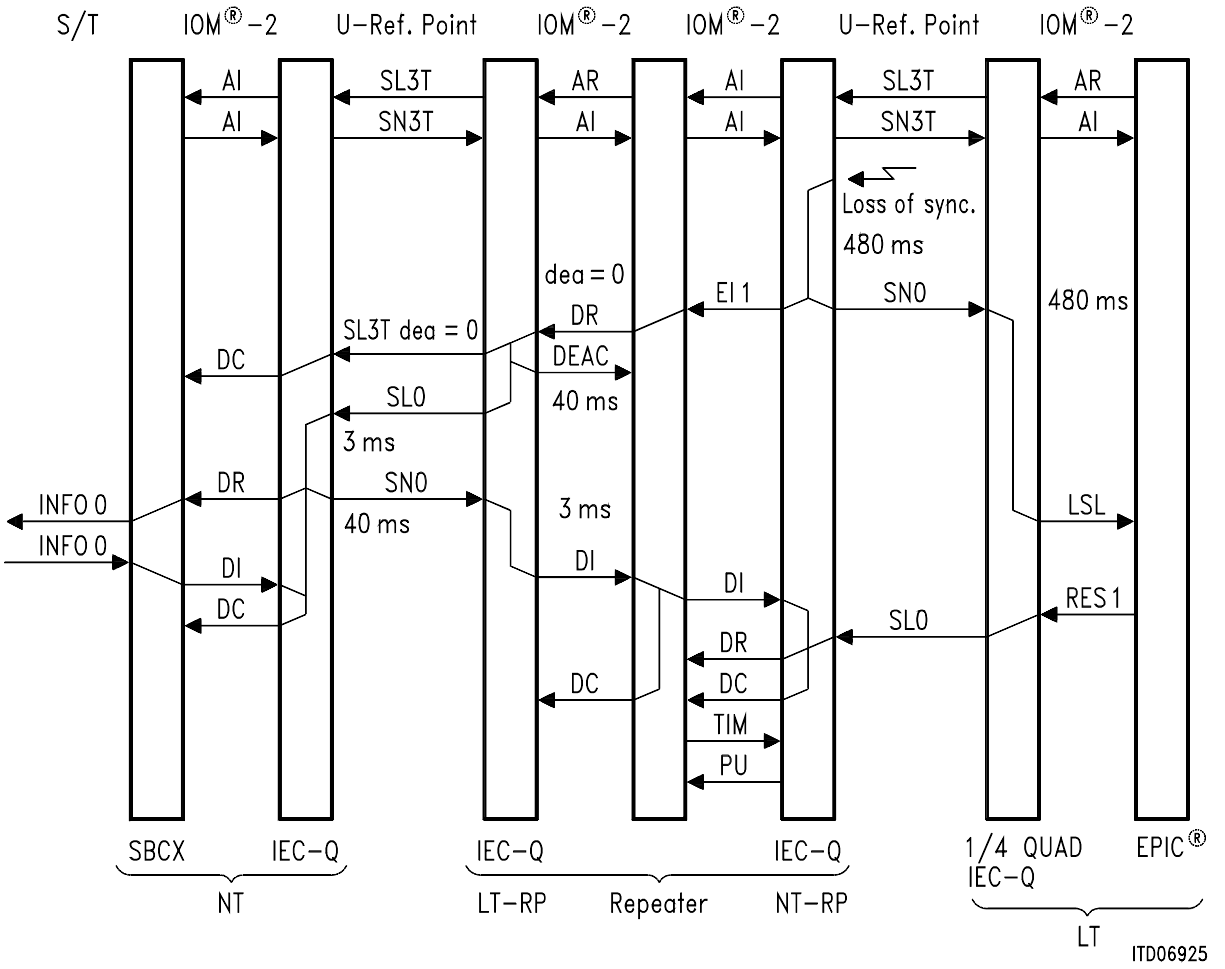
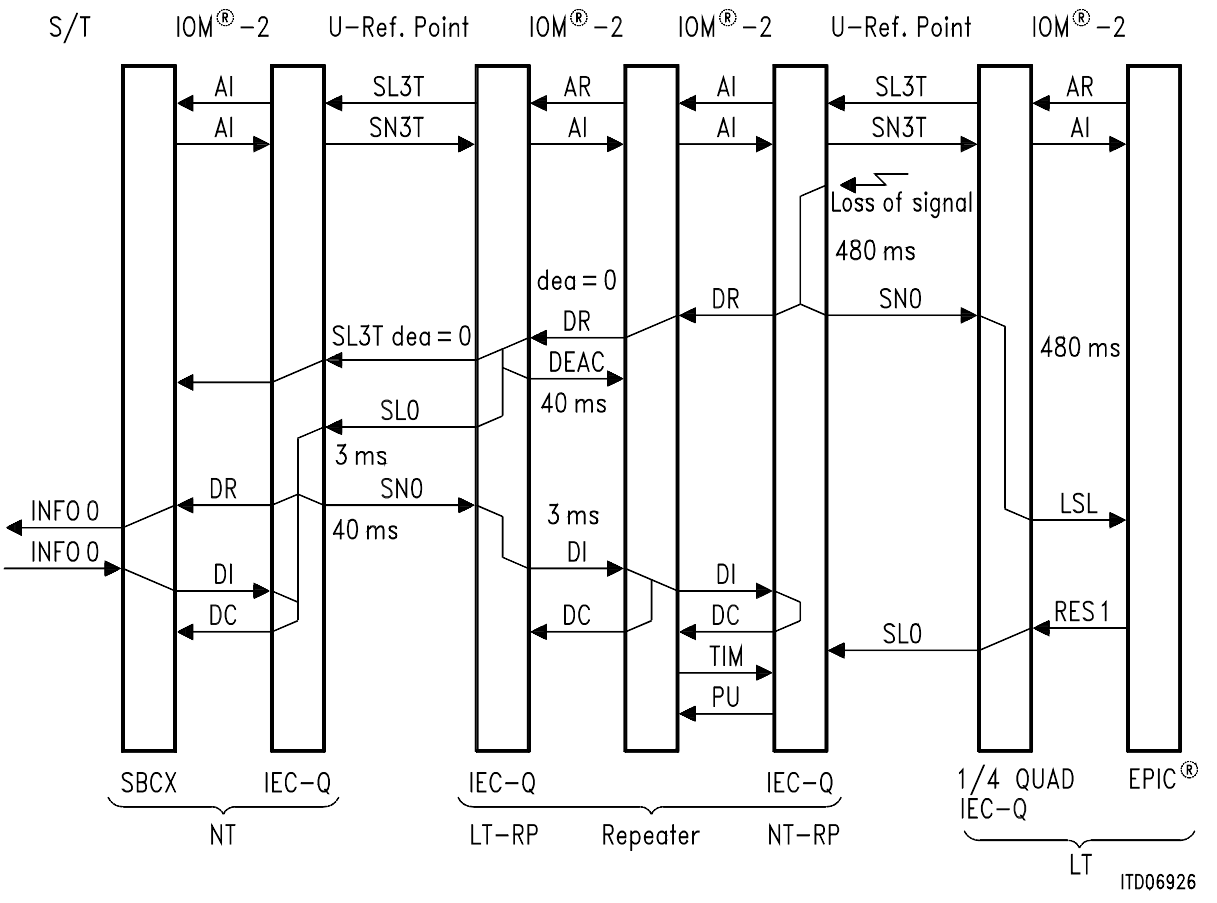


Figure 39

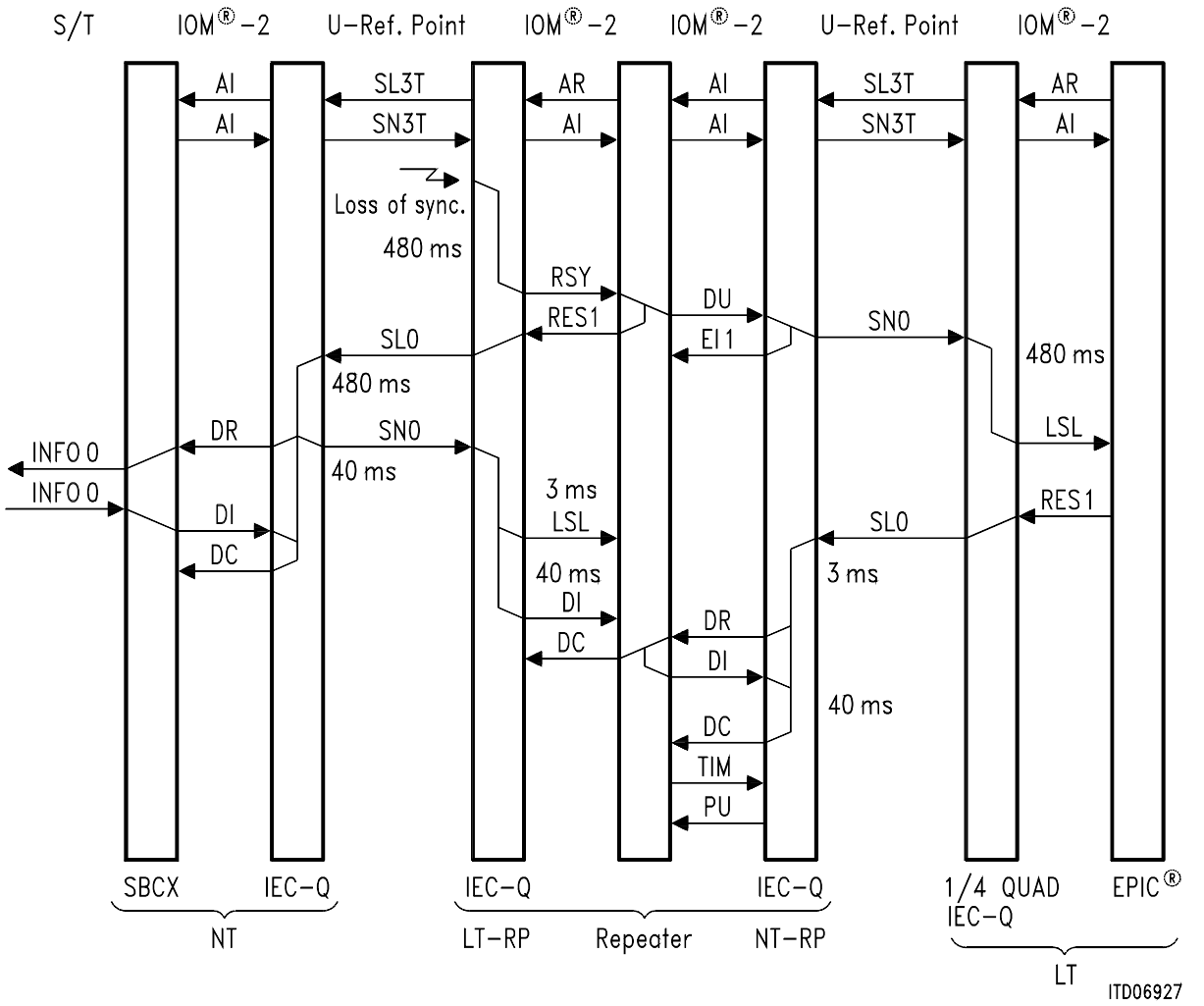
Loss of Synchronization at Repeater (LT-side)

Figure 40



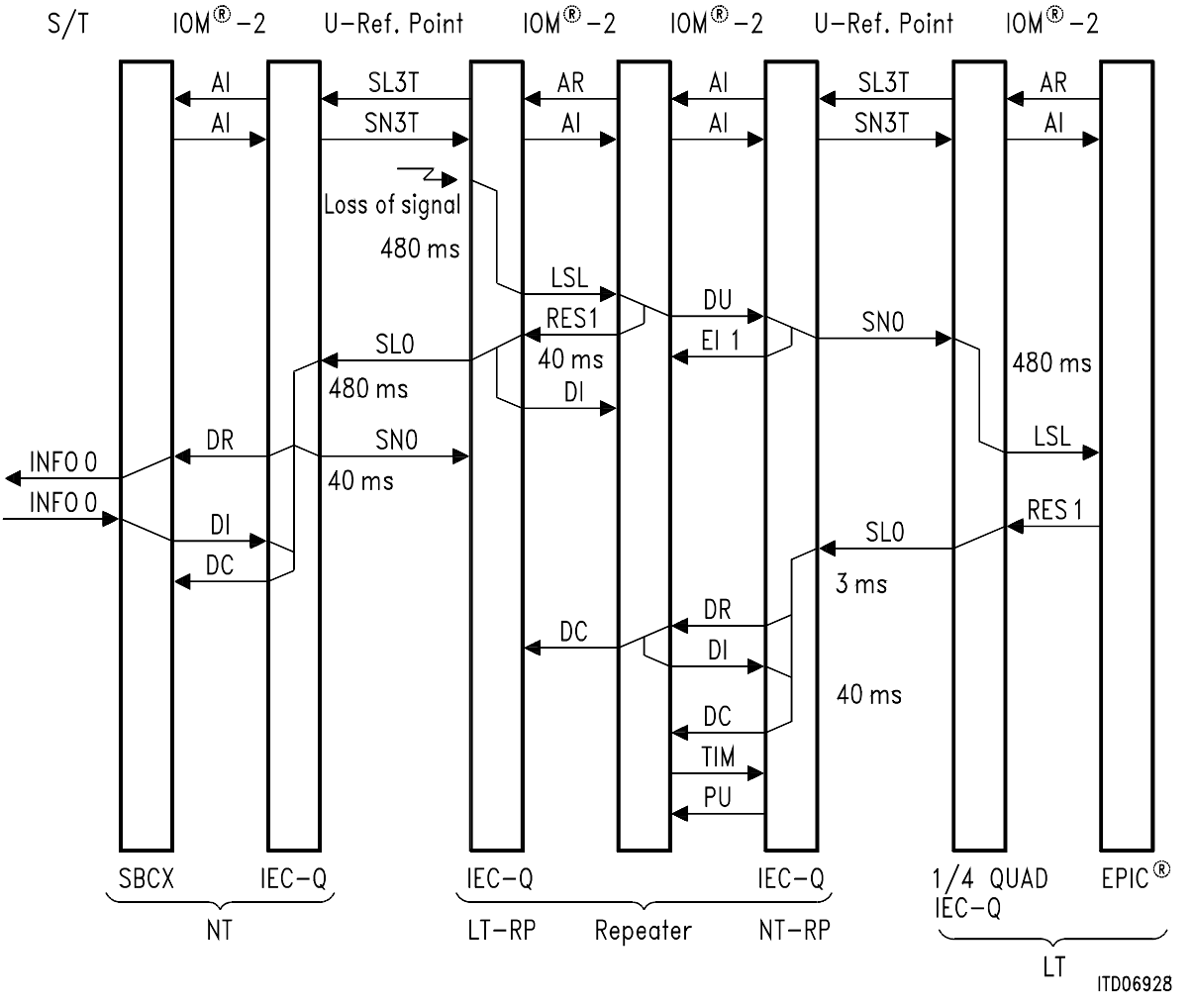
Loss of Signal at Repeater (LT-side)

Figure 41



Loss of Synchronization at Repeater (NT-side)

Figure 42



Loss of Signal at Repeater (NT-side)

2.8.13 Deactivation with Repeater

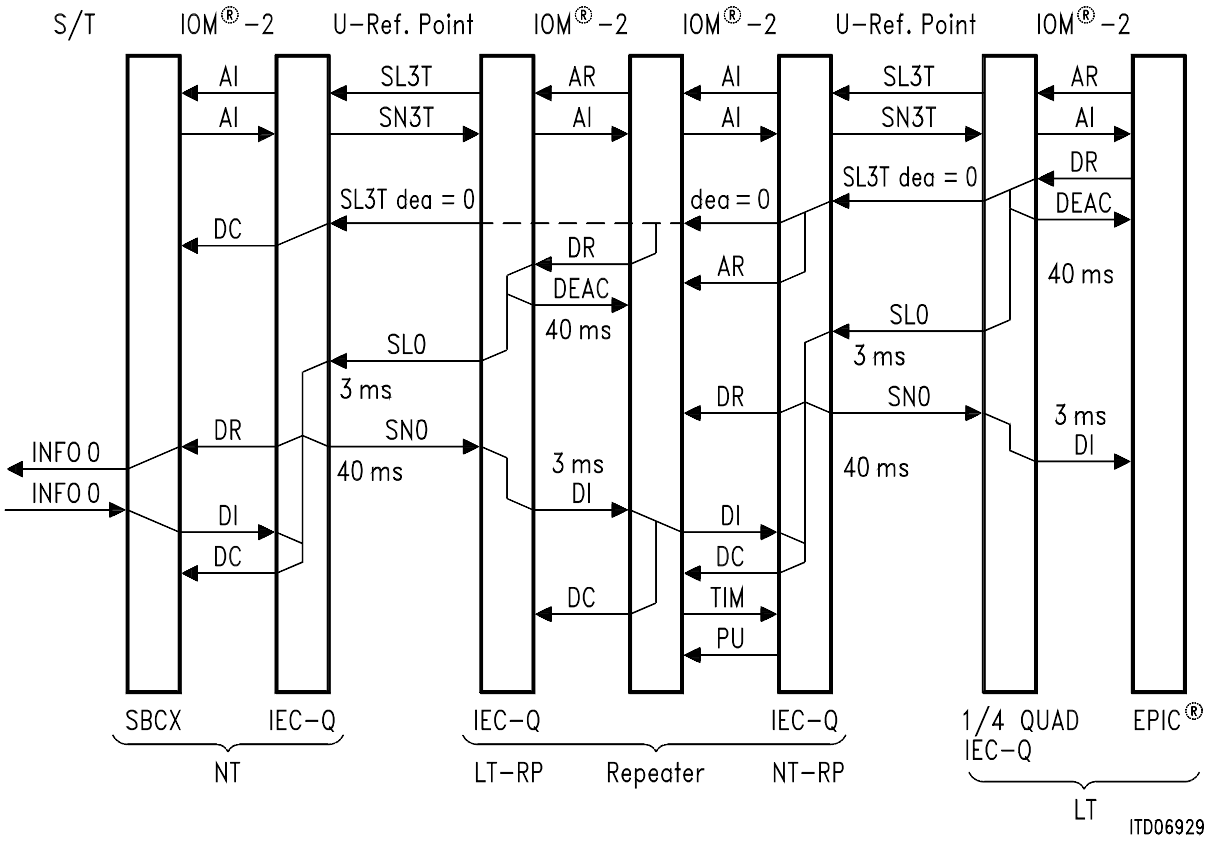


Figure 43
Deactivation with Repeater

2.9 State Machine

State machines are the key to understand start-up and tear-down behavior of the Quad IEC DFE-Q. They include all information relevant to the user and enable him to understand and predict the behavior of the Quad IEC DFE-Q. The informations contained in the state diagram are:

- state name
- U-signal transmitted
- overhead bits transmitted
- C/I-code transmitted
- transition criteria
- timers

State diagrams are interpreted as follows:

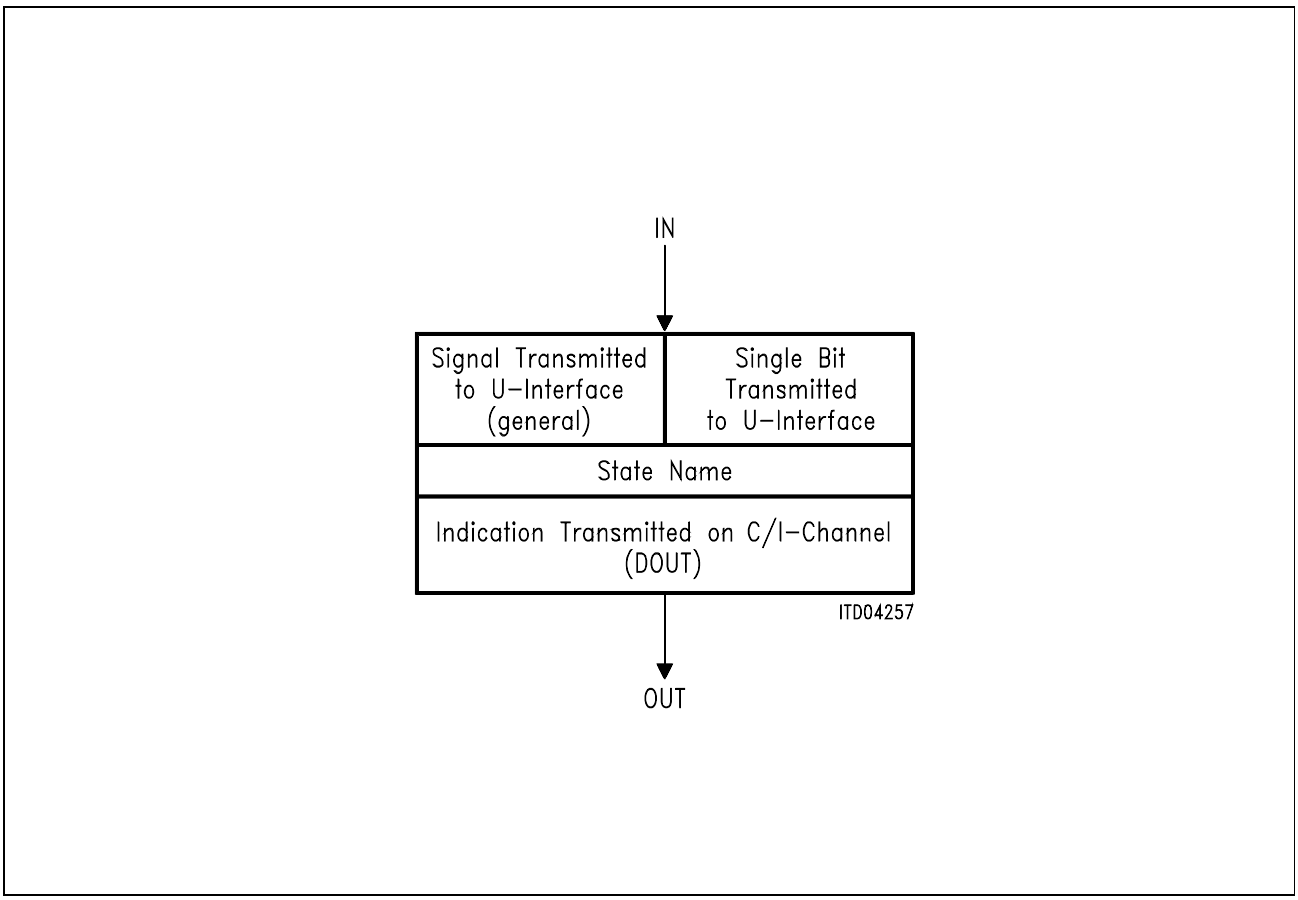


Figure 44
Explanation of State Diagram

The following example explains the use of a state diagram by an extract of the LT-state diagram. The state explained is the “Deactivated” state.

The state may be entered by either of three methods:

– from state “Receive Reset” after time T7 has expired (T7 E*xpired*)
– from state “Tear Down” after the internal transition criterion “LSU” is fulfilled
– from state “Test” after the C/I-command “DR” has been sent on DIN

The following information is transmitted:

– SL0 (no signal, see chapter 2.8) is sent on the U-interface
– no overhead bits are sent
– C/I-message “DI” is issued on DOUT

The state may be left by either of the following methods:

– Leave for state “Awake” after NT wake up tone (TN) was detected and the C/I-code DC is present on DIN
– Leave for state “Alerting” after C/I-commands “AR”, “AR0” or “UAR” were received
– Leave for state “Reset for Loop” after C/I-command “ARL” was received

Combinations of transition criteria are possible. Logical “AND” is indicated by “&” (TN & DC), logical “OR” is written “or” and for a negation “/” is used. The start of a timer is indicated with “TxS” (“x” being equivalent to the timer number). Timers are always started when entering the new state. The action resulting after a timer has expired is indicated by the path labelled “TxE”.

The section following the state diagram contains detailed information on all states and signals used.

2.9.1 LT State Diagram

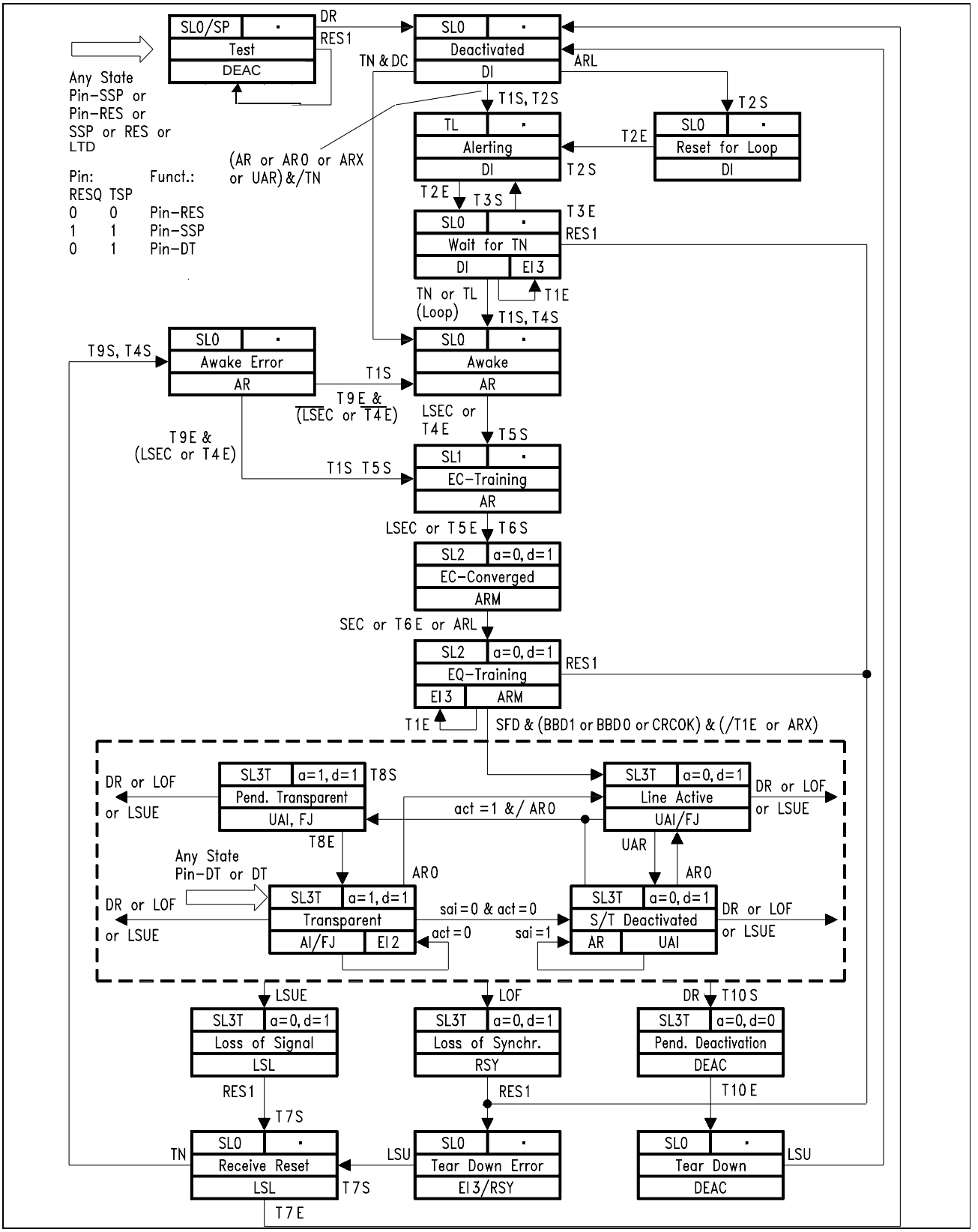


Figure 45
State Transition Diagram

2.9.2 Transition Criteria

The transition criteria used by the Quad IEC DFE-Q are described in the following sections. They are grouped into:

– C/I-commands
– Pin states
– Events related to the U-interface
– Timers

2.9.2.1 C/I-Commands

AR Activation Request
The Quad IEC DFE-Q is requested to enter the power-up state and to start an activation procedure by sending the wake-up signal TL.

AR0 Activation Request with “ACT” bit = (0)
The Quad IEC DFE-Q is requested to enter the power-up state and to start an activation procedure by sending the wake-up signal TL. After “EQ Training” the state “Line Active” will be entered independent of the “ACT” bit. Evaluation of the “ACT” bit is disabled when AR0 is received and enabled when AR is received.

ARL Activation Request Local Loop-back
The Quad IEC DFE-Q is requested to operate an analog loop-back (close to the U-interface) and to start the start-up sequence by sending the wake-up tone TL. This command may be issued only after the Quad IEC DFE-Q has been set to the “Deactivated” state (C/I-channel code DI issued on DOUT) and has to be issued continuously as long as loop-back is requested.

ARX Activation Request Extended
The Quad IEC DFE-Q is requested to enter the power-up state and to start an activation procedure by sending the wake-up signal TL. The difference to the command AR is that the Timer T1 is disabled. The activation duration may exceed 15 sec.

DC Deactivation Confirmation
If ’DC’ is applied in state “Deactivated” the Quad IEC DFE-Q transitions to state ’AWAKE as soon as it receives a wake-up tone from the NT. If ’DR’ is applied in state “Deactivated” the wake up request of the NT is not acknowledged. This way the linecard is able to reject an activation attempt by the NT e.g. during a service procedure.

By means of the ’DC’ command the LT is also during an U-only activation capable to control the point of time when the complete transmission line is set transparent in case a terminal initiated activation request has occurred. In state ’S/T Deactivated’ with applied C/I code ’UAR’ the Quad IEC DFE-Q issues ’UOA= 0’ and receives ’SAI= 0’ from the deactivated S interface. If the terminal

requests an activation with 'AR' issued in the NT the SAI bit is set to '1' and the LT indication 'UAI' switches to 'AR'. As soon as 'DC' is applied instead of 'UAR' on the LT side the line is set transparent, since the UOA bit reflects the polarity of SAI and is thus set to '1'.

DR Deactivation Request
This command requests the Quad IEC DFE-Q to start a deactivation procedure by setting the DEA bit to "0" and to cease transmission afterwards. The DR-code is a conditional command causing the Quad IEC DFE-Q only to react in the states "Test", "S/T Deactivated", "Line Active", "Pending Transparent" and "Transparent", i.e. when the C/I-channel codes DEAC, UAI, AR, AI, FJ or EI2 are issued on DOUT.

DT Data Through
This unconditional command is used for test purposes only and forces the Quad IEC DFE-Q into the transparent state independent of the wake-up protocol. A far-end transceiver needs not to be connected; in case a far-end transceiver is present it is assumed to be in the same condition.

RES Reset
Unconditional command which resets the chip channel wise; for cold start the reset code should be applied for a period of at least 8 IOM-frames (1 ms).The driver outputs are not affected by the C/I-Reset.

RES1 Reset 1
The reset 1 command resets all receiver functions; especially the EC- and EQ-coefficients and the AGC are set to zero. The RES1-code does not reset IOM-functions (e.g. monitor channel procedure or power controller interface). The RES1-code should be used when the Quad IEC DFE-Q has entered a failure condition (expiry of timer T1, loss of framing or loss of signal level) indicated by the C/I-channel EI3, RSY or LSL on DOUT. Besides resetting the receiver, this command stops transmission on the U-interface. The DEA bit is not set to "0" by RES1.

SSP Send Single Pulses
Unconditional command which requests the transmission of single pulses on the U-interface. The pulses are issued at 1.5 ms intervals and have a duration of 12.5 µs.
The chip is transferred to the "Test" state; the receiver will not be reset.

UAR Partial Activation Request (U only)
The Quad IEC DFE-Q is requested to enter power-up state and to start an activation procedure of the U-interface only.

2.9.2.2 Pins

Pins influence all four ports while C/I Codes only address the port they are issued for.

Pin-RES Pin-Reset
Corresponds to a low level at pin RESQ. The function of this pin is equivalent to sending C/I 'RES' to all chanells. The duration of the reset pulse must be 10 ns minimum. Before the reset pulse is sent the DCL clock must be applied. Additionally, the driver output pins, the interface to the AFE(SDX) and the propagation delay measurement are reset even without a running DCL clock.

Pin-SSP Pin-Send Single Pulses
Corresponds to a high level at pin TSP. The function of this pin is the same as for the C/I-code SSP. The C/I-message DEAC will be issued. The high level needs to be applied continuously for the transmission of single pulses.

Pin-DT Pin-Data Through
Entered when both RESQ and TSP are active (RESQ = "0" and TSP = "1"). The function is identical with the C/I-code DT.

2.9.2.3 U-Interface Events

ACT = 0/1 "ACT" bit received from the NT-side.

– ACT = 1 signals that the NT has detected INFO3 on the S/T-interface and indicates that the complete basic access system is synchronized in both directions of transmission. The LT-side is requested to provide transparency of transmission in both directions and to respond with setting the ACT-bit to "1". In the case of loop-backs (loop-back 2 or single-channel loop-back in the NT), however, transparency is required even when the NT is not sending ACT = 1. Transparency is achieved in the following manner:

– The Quad IEC DFE-Q performs transparency in both directions of transmission after the receiver has achieved synchronization (state EQ-training is left) independent of the status of the received ACT-bit.

– The status "ready for sending" is reached when the state transparent is entered i.e. when the C/I-channel indication AI is issued. This is valid in the case of a normal activation procedure for call control. In the case of loop-backs (loop-back 2 or single-channel loop-back in the NT and analog loop-back in the LT) however, the status "ready for sending" is reached when the state line active is entered i.e. when the C/I-channel indication UAI is issued. Until the status "ready for sending" is reached, binary "0s" have to be passed in the B- and D-channels on DIN.

– ACT = 0 indicates the loss of transparency on the NT-side (loss of framing or loss of signal level on the S/T-interface). The Quad IEC DFE-Q informs the LT-side by issuing the C/I-channel indication EI2, but performs no state change or other actions.

CRCOK Cyclic Redundancy Check OK
This input is used as a criterion that the receiver has acquired frame synchronization and both its EC and EQ coefficients have converged.

LOF Loss of Framing on the U-interface
This condition is fulfilled if framing is lost for 576 ms. 576 ms are the upper limit. If the correlation between synchronization word and input signal is not optimal, LOF can be issued earlier.

LSEC Loss of Signal Level behind the Echo Canceler
In the “Awake” state, this input is used as indication that the NT has ceased the transmission of signal SN1. In the EC-training state, this input is used as an internal signal indicating that the EC in the LT has converged.

LSU Loss of Signal Level on the U-interface
This signal indicates that a loss of signal level for the duration of 3 ms has been detected on the U-interface. This short response time is relevant in all cases where the LT waits for a response (no signal level) from the NT-side, i.e. after a deactivation procedure has been started or after loss of framing in the LT occurred.

LSUE Loss of Signal Level on the U-interface (error condition)
After a loss of signal level has been noticed, a 492 ms timer is started. After this timer has elapsed, the LSUE-criterion is fulfilled. This long response time (see also LSU) is valid in all cases where the LT is not prepared to lose signal level. Note that 492 ms represent a minimum value; the actual loss of signal might have occurred earlier, e.g. when a long loop is cut at the LT-side, the echo coefficients need to be readjusted to new parameters. Only after the adjusted coefficient cancel the echo completely, the loss of signal is detected and the timer can be started (if the long loop is cut at the remote end, the coefficients are still correct and a loss of signal will be detected immediately).

SEC Signal Level behind the echo canceler
This signal indicates that a signal level corresponding to SN2 from the NT has been detected on the U-interface.

SFD Superframe Detected

TN Tone (wake-up signal) received from the NT.
When in the “Deactivated” state, the Quad IEC DFE-Q is requested to start an activation procedure and to inform the LT-side making use of the C/I-channel code AR. When in the “Wait for TN” state, the signal TN sent by the NT acknowledges the receipt of a wake-up signal TL from the LT.
When an analog loop-back is operated, the wake-up signal TL sent by the LT-transmitter is detected by the LT-receiver.

The TN-criteria is fulfilled when 12 consecutive periods of the 10 kHz wake-up tone were detected.

BBD0/1 Binary “0” or “1s” detected in the B- and D-channels
This internal signal indicates that for a period of time of 6–12 ms a continuous stream of binary “0s” or “1s” has been detected. It is used as a criterion that the receiver has acquired frame synchronization and both its EC- and EQ-coefficients have converged. BBD1 corresponds to the signals SN2 or SN3 in the case of a normal activation and BBD0 corresponds to the internally received signal SL2 in the case of an analog loop-back or possibly a loop-back 2 in the NT.

2.9.2.4 Timers

The start of timers is indicated by TxS, the expiry by TxE. The following **table 23** shows which timers are used:

Table 23
Timers Used in LT-Modes

Timer	Duration (ms)	Function	State
T1	15000	Supervisor for start-up	
T2	3	TL-transmission Receiver reset	Alerting Reset for loop
T3	40	Re-transmission of TL	Wait for TN
T4	6000	Supervisor SN0 detect	Awake
T5	1000	Supervisor EC converge	EC training
T6	6000	Supervisor SN2 detect	EC converge
T7	40	Hold time	Receiver reset
T8	24	Delay time for AI detection	Pend. transparent
T9	40	Hold time	Awake error
T10	40	“DEA” = (0) transmission	Pend. Deactivation

2.9.3 Transmitted Signals and Indications

Signals and indications are issued on the IOM-2-interface (C/I-codes) and U-interface (predefined U-signals).

2.9.3.1 C/I-Indications

AI Activation Indication
This indication signals that “ACT” = 1 has been received and that timer T8

has elapsed. This indication is not issued in case AR0 is applied to DOUT or an analog loop-back is operated.

AR — Activation Request
The AR-code signals that a wake-up signal has been received and that a start-up procedure has commenced. Receiver synchronization has not yet been achieved.
When already partially active (U only activation), AR indicates that the “SAI” bit was set to (1), i.e. the S/T-interface has become active.

DEAC — Deactivation
This indication is issued in response to a DR-code (Pend. Deactivation, Tear Down) and in the “Test” state (unless PFOFF is active, i.e. PS1 = (1)).

DI — Deactivation Indication
Idle code on the IOM-interface. Normally the Quad IEC DFE-Q stays in the “Deactivated” state unless an activation procedure is started by the NT-side.

EI2 — Error Indication 2
EI2 is issued if the received ACT-bit is (0). The NT receiver indicates a loss of signal or framing on the S/T-interface by setting the upstream ACT-bit to (0). The Quad IEC DFE-Q remains in the “Transparent” state. After a signal level or framing is detected again, the C/I-indication AI will be issued anew.

EI3 — Error Indication 3
This indication is issued when the Quad IEC DFE-Q has not been able to activate successfully (expiry of timer T1).

LSL — Loss of Signal Level
The Quad IEC DFE-Q has entered a failure condition after loss of signal level (LSUE).

RSY — Re-Synchronization indication after a loss of framing (LOF)
For EI3, LSL and RSY indication the LT-side should react by applying the C/I-channel code RES1 to allow the Quad IEC DFE-Q to enter the “Receive reset” state and to reset the receiver functions.

FJ — Frame Jump
This indication signals that either a data buffer overflow/underflow has been detected or a phase jump of one of the IOM-timing signals DCL or FSC has occurred. The FJ-code is issued for a period of 1.5 ms.

UAI — U-Activation Indication
The UAI-code signals that the line system is synchronized in both directions of transmission (see also the input ACT = 1). Maintenance bits are transmitted normally.

ARM Activation Request Maintenance
Transmission of maintenance bits is possible.

2.9.3.2 Signals on U-Interface

The signals SLx, TL and SP transmitted on the U-interface are defined in section **2.8**. The polarity of the overhead bits ACT and DEA is indicated as follows:

a = 0/1 corresponds to ACT bit set to binary “0/1”.
d = 0/1 corresponds to DEA bit set to binary “0/1”.

The polarity of the transmitted UOA-bit depends on the received C/I-channel code:

– UAR sets UOA-bit to binary 0.
– AR sets UOA-bit to binary 1.
– Any other C/I-codes sets the UOA to the same value as the received SAI bit. After deactivation the UOA-bit is set to binary 0 until a valid SAI-bit is received.

2.9.4 States

This section describes the functions of all states.

Alerting

The wake-up signal TL is transmitted for 3 ms (T2) in response to an activation request from the LT side (AR or ARL). In the case of an analog loop-back, the signal TL is forwarded internally to the wake-up signal detector and stored.

Awake

The “Awake” state is entered upon the receipt of a wake-up or an acknowledge signal TN from the NT. In the case of an activation started by the LT-side, timer T1 is restarted when the “Awake” state is entered.

Awake Error

The “Awake Error” state is equivalent to the “Awake” state, but is entered only when a wake-up signal is received while being in the “Receive reset” state. As the “Receive reset” state was entered upon the application of the C/I-channel code RES1, the “Awake error” state assures that a minimum amount of time elapses between the application of the RES1-code and the Quad IEC DFE-Q entering a state (EQ training) in which it again reacts on the RES1-code. The LT-side is requested to stop issuing the command RES1 within T9 after the receipt of the C/I-channel code AR on DOUT and to replace it by another command such as the idle code DC for instance.

Deactivated (Full Reset)

In the “Deactivated” state the device may enter the low power consumption condition. The power-down mode is entered if no monitor messages are to be expected. In power-down the receiver and parts of the interface are deactivated while functions related to the IOM-2-interface and the wake-up detector are still active.
No signal is sent on the U-interface, the differential outputs AOUT and BOUT are set to 0 V. The Quad IEC DFE-Q waits for a wake-up signal TN from the NT-side or an activation request (AR, AR0, UAR or ARL) from the LT-side to start an activation procedure.

For the recognition of the wake-up signal TN the following procedure applies:

– TN detected for 4 periods –> transfer within the “Deactivated” state into power-up
– In power-up both differential outputs are set to 3.2 V
– TN detected for a total of 12 consecutive periods –> transition criterion TN fulfilled, change to next state, if in addition the C/I-command DC is given on DIN.
– TN detected for more than 4 but less than 12 periods –> return to power-down

The input sensitivity stated in chapter “Electrical Characteristics” presents the minimum level required to meet the TN transition criterion. The power-up condition may thus already be entered at a lower level.

EC Converged

Upon the EC-coefficients having converged, the Quad IEC DFE-Q starts the transmission of signal SL2 and waits for the receipt of signal SN2 from the NT (SEC). If no signal is detected within T6, nevertheless the start-up procedure will be continued. In the case of an analog loop-back, this state is left immediately because the EC compensates for the looped back transmit signal.

EC-Training

The signal SL1 is transmitted on the U-interface to allow the LT-receiver to update its EC-coefficients. The “EC-training” state is left when the EC has converged (LSEC) or when timer T5 has elapsed. Timer T5 allows the start-up procedure to proceed even if LSEC due to a high noise level on the U-interface for instance, could not be detected.

EQ-Training

The “EQ-Training” is left after the receiver has achieved synchronization and the superframe indication has been detected (SFD). Upon expiry of timer T1 the C/I-channel indication EI3 is issued.

Line Active

In the “Line Active” state, the Quad IEC DFE-Q transmits transparently in both directions. The U-Interface is synchronized and the maintenance channel is operational. The Quad IEC DFE-Q stays in the line-active state

– during a normal activation procedure while the “ACT” bit = (0) is received
– when an analog loop-back is established
– while C/I-command AR0 is applied to DIN

In the case of normal activation with call control, binary “0s” have to be applied to the B and D channels on the IOM-interface. After the C/I-channel indication UAI has been issued, the layer-2 receiver should be fully operational to prevent the first layer-2 message issued by the NT-side upon the receipt of the ALI-code in the TE, to be lost.

Loss of Signal

The “Loss of Signal” state is entered upon the detection of a failure condition i.e. loss of receive signal (LSUE). The ACT bit is set to “0” and the C/I-channel indication LSL is issued. The Quad IEC DFE-Q waits for the C/I-channel command RES1 to enter the “Receive Reset” state.

Loss of Synchronization

The “Loss of Synchronization” state is entered upon the detection of a failure condition i.e. loss of framing by the LT-receiver (LOF). The ACT-bit is set to “0” and the C/I-channel indication RSY is issued. The Quad IEC DFE-Q waits for the C/I-channel command RES1 to enter the “Tear Down Error” state and subsequently the “Receive Reset” state.

Pending Deactivation

“Pending Deactivation” is a transient state entered after the receipt of a DR-code. The DEA-bit is set to “0”. Timer T10 assures that the DEA-bit is set to “0” in at least three consecutive superframes before the transmit level is turned off.

Pending Transparent

“Pending Transparent” is a transient state entered upon the detection of ACT = 1 and left by T8. The ACT-bit is set to “1”. The purpose of this state is to issue the C/I-channel indication AI (corresponding to “ready for sending”) 24 ms after the ACT-bit has been set to “1” by the LT-transceiver. This assures that under normal operating conditions the AI-indication is issued first on the TE-side and only afterwards on the LT-side. Thus the layer-2 receiver in the TE is already operational when the first layer-2 message is issued by the LT-side.

Reset for Loop

"Reset for Loop" resets the receiver in order to guarantee a correct adaption of the echo- and equalizer coefficients.

Receive Reset

The "Receive Reset" state assures that for a period of T7 no signal, especially no wake-up signal TL, is sent on the U-interface, i.e. no activation procedure is started from the LT-side. A wake-up signal TN, however, from the NT-side is acknowledged.

S/T Deactivated

The state "S/T Deactivated" will be entered if the received ACT- and SAI-bits are set to (0). In this state the signal SL3T, ACT = (0), DEA = (1) and UOA = (0) are transmitted downstream. On the IOM-2-bus the C/I-code UAI is issued while the received SAI = (0). In order to initiate a complete activation from the S/T deactivation state, the LT needs to set the UOA-bit to (1). This will occur if either of the following three conditions are met:

– C/I = AR(LT-activation)
– SAI = (1) & AR(TE-activation with exchange control [DIN = C/I UAR])
– SAI = (1)(TE-activation without exchange control [DIN = C/I DC])

"S/T deactivated" will be left if the received ACT bit is (1), or the C/I code AR0 is applied.

Tear Down

In "Tear Down" state, transmission ceases in order to deactivate the basic access, and the Quad IEC DFE-Q waits for a response (no signal level, LSU) from the NT-side.

Tear Down Error

"Tear Down Error" state is entered after loss of framing has been detected. Transmission ceases in order to deactivate the basic access and the Quad IEC DFE-Q waits for a response (no signal level, LSU) from the NT-side. EI3-indication is transmitted after a transition forced by RES1 from the wait-for-TN or EQ-training states. In the case of transition from the "Loss of synchronization" state RSY is sent.

Test

This "Test" mode is entered when the unconditional commands RES, SSP, Pin-RES or Pin-SSP are used. It is left when the pins RESQ and TSP are inactive and the C/I-channel code DR is received. The output signals are as follows:

– when the C/I-channel code RES or RES1 is applied or when the pin RESQ is activated:
  SL0 and DEAC
– when the C/I-channel code SSP is applied or when the pin TSP is activated:
  single pulses (SP) and DEAC

In this state the Quad IEC DFE-Q does not react to the receipt of a wake-up signal TN.

Transparent

This “Transparent” state corresponds to the fully active state in the case of a normal activation for call control. It may also be entered in the case of a loop-back 2 if the NT issues ACT = 1 or in case of a single-channel loop-back in the NT. The LT-side is informed that the status “ready for sending” is reached (indication AI). If the NT-side loses transparency (receipt of ACT = 0), the LT-side is informed by making use of the C/I-channel indication EI2, but no state change is performed. If the S/T-interface is deactivated (SAI = (0) & ACT = (0)), the device is transferred to the S/T deactivated state.

Wait for TN

In “Wait for TN” the Quad IEC DFE-Q waits for a response (tone TN from the NT or tone TL in case of an analog loop-back) to the transmission of the wake-up signal TL. If no response is received within T3, the state is left for re-transmission of a wake-up tone TL. This procedure is repeated until the detection of tone TN or until expiry of timer T1. In this case the C/I-channel indication EI3 is issued, but no state change is performed.

2.10 Maintenance Functions

This chapter summarizes all features provided by the Quad IEC DFE-Q to support maintenance functions and system measurements. Three main groups may be distinguished:

– maintenance functions to close and open test loop-backs
– features facilitating the recognition of transmission errors
– test modes required for system measurements

A fourth group yields information about the access to internal chip data. As a use of this feature requires very detailed knowledge about the internals of the Quad IEC DFE-Q, only in few cases these informations will be of practical relevance to the user.

2.10.1 Test Loop-Backs

Test loop-backs are specified by the national PTTs in order to facilitate the location of defect systems. Four different loop-backs are defined. The position of each loop-back is illustrated in **figure 46.**

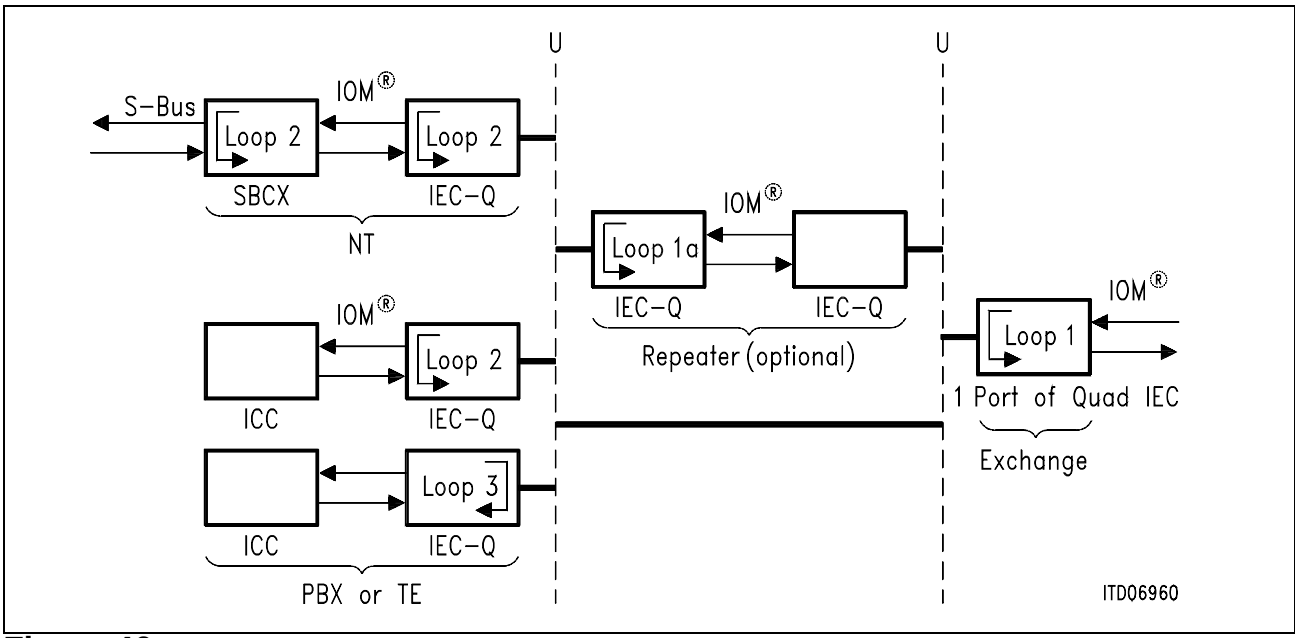


Figure 46
Test Loop-Backs

Loop-backs #1, #1A and #2 are controlled by the exchange. Loop-back #3 is controlled by the terminal. All four loop-back types are transparent. This means all bits that are looped back will also be passed onwards in the normal manner.

The next sections describe how loop-backs #1 and #2 are closed and opened using the C/I- and MON-commands available to the Quad IEC DFE-Q. Loopback #1A and #3 are not in the scope of the Quad IEC DFE-Q.

2.10.1.1 Analog Loop-Back (No.1 / No. 1a/ No. 3)

Loop-back #1 is initiated by the Quad IEC DFE-Q . It is closed by the ESCC8 as near to the U-interface as possible. For this reason it is also called analog loop-backs. All analog signals will still be passed on to the U-interface. This results in the opposite station to be activated as well.

Before an analog loop-back is closed with the C/I-command ARL (activation request loop-back), the device must have been reset.

In order to open an analog loop-back correctly, reset the device into the TEST state with the C/I-command RES (or by pin reset). This ensures that the echo coefficients and equalizer coefficients will converge correctly when activating the following time.

The example below demonstrates the use of loop-backs #1.

Loop-back #1 (LT-side)

NT IOM-2 LT IOM-2

<------	C/I DC	(1111b)	C/I DI	(1111b)	------>	
			C/I ARL	**(1010b)**	**<------**	; Close loop-back #1
<------	C/I AR	(1000b)	C/I AR	(1000b)	------>	; Activation proceeds in NT
			C/I ARM	(1001b)	------>	; and LT
			C/I UAI	(0111b)	------>	; Activation complete, ; #1 closed
			C/I RES	**(0001b)**	**<------**	; Open loop-back #1, ; reset the Quad IEC DFE-Q

Function

The analog loop may be closed in three different locations: in the LT (No.1), in the repeater (No. 1a), and in the NT-PBX or TE (No.3) see **Fig. 36**. The loop is closed at the U-interface. The 6 dB range attenuation in the ESCC8 is active. Only loop #1 and 1A are supported by the Quad IEC DFE-Q.

Initialization

Before loops No.1, No.1A or No. 3 may be closed, a master reset is required. Loops No. 1 and No. 1a are closed in the “Deactivated” state. Loop No. 3 is started from the “Test” state. All analog loops are closed with the C/I-command ARL. This command must be issued continuously while the loop-back is required.

Transparency

Only the internal loop-back signal is processed; signals on the receive pins are ignored. For this reason the device stays in the “Line Active” state for loops No. 1 and No. 1a (upstream ACT-bit cannot be received).
All transmitted signals (IOM –> U) are passed on to the U-interface transparently.

2.10.1.2 Partial and Complete Loop-Back (No. 2)

For loop-back #2 several alternatives exist. Both the type of loop-back and the location may vary. Three loop-back types belong to the loop-back-#2 category:

– Complete loop-back
– B1-channel loop-back
– B2-channel loop-back

The complete loop-back comprises both B-channels and the D-channel. It may be closed either in the NT IEC-Q itself or in a downstream device. Single-channel loop-backs are always performed within the IEC-Q at the NT side. In this case the digital data of DOUT will be directly fed back into DIN. This also applies if the complete loop-back is closed in the NT IEC-Q.

Normally loop-back #2 is controlled from the exchange. The EOC monitor commands LBBD, LB1 and LB2 are used. They will be recognized and executed automatically in the NT IEC-Q if the auto-mode is selected. Alternatively (e.g. when NT operates in transparent mode) MON-8-commands are available. Refer to the PEB 2091 user's manual for further details on the operation of NTs.

All loop-back functions are latched. This allows channel B1 and channel B2 to be looped back simultaneously. All loop-backs are opened when the EOC command RTN or the MON-8-command NORM is sent.

2.10.1.2.1 Complete Loop-Back

When receiving the EOC-command LBBD in auto-mode, the NT IEC-Q does not close the loop-back immediately. Because the intention of this loop-back is to test the complete NT, the IEC-Q passes the complete loop-back request on to the next downstream device (e.g. SBCX). This is achieved by issuing the C/I-code AIL in the "Transparent" state or C/I = ARL in states different than "Transparent". If the downstream device is not able to close the complete loop-back, a MON-8-message LBBD may be returned to the NT IEC-Q. This then will close the complete loop-back within the IEC-Q itself (B1 + B2 + D-channels). All remaining IOM-information (monitor, C/I-channel as well as the bits MR and MX) are still read from the IOM-2-interface. For this reason it is still possible for a layer-2 device to deactivate the NT despite the fact that the loop-backs are controlled by the exchange.

Figure 47 illustrates these two options.

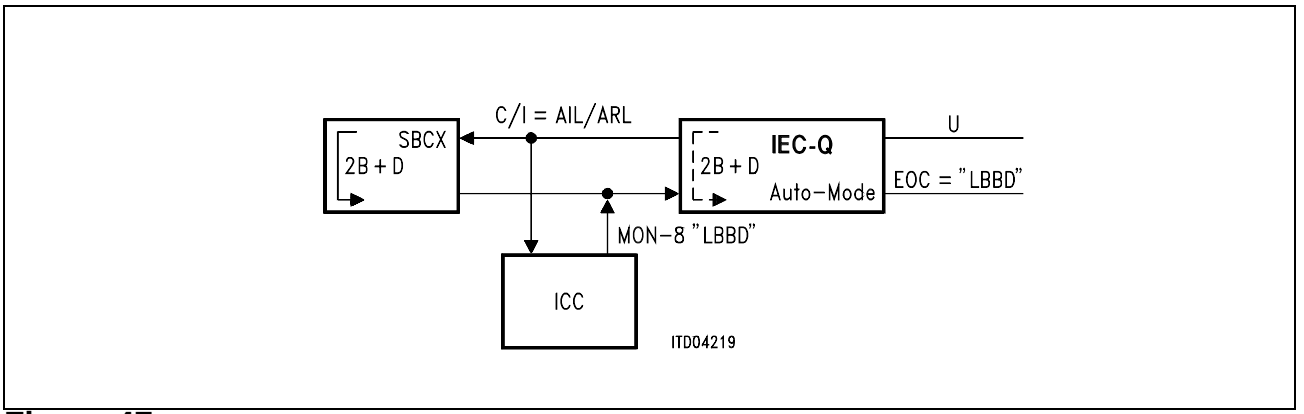


Figure 47
Complete Loop-Back Options in the NT

Note: *If operated in auto-mode, the complete loop-back can only be closed in the IEC-Q if previously the EOC-command LBBD was received. Without this EOC-message the MON-8-command LBBD will be ignored.*
If operated in transparent mode, a complete loop-back may be closed at any time with MON-8 LBBD.

Complete Loop-Back in NT-Auto-Mode:

In auto-mode the complete loop-back is reset after RTN has been received in the EOC-channel. In transparent mode MON-8 NORM is used for this purpose. No reset as for loop-backs #1 or #3 is required for loop-back #2. The line is active and ready for data transmission.

The typical procedure for closing and opening a complete loop-back is demonstrated in the examples below.

	NT IOM-2			LT IOM-2			
				C/I AR	(1000b)	<------	; U-interface is activated
<------	C/I AR	(1000b)		C/I UAI	(0111b)	------>	; without terminal
							; confirmation
(------>	C/I AI	(1100b)					; or with
<------	C/I AI	(1100b)		C/I AI	(1100b)	------>	; terminal confirmation)
				MON-0 LBBD (50_H)		**<------**	;Close complete loop (EOC)
<------	C/I AIL	(1110b)					; Request for downstream
<------	MON-0 LBBD (50_H)						; device to close complete
							; loop-back
				MON-0 LBBD (50_H)		------>	; Receive acknowledgment
------>	**[MON-8 LBBD ($F1_H$)]**						; If downstream device can't
							; close, loop is closed in IEC
				MON-0 RTN (FF_H)		**<------**	; Open all loop-backs
<------	MON-0 RTN (FF_H)						; All loop-backs opened
				MON-0 RTN (FF_H)		------>	; Receive acknowledgment

In the above example the LT is operated in auto-mode.

Complete Loop-Back in Transparent NT-Mode:

	NT IOM-2		LT IOM-2			
------>	C/I AI	(1100b)	C/I AR	(1000b)	<------	; U-interface is activated
<------	C/I AI	(1100b)	C/I AI	(1100b)	------>	
			MON-0 LBBD (50_H)		<------	; Close complete loop (EOC)
<------	MON-0 LBBD (50_H)					; Request passes DFE-Q ; transparent
------>	**MON-0 LBBD (50_H)**		MON-0 LBBD (50_H)		------>	; Transmit acknowledgment
------>	**MON-8 LBBD ($F1_H$)**					; Close complete loop in IEC
			MON-0 RTN (FF_H)		<------	; Request to open all loops
------>	**MON-0 RTN (FF_H)**		MON-0 RTN (FF_H)		------>	; Receive acknowledgment
------>	**MON-8 NORM (FF_H)**					; Open all loop-backs

In the above example the LT is operated in auto-mode.

2.10.1.2.2 Single-Channel Loop-Backs

Single-channel loop-backs are always performed directly in the NT IEC-Q. No difference between the B1-channel and the B2-channel loop-back control procedure exists. They are therefore discussed together.

In auto-mode the B1-channel is closed with the EOC-command LB1. LB2 causes the channel B2 to loop-back. Because these functions are latched, both channels may be looped back simultaneously by sending first the command to close one channel followed by the command for the remaining channel.

Single-channel loop-backs are resolved in the same manner as described for the complete loop-back. The NT may be deactivated with layer 2 while single loop-backs are closed.

Single-Channel Loop-Back in NT-Auto-Mode:

	NT IOM-2		LT IOM-2			
------>	C/I AI	(1100b)	C/I AR	(1000b)	<------	; U-interface is activated
<------	C/I AI	(1100b)	C/I AI	(1100b)	------>	
			MON-0 LB1 (51_H)		<------	; Close B1 loop (EOC)
<------	MON-0 LB1 (51_H)					; Loop B1 closed
			MON-0 LB1 (51_H)		------>	; Receive acknowledgment
			MON-0 LB2 (52_H)		<------	; Close B2 loop-back (EOC)
<------	MON-0 LB2 (52_H)					; Loop-back B1 and B2 ; closed
			MON-0 LB2 (52_H)		------>	; Receive acknowledgment
			MON-0 RTN (FF_H)		<------	; Open all loop-backs
<------	MON-0 RTN (FF_H)					; All loop-backs opened
			MON-0 RTN (FF_H)		------>	; Receive acknowledgment

In the above example the LT is operated in auto-mode.

Single-Channel Loop-Back in NT-Transparent Mode:

	NT IOM-2		LT IOM-2			
------>	C/I AI	(1100b)	C/I AR	(1000b)	<------	; U-interface is activated
<------	C/I AI	(1100b)	C/I AI	(1100b)	------>	
			MON-0 LBBD (51_H)		<------	; Close B1 loop (EOC)
<------	MON-0 LB1 (51_H)					; Request passes DFE-Q ; transparent
------>	**MON-0 LB1 (51_H)**		MON-0 LBBD (51_H)		------>	; Transmit acknowledgment
------>	**MON-8 LB1 ($F4_H$)**					; Close B1 loop in IEC
			MON-0 LBBD (52_H)		<------	; Close B2 loop (EOC)
<------	MON-0 LB2 (52_H)					; Request passes DFE-Q ; transparent
------>	**MON-0 LB2 (52_H)**		MON-0 LB2 (52_H)		------>	; Transmit acknowledgment
------>	**MON-8 LB2 ($F2_H$)**					; Close B2 loop in IEC ; B1 and B2 closed
			MON-0 RTN (FF_H)		<------	; Request to open all loops
------>	**MON-0 RTN (FF_H)**		MON-0 RTN (FF_H)		------>	; Receive acknowledgment
------>	**MON-8 NORM (FF_H)**					; Open all loop-backs

In the above example the LT is operated in auto-mode.

For a quick reference the key characteristics of the „Partial and Complete Loop-Back“ are summarized on the following pages.

Function

Loop No. 2 comprises three options: Loop-back of channel B1 only, loop-back of channel B2 only or loop-back of channels B1 + B2 + D (complete loop). Loop-backs of channels B1 or B2 are always performed in the Quad IEC DFE-Q itself. A complete loop may be closed alternatively in the Quad IEC DFE-Q or in the downstream device. When issuing several commands all commands will be executed simultaneously i.e. channel B1 and channel B2 can be looped-back at the same time.

All loop variations are closed as near to the IOM-interface as possible.

Initialization

The procedure for closing loop No. 2 differs, depending on the selected processing mode.

Auto-Mode

Single-channel loop-backs are closed from the LT-side with the MON-0-commands “LB1” (channel B1) and “LB2” (channel B2). Due to the automatic acknowledgment in auto-mode, the EOC-message will be mirrored back immediately by the NT as a confirmation.

Note: *This confirmation is issued before the loop-back function is initialized. Therefore it cannot be regarded as an acknowledgment that the loop-back function was started correctly.*

Initialization

MON-0							LB1	Close loop-back in B1-channel							
0	0	0	0	0	0	0	1	0	1	0	1	0	0	0	1

Acknowledgment (issued on LT- and NT-side)

MON-0							LB1	Close loop-back in B1-channel							
0	0	0	0	0	0	0	1	0	1	0	1	0	0	0	1

Initialization

MON-0							LB2	Close loop-back in B2-channel							
0	0	0	0	0	0	0	1	0	1	0	1	0	0	1	0

Acknowledgment (issued on LT- and NT-side)

MON-0							LB2	Close loop-back in B2-channel							
0	0	0	0	0	0	0	1	0	1	0	1	0	0	1	0

Complete loops are closed with a single MON-0-command from LT-side (loop-back not in Quad IEC DFE-Q itself) or a combination of MON-0 (LT-side) and MON-8 (NT-side) commands. Refer to section 2.10.1 “Complete Loop-Back”. With respect to the command acknowledgment received, the aforesaid applies to complete loop requests, too.

Close complete loop not in Quad IEC DFE-Q

Initialization (LT-side)

MON-0							LBBD
0	0	0	0	0	0	0	1

Close loop-back 2B + D							
0	1	0	1	0	0	0	0

Acknowledgment (issued on LT- and NT-side)

MON-0							LBBD
0	0	0	0	0	0	0	1

Close loop-back 2B + D							
0	1	0	1	0	0	0	0

Close complete loop in Quad IEC DFE-Q

Initialization (LT-side)

MON-0							LBBD
0	0	0	0	0	0	0	1

Close loop-back 2B + D							
0	1	0	1	0	0	0	0

Acknowledgment (issued on LT- and NT-side)

MON-0							LBBD
0	0	0	0	0	0	0	1

Close loop-back 2B + D							
0	1	0	1	0	0	0	0

Close loop in IEC-Q (NT-side)

MON-0							LBBD
1	0	0	0	0	0	0	0

Close loop-back 2B + D							
1	1	1	1	0	0	0	1

Transparent Mode

Single-channel and complete loop-backs are closed from the NT-side with the MON-8-commands “LB1” (channel B1), “LB2” (channel B2), and “LBBD” (2B + D). This is only possible if the device is operating in transparent mode. In auto-mode the commands will be ignored (with the exception “LBBD”; see auto-mode above). Normally MON-8-looping commands are used in response to an EOC-loop-back request (MON-0-message).

Initialization (NT-side)

No acknowledgment issued.

MON-8 LB1

1	0	0	0	0	0	0	0

Close loop-back in B1-channel

1	1	1	1	0	1	0	0

Initialization (NT-side)

MON-8 LB2

1	0	0	0	0	0	0	0

Close loop-back in B2-channel

1	1	1	1	0	0	1	0

No acknowledgment issued.

Initialization (NT-side)

MON-8 LBBD

1	0	0	0	0	0	0	0

Close loop-back in 2B + D

1	1	1	1	0	0	0	1

No acknowledgment issued.

Transparency

Except for the channels looped-back, all IOM-data received on DIN is passed transparently upstream. This allows a deactivation of the NT despite of closed test loop-backs.

Data sent downstream will be passed on completely (independent of closed loop-backs) to the IOM-interface (DOUT).

2.10.1.3 Repeater Loop-Back (No. 1A)

Loop-back #1A is always closed in the repeater. Functionally it corresponds to loop-backs #1 and #3 on the exchange and on the network side. If a line contains more than one repeater unit, it is possible to address each unit individually in order to close loop-back #1A in the specified unit only.

For loop-back #1A everything described in section 3.3.1 (Analog Loop-Back) applies: The loop-back is opened with the C/I-command RES, closed with the C/I-command ARL, and it is closed as near to the U-interface as possible. The difference results from the fact that the command ARL needs to be generated by the repeater control unit (µP system or ASIC) according to national repeater specifications.

This specification defines an EOC-command which will activate loop-back #1A if received in conjunction with the repeater address (001b). The NT-RP is operating in transparent mode. The repeater control unit watches for MON-0-commands with address (001b). If the predefined loop-back #1A command is received, the repeater control unit sends the C/I-code ARL to the LT-RP and loop-back #1A will be closed.

In case the address (000b) or (111b) (NT and broadcast address) is received, the control unit ignores all MON-0-commands and leaves the address unchanged.

Should the address read (010b) to (110b), the MON-0-command will be ignored but the address will be decremented. This procedure is described in **section 2.1.3.2** (EOC-Programming) and allows individual repeater addressing.

Figure 48 illustrates this in a system with two repeater units where the second unit is requested to close loop-back #1A.

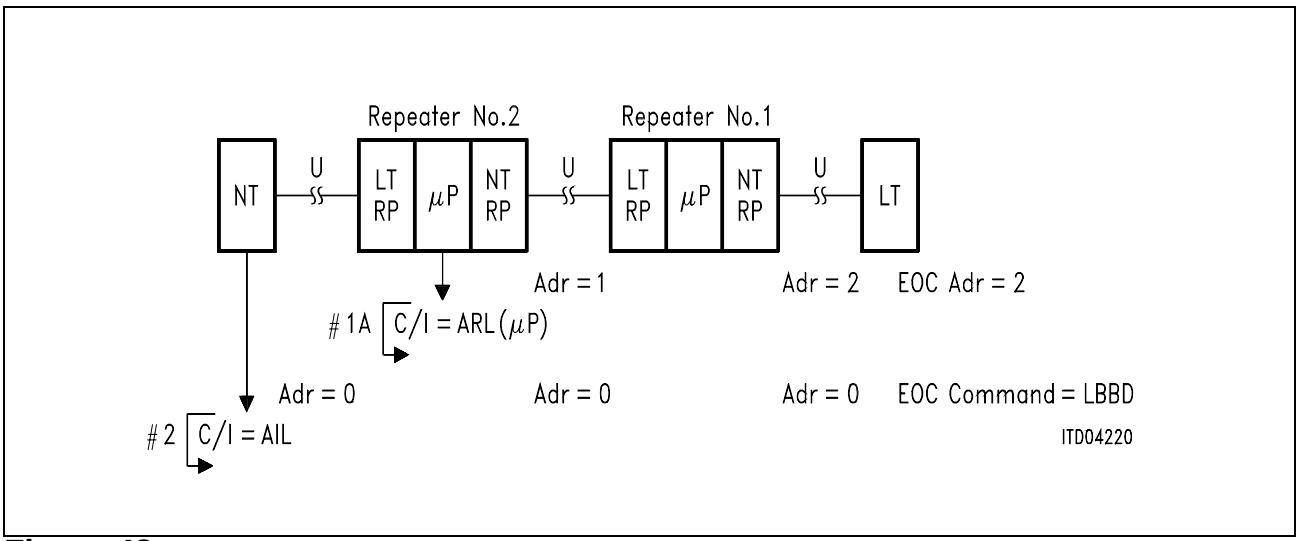


Figure 48
Closing Loop-Back #1A in a Multi-Repeater System

2.10.2 Block Error Counters

The Quad IEC DFE-Q provides internal counters for far-end and near-end block errors. This allows a comfortable surveillance of the transmission quality at the U-interface. In addition, MON-messages indicate the occurrence of near-end errors, far-end errors, and the simultaneous occurrence of both errors.

A block error is detected each time when the calculated checksum of the received data does not correspond to the control checksum transmitted in the successive superframe. One block error thus indicates that one U-superframe has not been transmitted correctly. No conclusion with respect to the number of bit errors is therefore possible.

The following two sections describe the operation of near and far-end block error counters as well as the commands available to test them.

2.10.2.1 Near-End and Far-End Block Error Counter

A near-end block error (NEBE) indicates that the error has been detected in the receive direction (i.e. NEBE in the NT = LT => NT error). This will be indicated with a MON-1-message NEBE in all NT-modes as well as the LT-RP-mode. Each detected NEBE-error increments the 8-bit NEBE-counter. When reaching the maximum count, counting is stopped and the counter value reads (FF_H).

The current value of the NEBE counter is read in both LT- and NT-modes with the MON-8-command RBEN. The response comprises two bytes: the first byte always indicates that a MON-8-message is replied to (80_H), the second represents the counter value (00_H) … (FF_H). Each read operation resets the counter to (00_H).

A far-end block error identifies errors in transmission direction (i.e. FEBE in the NT = NT => LT-error). FEBE errors are processed in the same manner as NEBE-errors. A far-end block error will be indicated with a MON-1-message FEBE (NT-modes and LT-RP). The FEBE counter is read and reset with the MON-8-command RBEF.

In case both, far-end and near-end block errors occur simultaneously, the MON-1-message FNBE will be issued in all NT-modes and the LT-RP-mode.

Near-End Errors

Definition

A near-end block error indicates errors that occurred in the receive direction, i.e.

NEBE (LT-side)error during transmission from NT to LT

NEBE (NT-side)error during transmission from LT to NT

A near-end block error is detected when the calculated check-sum of the received U-superframe does not correspond to the check-sum sent in the following U-superframe.

Indications

Each detected NEBE will cause the following indications:

NEBE counter will be incremented (maximum count is FF_H, no further incrementation after maximum count is reached)

U-maintenance bit “FEBE” is set to zero in the next U-superframe (for a duration of one superframe)

Read Out and Reset

The counter value may be read out with a MON-8-command

MON-8 RBEN

1	0	0	0	0	0	0	0

Read Block Errors Near-end

1	1	1	1	1	0	1	1

MON-8 ABEN

1	0	0	0	0	0	0	0

Answer Block Errors Near-end

C7	C6	C5	C4	C3	C2	C1	C0

C0 … C7: 8-bit counter value

Each read operation resets the NEBE-counter to 00_H. The counter is also reset in all except the following states:

Line Active
Pend. Transparent
Transparent
S/T Deactivated

Far End Errors

Definition

A far-end block error indicates errors that occurred in the transmit direction, i.e.

– FEBE (LT-side)error during transmission from LT to NT

A far-end block error is detected when the U-maintenance bit “FEBE” is set to zero.

Indications

Each detected FEBE will cause the following indications:

– FEBE-counter will be incremented (maximum count is FF_H, no further incrementation after maximum count is reached)

Read Out and Reset

The counter value may be read out with a MON-8-command

MON-8 RBEF

1	0	0	0	0	0	0	0

Read Block Errors Far-end

1	1	1	1	1	0	1	0

MON-8 ABEN

1	0	0	0	0	0	0	0

Answer Block Errors Far-end

C7	C6	C5	C4	C3	C2	C1	C0

C0 … C7: 8-bit counter value

Each read operation resets the FEBE-counter to 00_H. The counter is also reset in all except the following states:

Line Active
Pend. Transparent
Transparent
S/T Deactivated

The following section illustrates how block error counters can be tested.

2.10.2.2 Testing Block Error Counters

Figure 49 illustrates how near- and far-end block error counters can be tested. Transmission errors are simulated with artificially corrupted CRCs. With two commands the cyclic redundancy checksum can be inverted. A third command offers to invert single FEBE-bits.

MON-8 CCRC causes the Quad IEC DFE-Q to permanently transmit inverted CRCs. This command may be used on LT-side with the LT in transparent or auto-mode.

With the MON-8-command SFB it is possible to invert single FEBE-bits. Because this command does not provoke permanent FEBE-bit inversion but sets only one FEBE-bit to (0) per SFB command, it is possible to predict the exact FEBE-counter reading.

Note: *The main application for setting single FEBE-bits are repeater stations not operating in the LT-RP- or NT-RP-mode).*

With CCRC issued on LT-side, near-end block errors will be observed at the NT and far-end errors are noticed at the LT.

After RCC is issued on the LT-side (NT in auto-mode), near-end block errors will be registered on the LT-side.

With the MON-0-command NCC issued on LT-side the NEBE-detection can be disabled depending on the NT-mode selected:

Auto-mode	NEBE-detection stopped, no MON-1 NEBE-messages and NEBE-counter disabled

Transparent mode	NEBE-detection enabled, MON-1-message NEBE issued and NEBE-counter enabled

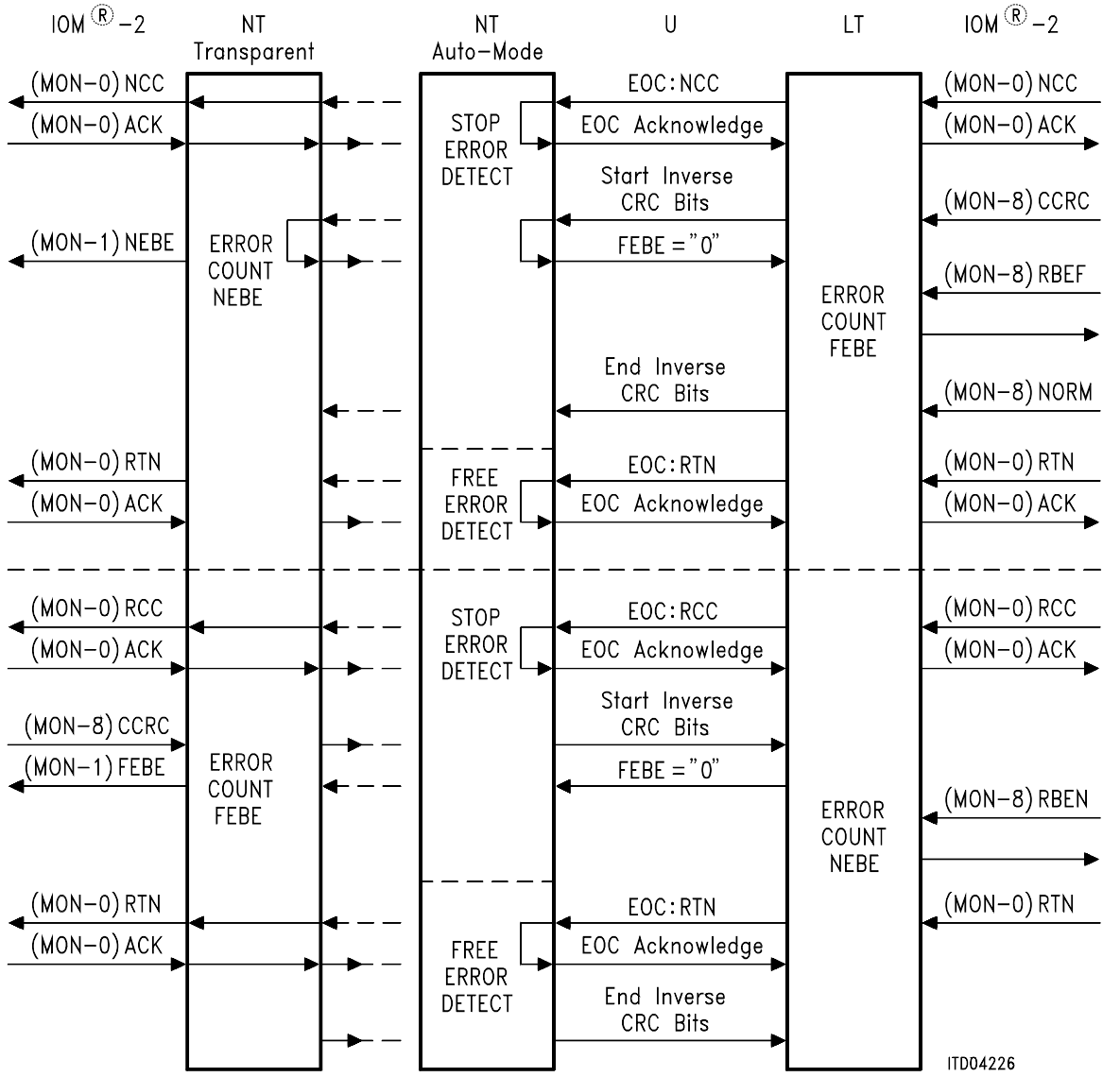


Figure 49
Block Error Counter Test

The following commands are available for testing block error counters:

Notify of Corrupt CRC

Initialization (LT-side)

MON-0						NCC		Notify of Corrupt CRC							
0	0	0	0	0	0	0	1	0	1	0	1	0	1	0	0

Acknowledgment (NT- and LT-side)

MON-0						NCC		Notify of Corrupt CRC							
0	0	0	0	0	0	0	1	0	1	0	1	0	1	0	0

Request Corrupt CRCs

Function

Requests the NT-side (in auto-mode) to transmit corrupted (i.e. inverted) CRCs upstream to test the LT NEBE-counter.

Initialization (LT-side)

MON-0						RCC		Request of Corrupt CRC							
0	0	0	0	0	0	0	1	0	1	0	1	0	0	1	1

Acknowledgment (NT- and LT-side)

MON-0						RCC		Request of Corrupt CRC							
0	0	0	0	0	0	0	1	0	1	0	1	0	0	1	1

Return to Normal

Function

Disables all previously sent EOC-commands.

Initialization (LT-side)

MON-0						RTN		Return to Normal							
0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1

Acknowledgment (NT- and LT-side)

MON-0						RTN		Return to Normal							
0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1

Corrupt CRCs

Function

Requests the device to transmit corrupted (i.e. inverted) CRCs. In auto- and transparent mode of LT-modes the command will be executed directly.

Initialization:

MON-8						CCRC	
1	0	0	0	0	0	0	0

Corrupt CRC							
1	1	1	1	0	0	0	0

No acknowledgment will be issued.

Normal

Function

Disables all previously sent MON-8 latching commands..

Initialization:

MON-8						NORM	
1	0	0	0	0	0	0	0

Normal							
1	1	1	1	1	1	1	1

No acknowledgment will be issued.

2.10.3 Test Modes and System Measurements

With a number of operational modes the Quad IEC DFE-Q supports system measurements. These modes along with the most frequently needed system measurements are described in the following sections.

2.10.3.1 Single-Pulses Test Mode

In the single-pulses test mode, the Quad IEC DFE-Q transmits to the U-interface alternating ± 3 pulses spaced by 1.5 ms. Three options exist for selecting the “Send-Single-Pulses” (SSP) mode:

– hardware selection:RESQ = 1 & TSP = 1
– software selection:C/I = SSP (0101_B)
– selection by TAP-controller command (1010_B)

All methods are fully equivalent with the exception that a hardware selection and TAP-controller command impact all four channels, while the software selection only impacts the chosen channel. In the SSP-mode the C/I-code transmitted by the Quad IEC DFE-Q is DEAC.

The SSP-test mode is required for pulse mask measurements.

2.10.3.2 Data-Through Mode

When selecting the data-through mode, the Quad IEC DFE-Q is forced directly into the “Transparent” state. This is possible from any state in the state diagram.

The Data-Through option (DT) provides the possibility to transmit a standard scrambled U-signal even if no U-interface wake-up protocol is possible. This feature is of interest when no counter station can be connected to supply the wake-up protocol signals.

As with the SSP-mode, three options are available.

– hardware selection:RESQ = 0 & TSP = 1
– software selection:C/I = DT (0110_B)
– TAP-controller command (1001_B)

Compared with the software selection, a hardware selection and a TAP command offer the option to initiate Quad IEC DFE-Q actions via C/I-code (e.g. analog loop-back with C/I = ARL). All methods are fully equivalent with the exception that a hardware selection and TAP-controller command impact all four channels, while the software selection only impacts the chosen channel.

The DT-mode is required for power spectral density and total power measurements.

2.10.3.3 Master-Reset Mode

The master-reset mode characterizes the mode where the Quad IEC DFE-Q does not transmit any signals. The chip is in the “Test” state. All echo canceller and equalizer coefficients are reset. As can be seen from the state diagram, no activation is possible when the device is in the “Test” state.

For measurements two methods are recommended in order to transfer the Quad IEC DFE-Q into the master-reset mode:

– hardware selection:RESQ = 0 & TSP = 0
– software selection:C/I = RES (0001_B)

Both alternatives are fully compatible with the exception that a hardware reset impacts all four channels, while the software reset only impacts the chosen channel.

The C/I-code transmitted by the Quad IEC DFE-Q in the “Test” state is DEAC.

The master-reset test mode is used for the return-loss measurements.

2.10.3.4 Pulse Mask Measurement

– Pulse mask is defined in ANSI T1.601 1991 and ETSI ETR080 1993
– U-interface has to be terminated with 135 Ω
– Quad IEC DFE-Q is in “Single-Pulses” mode (see **section 2.10.3.1**)
– Measurements are done using an oscilloscope

2.10.3.5 Power Spectral-Density Measurement

– PSD is defined in ANSI T1.601 1991 and ETSI ETR080 1993
– U-interface has to be terminated with 135 Ω
– Quad IEC DFE-Q is in “Data-Through” mode (see **section 2.10.3.2**)
– For measurements a spectrum analyzer is employed

2.10.3.6 Total Power Measurement

– Total power is defined in ANSI T1.601 1991 and ETSI ETR080 1993
– Total power must be between 13 dBm and 14 dBm
– U-interface has to be terminated with 135 Ω
– Quad IEC DFE-Q is in “Data-Through” mode (see **section 2.10.3.2**)
– Measurements are done using an 80 kHz high-impedance low-pass filter and true RMS-voltmeter

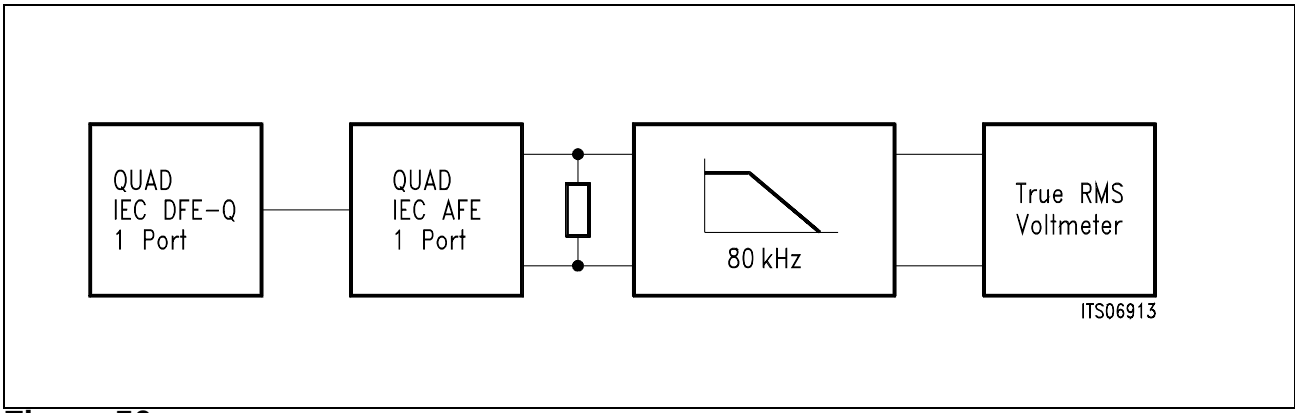


Figure 50
Total Power Measurement Set-Up

2.10.3.7 Return-Loss Measurement

– Return loss is defined in ANSI T1.601 1991 and ETSI ETR080 1993
– Quad IEC DFE-Q is in “Test” state (C/I = 0001 or/RESQ = 0 & TSP = 0)
– Measure complex impedance “Z” from 14 kHz – 200 kHz
– Calculate return loss with formula:
RL(dB) = 20log (abs((Z + 135) / (Z –135)))

2.10.3.8 Quiet Mode Measurement

– Quiet mode is defined in ANSI T1.601 1991 and ETSI ETR080 1993
– Quad IEC DFE-Q is in the “Test” state (C/I = 0001 or/RESQ = 0 & TSP = 0)
– Trigger and exit criteria have to be realized externally

2.10.3.9 Insertion Loss Measurement

– Insertion loss is defined in ANSI T1.601 1991 and ETSI ETR080 1993
– Quad IEC DFE-Q is in “Data-Through” mode (see **section 2.10.3.2**)
– Trigger and exit criteria have to be realized externally

2.10.4 Chip Internal Test Options

In addition to the features described in the previous sections, the Quad IEC DFE-Q permits limited access to internal test procedures and internal data.

2.10.4.1 Coefficient Values

Some of the internal chip registers can be read via MON-8-messages.

Of interest to the user are the values of the coefficients for equalizer and echo canceller. This information will however only proof useful if a detailed, theoretical chip knowledge exists.

Registers are read by sending a two-byte MON-8-message. The first byte identifies the command as an internal register access, the second addresses the register. The 16-bit register value is returned in two messages of two bytes each.

For a quick reference the key characteristics of Chip Internal Test Options are summarized on the following lines:

Function

Internal data is partly available in internal registers. These registers are read by sending a two-byte MON-8-message. The first byte identifies the command as an internal register access, the second byte addresses the register.

Table 24 shows the address range for equalizer (26 coefficients) and echo canceller coefficients
(36 coefficients).

Initialization

Read request

MON-8	(1. Byte)	1 0 0 0	1 0 0 0	; Select register access
	(2. Byte)	a a a a	a a a a	; Coefficient address

For each requested coefficient 16 bit are returned in the following manner

MON-8	(1. Byte)	1 0 0 0	1 0 0 0	
	(2. Byte)	d d d d	d d d d	; Data bits D0 – D7[1)]
	(3. Byte)	1 0 0 0	1 1 0 0	
	(4. Byte)	d d d d	d d d d	; Data bits D8 – D15[1)]

Note: [1)] *Binary complement format ($FFFF_H$ = –1d)*

Table 24
Internal Coefficient Addresses

Register	Address Range (decimal)	1. Filter Coefficient
Echo Canceller	6 … 41	41
Equalizer	44 … 69	69

2.10.4.2 Test Pins

Three test pins, TP (pin 62), TP1 (pin 63) and TPD (pin 16) exist. All test pins are used for Siemens internal testing only and have no relevance to the user. For a correct operation of the Quad IEC DFE-Q, these pins should be connected to ground (GND).

2.11 Boundary Scan Test Controller

The Quad IEC DFE-Q provides a boundary scan support for a cost effective board testing. It consists of:

–Complete boundary scan for 49 signals (pins) according to IEEE Std. 1149.1 specification

–Test access port controller (TAP)

–Four dedicated pins (TCK, TMS, TDI, TDO)

–One 32-bit IDCODE register

–two additional test commands performing "send single pulses" and "data through" modes

Boundary Scan

All pins except the power supply pins, the "not connected" pins and pins TDI, TDO, TCK, TMS are included in the boundary scan.

Depending on the pin functionality one, two or three boundary scan cells are provided. Note, that there are several pins, which for chip test are used as I/O pins. Please refer to **section 1.4** whether these pins are inputs or outputs. However, they are included to the boundary scan as I/O pins with three scan cells

Table 25
Boundary Scan Cells.

Pin Type	Number of Boundary Scan Cells	Usage
Input	1	input
Output	2	output, enable
I/O	3	input, output, enable

When the TAP controller is in the appropriate mode data is shifted into or out of the boundary scan via the pins TDI/TDO using the 6.25 MHz clock on pin TCK.

The pins are included in the following sequence in the boundary scan:

Table 26
Boundary Scan Sequence

Boundary Scan Number TDI –––>	Pin Number	Pin Name	Type	Number of Scan Cells
1	63	TP1	I/O	3
2	62	TP	I	1
3	61	CLS3	O	2
4	60	RESQ	I	1
5	59	AUTO	I	1
6	58	PBX	I	1
7	56	TSP	I	1
8	55	SLOT	I	1
9	53	LT	I/O	3
10	52	CLS2	I/O	3
11	51	D3D	I/O	3
12	50	D2D	I/O	3
13	48	D1D	I/O	3
14	47	D0D	I/O	3
15	46	D3C	I/O	3
16	44	D2C	I/O	3
17	43	D1C	I/O	3
18	42	D0C	I/O	3
19	40	D3B	O	2
20	39	D2B	O	2
21	37	D1B	O	2
22	36	DSYNC	I/O	3
23	35	D0B	O	2
24	34	D3A	O	2
25	33	D2A	O	2
26	31	D1A	O	2
27	30	D0A	O	2
28	29	CLS0	O	2

Boundary Scan Number TDI –––>	Pin Number	Pin Name	Type	Number of Scan Cells
29	28	ST00	I	1
30	27	ST01	I	1
31	26	ST10	I	1
32	24	ST11	I	1
33	23	ST20	I	1
34	21	ST21	I	1
35	20	CLS1	O	2
36	19	ST30	I	1
37	18	ST31	I/O	3
38	17	SDX	O	2
39	16	TPD	I	1
40	15	DOUT	O	2
41	14	DIN	I	1
42	13	FSC	I/O	3
43	12	DCL	I/O	3
44	11	PDM0	I/O	3
45	10	PDM1	I/O	3
46	8	PDM2	I	1
47	7	PDM3	I	1
48	5	SDR	I/O	3
49	4	CL15	I	1

TAP Controller

The *Test Access Port* (TAP) controller implements the state machine defined in the JTAG standard IEEE Std. 1149.1. Transitions on the pin TMS cause the TAP controller to perform a state change.

Following the standard definition 7 instructions are executable. Additionally, there are two specific test instructions.

Table 27
TAP controller instructions:

Code	Instruction	Function
0000	EXTEST	External testing
0001	INTEST	Internal testing
0010	SAMPLE/PRELOAD	Snap-shot testing
0011	IDCODE	Reading ID code
01XX	reserved	
1000	reserved	
1001	DT	Data through
1010	SSP	Send single pulses
1011	reserved	
11XX	BYPASS	Bypass operation

EXTEST is used to examine the board interconnections.

When the TAP controller is in the state "update DR", all output pins are updated with the falling edge of TCK. When it has entered state "capture DR" the levels of all input pins are latched with the rising edge of TCK. The in/out shifting of the scan vectors is typically done using the instruction SAMPLE/PRELOAD.

INTEST supports internal chip testing.

When the TAP controller is in the state "update DR", all inputs are updated internally with the falling edge of TCK. When it has entered state "capture DR" the levels of all outputs are latched with the rising edge of TCK. The in/out shifting of the scan vectors is typically done using the instruction SAMPLE/PRELOAD.

Note: 0001 (INTEST) is the default value of the instruction register.

SAMPLE/PRELOAD provides a snap-shot of the pin level during normal operation or is used to preload (TDI) / shift out (TDO) the boundary scan with a test vector. Both activities are transparent to the system functionality.

IDCODE Register

The 32-bit identification register is serially read out via TDO. It contains the version number (4 bits), the device code (16 bits) and the manufacturer code (11 bits). The LSB is fixed to "1".

Version	Device Code	Manufacturer Code		Output
0010	0000 0000 0010 1001	0000 1000 001	1	--> TDO

Note: In the state "test logic reset" the code "0011" is loaded into the instruction code register.

BYPASS, a bit entering TDI is shifted to TDO after one TCK clock cycle, e.g. to skip testing of selected ICs on a printed circuit board.

SSP does the same as setting the pins TSP and RESQ in SSP-mode. Single alternating pulses are issued to the ESCC8 on all ports via the SDX pin.

DT sets the device in "data through" mode. The function is exactly as if data through were set with the TSP pin and the RESQ pin.

3 Electrical Characteristics

Absolute Maximum Ratings

Parameter	Symbol	Limit Values	Unit
Ambient temperature under bias: PEB PEF	T_A	0 to 70 – 40 to 85	°C
Storage temperature	T_{stg}	– 65 to 125	°C
Voltage on any pin with respect to ground	V_S	– 0.4 to V_{DD} + 0.4	V
Maximum voltage on any pin	V_{max}	6	V

Note: Stresses above those listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
Maximum ratings are absolute ratings; exceeding only one of these values may cause irreversible damage to the integrated circuit.

3.1 Static Characteristics

V_{DD} = 4.75 to 5.25 V

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
High-level input voltage	V_{IH}	2.0	V_{DD} + 0.3	V	
Low-level input voltage	V_{IL}		0.8	V	
Low-level input leakage current	I_{IL}	-1		µA	V_I = GND[1)]
High-level input leakage current	I_{IH}		1	µA	V_I = VDD[1)]
Low-level leakage current pull up pins	I_{IT}	-500		µA	V_I = GND[1)]
High-level output voltage (except DOUT, relay driver pins D0A .. D3D)	V_{OH1}	2.4		V	I_{OH1} = 0.4 mA
High-level output voltage for DOUT	V_{OH2}	3.5		V	I_{OH2} = 6 mA[1)]
High-level output voltage for relay driver pins D0A .. D3D	V_{OH3}	2.4		V	I_{OH3} = 2.0 mA [1)]
Low-level output voltage	V_{OL1}		0.4	V	I_{OL1} = 2 mA[1)]
Low-level output voltage for DOUT	V_{OL2}		0.5	V	I_{OL1} = 7 mA[1)]
Input capacitance	C_{IN}		10	pF	

Note: *[1)] Inputs at VDD/GND*

3.2 Dynamic Characteristics

Ambient temperature under bias range, V_{DD} = 5 V ± 5 %.

Inputs are driven to 2.4 V for a logical ’1’ and to 0.4 V for a logical ’0’.
Timing measurements are made at 2.0 V for a logical ’1’ and at 0.8 V for a logical ’0’.
The AC-testing input/output wave forms are shown below. The test load is 100pF, unless otherwise indicated.

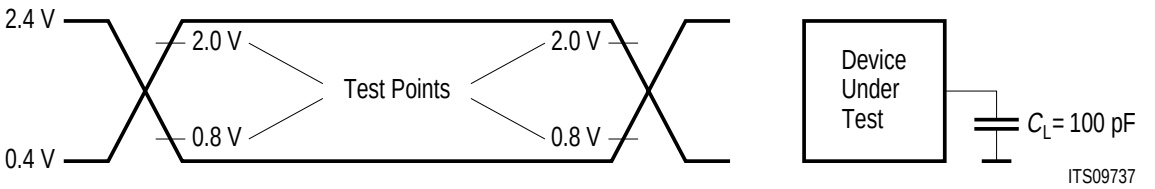


Figure 51
I/O-Wave Form for AC-Test

IOM-2 Timing

In case the period of signals is stated the time reference will be at 1.4 V; in all other cases 0.8 V (low) and 2.0 V (high) thresholds are used as reference.

The dynamic characteristics of the IOM-2-interface is given in **figure 52** where Detail “a” of **figure 11** is shown in more detail.

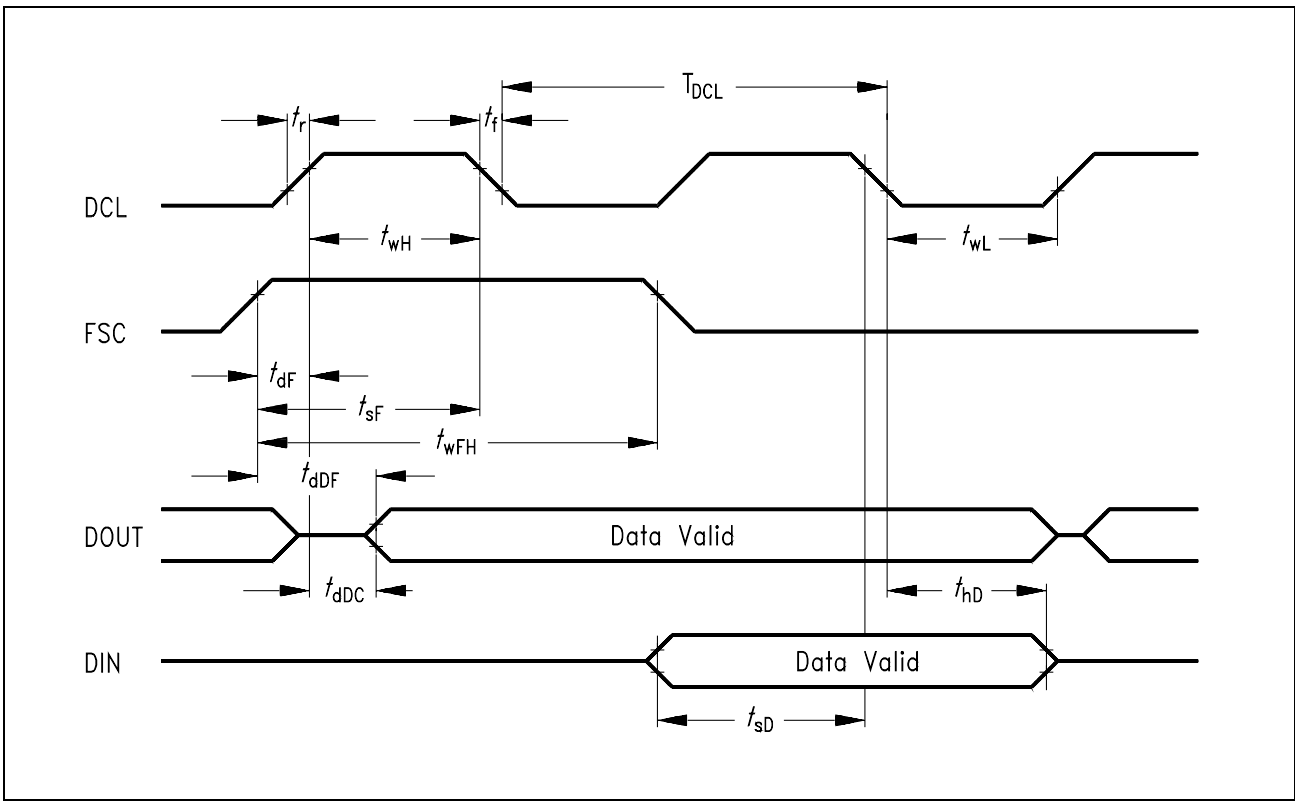


Figure 52
IOM®-2 Timing of IOM-2 Interface (Detail)

Table 28
IOM®-2 Dynamic Input Characteristics

Parameter	Signal	Symbol	Limit Values		Unit
			min.	max.	
Data clock rise/fall	DCL	t_r, t_f		60	ns
Clock period		T_{DCL}	200		ns
Pulse width high/low		t_{wH} t_{wL}	53 53		ns ns
Frame synch. rise/fall	FSC	t_r, t_f		60	ns
Frame setup		t_{sF}	30		ns

Parameter	Signal	Symbol	Limit Values		Unit
			min.	max.	
Frame hold		t_{dF}		t_{wL} – 30	ns
Frame width high/low [1]		t_{wFH} t_{wFL}	100 $2 \times T_{DCL}$		ns
Data sample delay	DIN	t_{sD}	t_{wH} + 20		ns
Data hold		t_{hD}	50		ns

Note: *[1] This is in accordance with the IOM-timing specification. For correct functional operation the high period must be $1 \times T_{DCL}$ for superframe markers and at least $2 \times T_{DCL}$ for non-superframe markers.*

Table 29
IOM®-2 Dynamic Output Characteristics

Parameter	Signal	Symbol	Limit Values			Unit	Test Condition
			min.	typ.	max.		
Data delay/clock [1]	DOUT	t_{dDC}			100	ns	C_L = 150 pF
Data delay/frame [1]	DOUT	t_{dDF}			150	ns	C_L = 150 pF

Notes: *[1] The point of time at which the output data will be valid is referred to the rising edges of either FSC (t_{dDF}) or DCL (t_{dDC}). The rising edge of the signal appearing last (normally DCL) shall be the reference.*

Interface to the Analog Front End

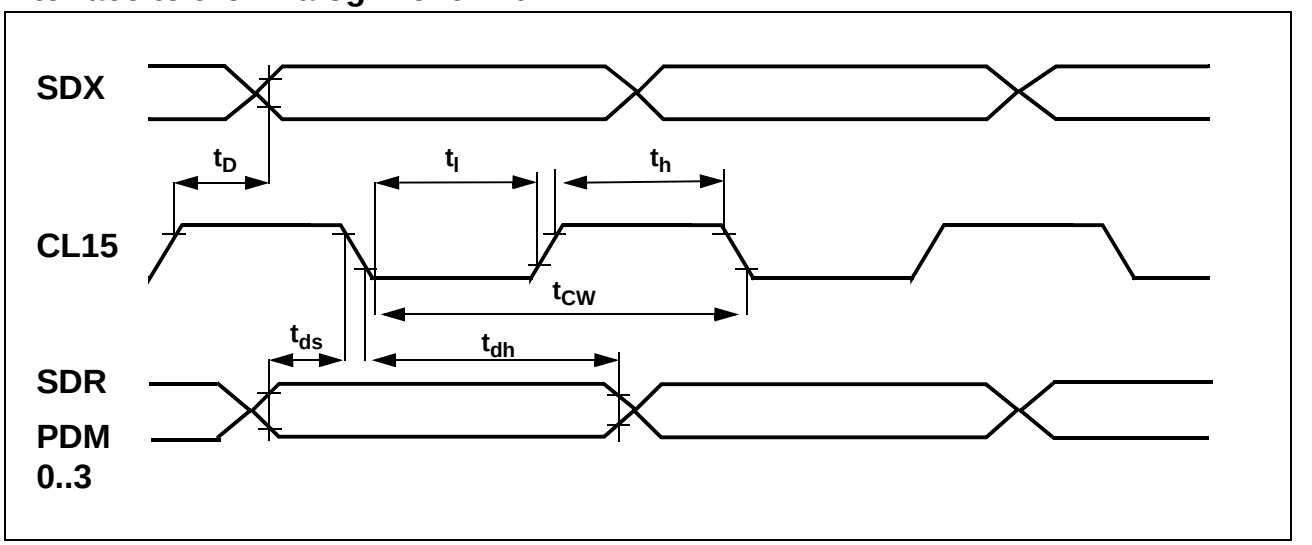


Figure 53
Dynamic Input and Output Requirements at the Analog Interface

Table 30
Dynamic Input Characteristics

Parameter	Signal	Symbol	Limit Values			Unit
			min.	typ.	max.	
Clock period	CL15	t_{cw}		65		ns
Pulse width high/ low	CL15	t_h t_l	25 25			ns ns
Data setup	SDR PDM0..3	t_{ds}	0 5			ns
Data hold	SDR PDM0..3	t_{dh}	15 8			ns

Table 31
Dynamic Output Characteristics

Parameter	Signal	Symbol	Limit Values			Unit
			min.	typ.	max.	
SDX data delay	SDX	t_D			28	ns

LT to FSC timing in LT-PBX mode with DECT synchronization

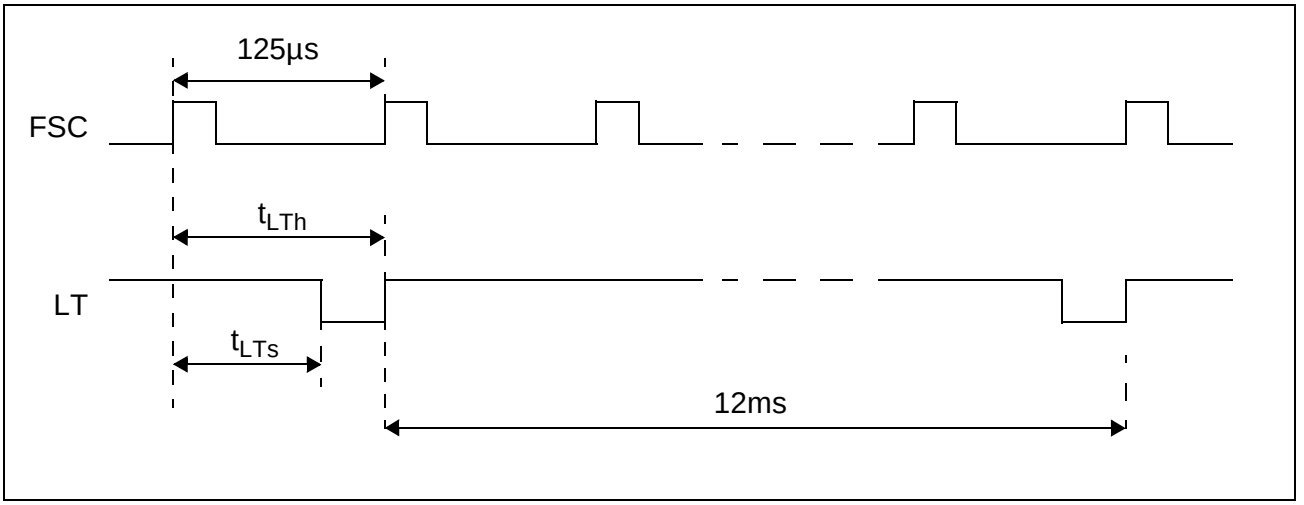


Figure 54
LT to FSC timing

Table 32
LT to FSC timing

Parameter	Limit Values		Unit
	min.	max.	
t_{LTs}	-9	105	µs
t_{LTh}	115	230	µs

Boundary Scan Timing

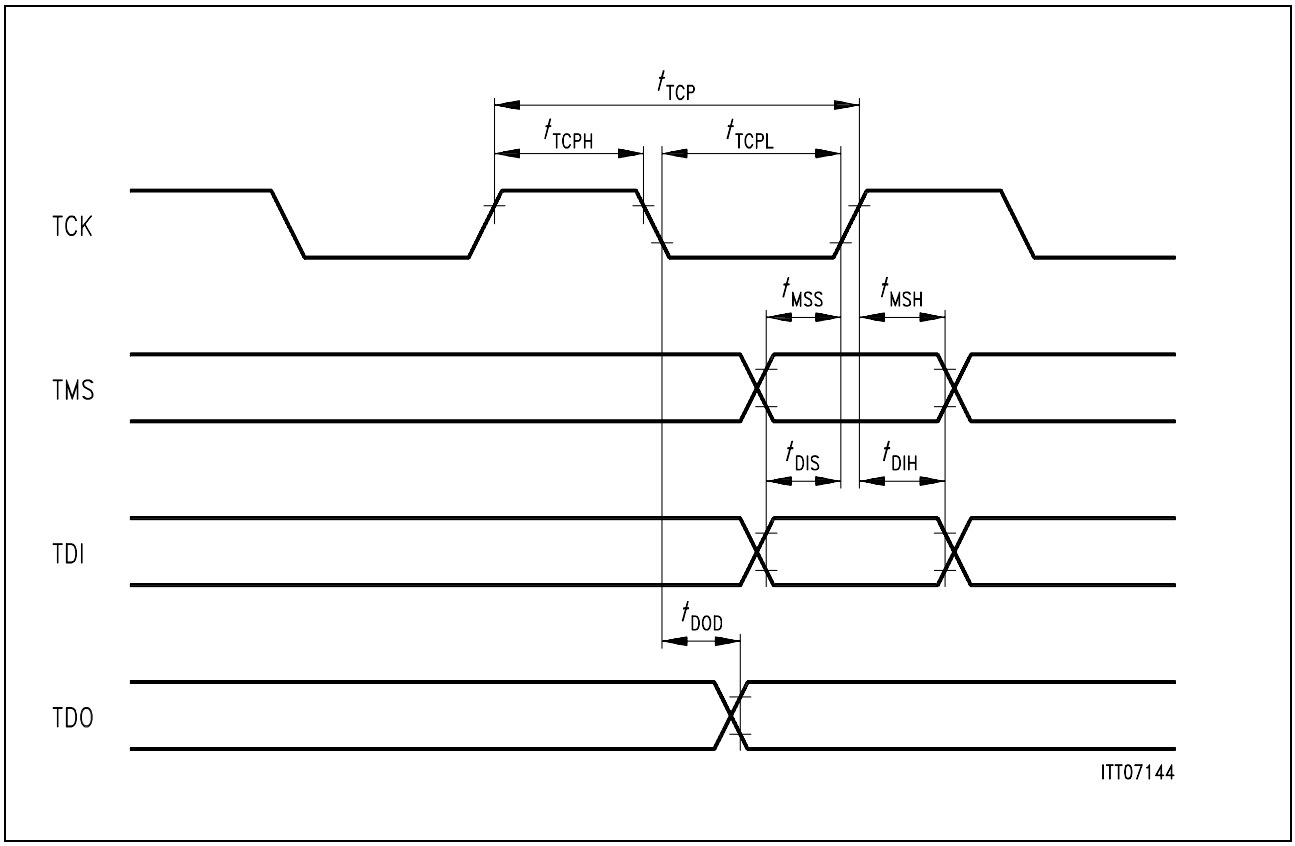


Figure 55
Boundary Scan Timing

Table 33
Boundary Scan Dynamic Timing Requirements

Parameter	Symbol	Limit Values		Unit
		min.	max.	
test clock period	t_{TCP}	160	-	ns
test clock period low	t_{TCPL}	70	-	ns
test clock period high	t_{TCPH}	70	-	ns
TMS set-up time to TCK	t_{MSS}	30	-	ns
TMS hold time from TCK	t_{MSH}	30	-	ns
TDI set-up time to TCK	t_{DIS}	30	-	ns
TDI hold time from TCK	t_{DIH}	30	-	ns
TDO valid delay from TCK	t_{DOD}	-	60	ns

3.3 Power Supply

Supply voltages

V_{DD} = + 5 V ± 0.25 V

Power Consumption

All measurements with random 2B + D data in active states.

Mode	Test conditions	Typ. values	Max. values	Unit
Power-up all Channels ?	5.00 V, open outputs, inputs at V_{DD} /V_{SS}	50	70	mA
Power-down	5.00 V, open outputs, inputs at V_{DD} /V_{SS}	15	25	mA

Absolute Maximum Ratings

Parameter	Symbol	Limit Values	Unit
Supply voltage	V_{DD}	– 0.3 < V_{DD} < 7.0	V
Input voltage	V_I	– 0.3 < V_I < V_{DD} + 0.3 (max. 7)	V
Output voltage	V_O	– 0.3 < V_O < V_{DD} + 0.3 (max 7)	V
Max. voltage between different GND pins	V_S	± 250	mV
Max. voltage between different VDD pins	V_S	± 250	mV
Storage temperature	T_{stg}	– 65 to 125	°C
Ambient temperature PEB 24911 PEF 24911	 T_A T_A	 0 to 70 – 40 to 85	 °C °C
Thermal resistance (system-air) (system-case)	 $R_{th\ SA}$ $R_{th\ SC}$	 55 15	 K/W K/W

Note: *Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.*
Exposure to conditions beyond those indicated in the recommended operational conditions of this specification may affect device reliability. This is a stress rating only and functional operation of the device under those conditions or at any other condition beyond those indicated in the operational conditions of this specification is not implied. It is not implied, that more than one of those conditions can be applied simultaneously.

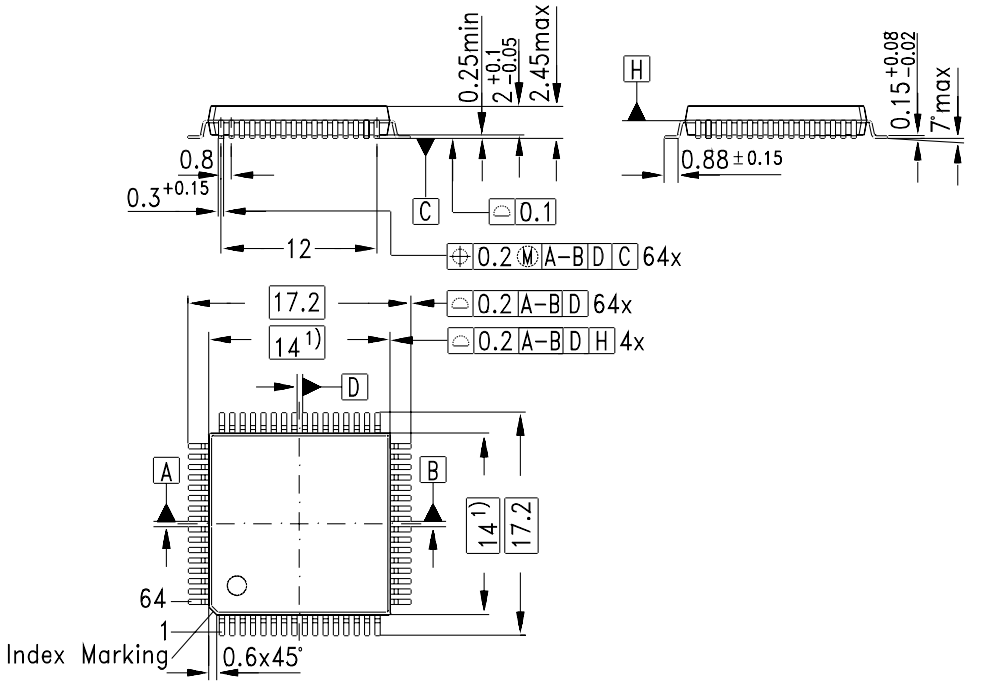
4 Glossary

AGC	Automatic gain control
ANSI	American National Standardization Institute
ARCOFI	Audio ringing codec filter
ASIC	Application specific integrated circuit
B	64-kbit/s voice and data transmission channel
C/I	Command/Indicate (channel)
CCITT	Comité Consultatif International des Téléphones et Télégraph
CCRC	Corrupted CRC
CLS	Synchronizing clock
CNET	Centre Nationale d'Etudes des Telecommunications
CO	Central office
CRC	Cyclic redundancy check
D	16-kbit/s data and control transmission channel
DCL	Data clock
DD	Data downstream
DIN	IOM-data input
DOUT	IOM-data output
DT	Data through test mode
DU	Data upstream
EC	Echo canceller
EOC	Embedded operations channel
EOM	End of message
EPIC	Extended peripheral interface controller
ETSI	European Telephone Standards Institute
FEBE	Far-end block error
FIFO	First-in first-out (memory)
FSC	Frame synchronizing clock
GND	Ground
HDLC	High-level data link control
IDEC	ISDN-D-channel exchange controller
IEC-Q	ISDN-echo cancellation circuit conforming to 2B1Q-transmission code
IOM-2	ISDN-oriented modular 2nd generation
INFO	U-interface signal as specified by ANSI
ISDN	Integrated services digital network
ISW	Inverted synchronization word
LB	Loop back
LBBD	Loop-back of B- and D-channels
LSB	Least significant bit
LT	Line termination
MON	Monitor channel command
MSB	Most significant bit

MR	Monitor read bit
MX	Monitor transmit bit
NCC	Notify of corrupt CRC
NEBE	Near-end block error
NT	Network termination
OSI	Open systems interconnection
PBX	Private branch exchange
PLL	Phase locked loop
PSD	Power spectral density
PTT	Post, telephone, and telegraph administration
PU	Power-up
RCC	Request corrupt CRC
RMS	Root mean square
RP	Repeater
S/T	Two-wire pair interface
SBCX	S/T-bus interface circuit extended
SICOFI	Signal processing codec filter
SLIC	Subscriber line interface circuit
SSP	Send single pulses (test mode)
SW	Synchronization word
TE	Terminal equipment
TL	Wake-up tone, LT side
TN	Wake-up tone, NT side
TP	Test pin
U	Single wire pair interface
UTC	Unable to comply
2B1Q	Transmission code requiring 80-kHz bandwidth

5 Package Outlines

M-QFP -64-1



1) Does not include plastic or metal protrusions of 0.25 max per side

Figure 56
Package Outlines