

■ MB89321A, MB89322A CMOS Programmable CRT Controller

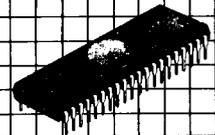
Description

The MB89321A/MB89322A Programmable CRT Controllers are single chip CMOS devices used to interface CRT raster scan displays with microcomputer systems. Both devices operate on a single +5 V power supply and have TTL-compatible I/O. The MB89321A interfaces to 6800 family microprocessors; the MB89322A to the 8080.

The MB89321A/MB89322A refresh the display by buffering information from main memory using thirty-three internal registers and keeping track of the display position of the screen. Both devices are designed to allow simple interfacing to most raster scan CRTs with a minimum of external hardware and software overhead.

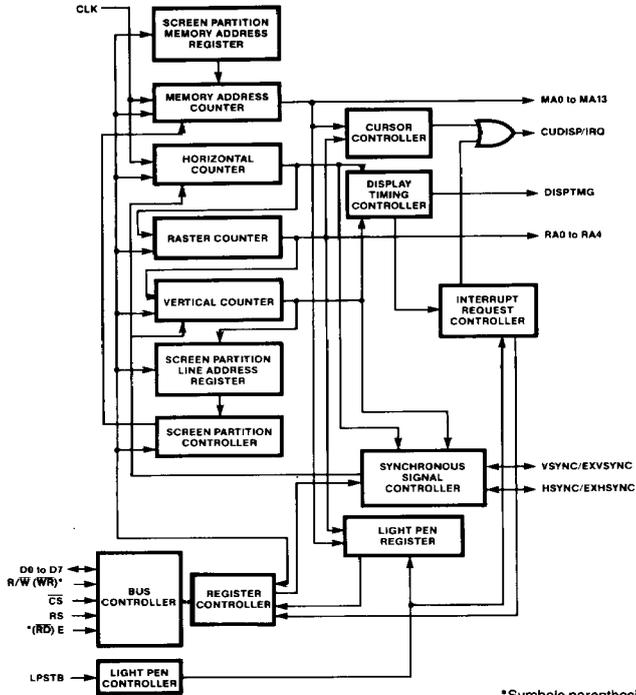
Features

- Programmable Screen and Character Formats
- Cursor Control (3 types)
- Selectable Scan Modes (3 types)
- Light Pen Detection
- Refresh Memory Address Function
- Screen Partitioning (up to 4 partitions)
- Independent Paging/Scrolling for Each Screen Partition
- Smooth Scrolling (up to 4 screens simultaneously)
- Status Generation and Processor Interrupt Generation by Vertical Blanking or Light Pen
- External Sync for TV Superimposition (synchronous mode) or Interface to Other CRT Controllers (master-slave mode)
- Double-Size Vertical Display using Raster Interpolation
- 4.0 MHz Clock Rate
- Single +5 V Power Supply
- CMOS Process
- 40-pin Plastic DIP



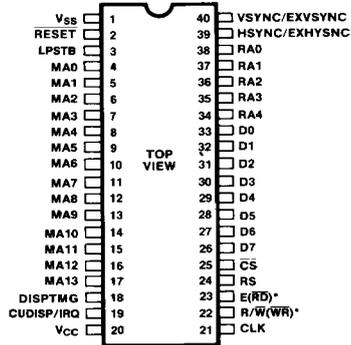
40-Lead Plastic DIP
(DIP-40P-M01)

Functional Block Diagram



*Symbols parenthesized are applied to MB89322A.

Pin Assignment



*Symbols parenthesized are applied to MB89322A.

Pin Descriptions
MB89321A(MB89322A)

Pin Number	Symbol	Pin Name	Function
1	V _{SS}	Ground	Ground
2	RESET	Reset	Input used for device reset. When RESET goes low: <ul style="list-style-type: none"> • Internal counters are cleared and stopped; • All outputs go low, and; • Control registers and status register are cleared, other internal registers unaffected. <p>Enabled only when LPSTB is low. RESET goes high, display is initiated immediately. Control registers R30 and R31 must be initialized by software after reset is released.</p>
3	LPSTB	Light Pen Strobe	Character detection input. When high, the memory address is loaded in the light pen register, the raster address in the light pen raster register, and the status bit set.
4 to 17	MA0 to MA13	Memory Address	Refresh memory address output
18	DISPTMG	Display Timing	Display timing output. Set to high during display.
19	CUDISP/IRQ	Cursor Display Timing/Interrupt Request	Cursor display timing output/interrupt request output. Set to high during display. Setting the control register enables a high-level interrupt request signal to be output while the display timing signal is low.
20	V _{CC}	Power Supply	+5 V power supply.
21	CLK	Clock	Clock input. Goes low during EXHSYNC in TV sync mode.
22	R/W (WR)*	Read/Write (Write)	MPU read/write input. (MPU write input)
23	E (RD)*	Enable (Read)	MPU enable input. (MPU read input)
24	RS	Register select	Internal register select input. Normally connected to the least significant bit (A0) of the address bus. When high, selects internal registers; when low, the address register.
25	\overline{CS}	Chip select	Chip select input. Goes low when the MPU accesses the CRTC.
26 to 33	D7 to D0	Data Bus	MPU data bus pins
34 to 38	RA4 to RA0	Raster Address	Raster address output
39	HSYNC/EXHSYNC	Hsync Output/Hsync Input	Horizontal sync output/external horizontal sync input. When reset, becomes the horizontal sync output.
40	VSYNC/EXVSYNC	Vsync Output/Vsync Input	Vertical sync output/external vertical sync input. When reset, becomes the vertical sync output.

*Symbols parenthesized are applied to MB89322A.

Register Description

Address Register (AR)

Sets the number of the internal register. Unchanged until a new value is written.

Total Number of Characters in Line Register (RO)

Sets horizontal scan sync. Settings indicate number of characters, and are determined by the formula:

$$\text{Total Number of Characters in Line} \times \text{Character Period} = \text{Horizontal Scan Period}$$

Values written to the register are 1 less than the set values.

Number of Characters Displayed in Line Register (R1)

Sets the horizontal display period. Settings indicate number of characters.

Horizontal Sync Position Register (R2)

Sets the horizontal sync signal position. Settings indicate number of characters. Values written to the register are 1 less than the set values.

Sync Signal Pulse Width Register (R3)

MSB				LSB			
V3	V2	V1	V0	H3	H2	H1	H0

Sets the sync signal pulse width. The 4 high-order bits are used for the vertical sync signal, the 4 low-order bits for the horizontal sync signal. the TV sync mode, the 4 low-order bits are used as the horizontal back porch.

Total Number of Lines Register (R4)

Used the the total raster adjust register to set vertical sync (field sync is set by number of rasters). Setting is in number of lines. Values written to the register are 1 less than the set value.

Total Raster Adjust Register (R5)

Used to fine tune the vertical sync. Settings indicate number of rasters, and must be less than the maximum raster address. Vertical sync is determined by the formula:

$$\text{Vertical Sync} = \text{Total Number of Lines} \times \text{Maximum Raster Address} + \text{Total Raster Adjust}$$

Number of Lines Displayed Register (R6)

Sets the vertical display period. Settings indicate number of lines.

Vertical Sync Position Register (R7)

Used with the vertical sync position fine adjust register (R27) to set vertical sync position using raster count. Settings indicate number of lines. Values written to the register are 1 less than the set values.

Scan Mode/Skew Register (R8)

MSB				LSB			
C1	C0	D1	D0	I1	I0		

Sets cursor display signal and display timing signal skew, and the scan mode. Bit functions are as shown below:

C1 C0 CUDISP Output

0	0	Output without skew
0	1	Skewed by 1 character
1	0	Skewed by 2 characters
1	1	No CUDISP output

D1 D0 DISPTMG Output

0	0	Output without skew
0	1	Skewed by 1 character
1	0	Skewed by 2 characters
1	1	No DISPTMG output

I1 I0 Scan Mode

0	0	Non-interlace mode
0	1	Interlace mode
1	0	Non-interlace mode
1	1	Interlace and video mode

Maximum Raster Address Register (R9)

Sets the number of rasters in a line. In interlace and non-interlace modes, the value written is 1 less than the set value; in interlace and video mode, 2 less. Examples of settings in each mode are as follows:

Interlace mode

0	-----	0
1	-----	1
2	-----	2
3	-----	3
4	-----	4

Raster count - 5
Value written - 4

Non-interlace mode

0	-----	
1	-----	
2	-----	
3	-----	
4	-----	

Raster count - 5
Value written - 4

Interlace & video modes

0	-----	1
2	-----	
4	-----	3

Raster count - 5
Value written - 3

Non-interlace mode and Interlace mode:
Written value = Setting value - 1
Interlace mode & video mode:
Written value = Setting value - 2

Register Description
(Continued)

Control Register (R30)

MSB						LSB	
VE	VS	IB	IL	SY	TV	P1	P0

Controls the external sync function, interrupt function, vertical sync position fine adjust function and screen

partition function. This register must be initialized by software after reset is released. Bit functions are as shown below:

VE	VS	TV	External Sync Function
0	0	0	Both VSYNC and HSYNC are in output mode. DISPTMG is active. External sync operation is disabled.
0	1	0	Outputs VSYNC for odd-numbered fields only in interlace mode. No VSYNC output when the programmed values of max. raster address and vertical sync position are odd numbers in interlace & video mode.
1	0	0	EXVSYNC is in input mode but external sync signal ignored. DISPTMG is active.
1	1	0	EXVSYNC is in input mode and external sync signal is accepted. DISPTMG goes low (disabled).
0	0	1	Disallowed
0	1	1	Disallowed
1	0	1	Both EXVSYNC and EXHSYNC are in input mode and external sync signal is accepted. DISPTMG output is active.
1	1	1	Both EXVSYNC and EXHSYNC are in input mode and external sync signal is accepted. DISPTMG goes low (disabled).

Notes:

1. When VS = 1, DISPTMG goes low.
2. When TV = 0, indicates master-slave mode. When TV = 1, indicates TV sync mode.
3. In TV sync mode, the horizontal back porch must be set using the horizontal sync pulse width register.
4. In TV sync mode, the internal control is in non-interlace mode.

IB	IL	Interrupt Function
0	0	None
0	1	With light pen strobe
1	0	With vertical blanking
1	1	With light pen or vertical blanking

Note: Interrupt signal is output for CUDISP while DISPTMG is low.

SY	Vertical Sync Position Fine Adjust Function
0	Vertical sync position fine adjust register disabled
1	Vertical sync position fine adjust register enabled

P1	P0	Screen Partition Function
0	0	Start Address 1 enabled
0	1	Start addresses 1 and 2 enabled; screen partitioned into two sections
1	0	Start addresses 1, 2, and 3 enabled; screen partitioned into three sections
1	1	Start addresses 1, 2, 3, and 4 enabled; screen partitioned into four sections

Note: Screen address 1 is always displayed starting from line number 0.

Register Description
(Continued)

Control/Status Register (R31)



Controls the smooth scrolling and raster interpolation functions, and performs read/write of the status register. This register must be initialized by software after reset is released. Control bit functions are as follows:

Control Bits Function

SS3 to SS0	Smooth scrolling control bits; when set to 1 the smooth scrolling register is enabled. Bits correspond to the screens as follows: SS3 = screen 4 SS2 = screen 3 SS1 = screen 2 SS0 = screen 1
RI	Raster interpolation bit. Set to 1, raster interpolation is performed. The raster counter is incremented every two rasters, doubling the vertical sync rate. Therefore, in this case, registers related to vertical sync control must be reprogrammed. The raster interpolation function can't be used in external sync mode and interlace & video mode.

Notes:

- "0s" must be written to lower 3 bits of the control register.
- Refer to diagram of "Double-Size Vertical Display" and item 6 of Notes on Operation.

Status Bits

The functions of status bits are as follows:

E Display Field Status

0	Odd-numbered screen display, or in non-interlace mode
1	Even-numbered screen display

SB Vertical Blanking Status

0	During screen display
1	During vertical blanking

SL Light Pen Strobe Status

0	Light pen strobe ignored
1	Light pen strobe accepted

Notes:

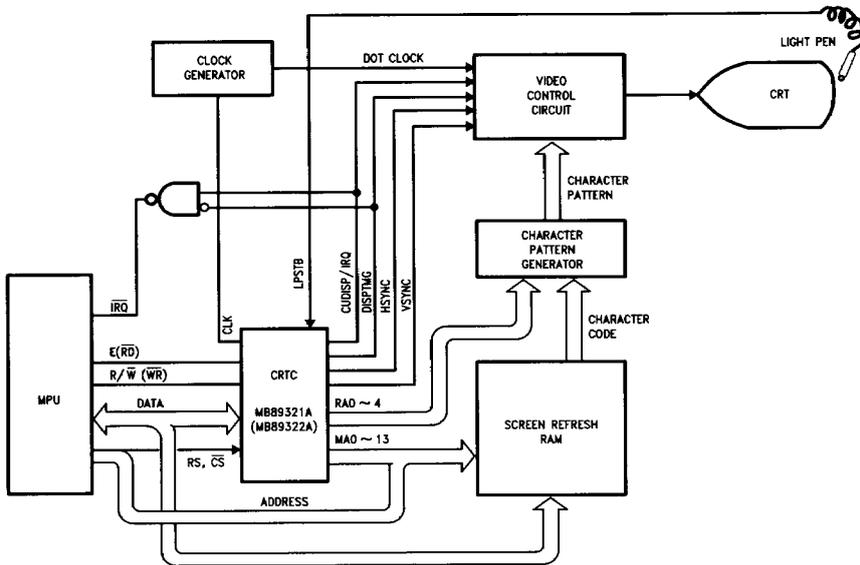
- Light pen strobe status is cleared by reset or by read of the status register.
- Vertical blanking status and light pen strobe status are set regardless of the setting of the control register interrupt function.
- E bit is controlled by the vertical blank. Therefore, E bit status is different from normal field image, and it's update timing changes depending on number of lines displayed. To get correct status, E bit must be read immediately after the display period.

Restrictions on Values Written to Registers

Values which may be written to internal registers are as follows:

- (1) $0 < \text{number of characters displayed in line (R1)} < \text{total number of characters in line (R0)} + 1 \leq 256$
- (2) $0 < \text{number of lines displayed (R6)} < \text{total number of lines (R4)} + 1 \leq 128$
- (3) $0 \leq \text{horizontal sync position (R2)} \leq \text{total number of characters in line (R0)}$
- (4) $0 \leq \text{vertical sync position (R7)} \leq \text{total number of lines (R4)}$
- (5) $0 \leq \text{cursor start raster (R10)} \leq \text{cursor end raster (R11)} \leq \text{maximum raster address (R9)}$
(interlace mode and non-interlace modes)
 $0 \leq \text{cursor start raster (R10)} \leq \text{cursor end raster (R11)} \leq \text{maximum raster address (R9)} + 1$
(interlace & video mode)
- (6) $2 \leq \text{maximum raster address (R9)} \leq 30$
(interlace & video mode only)
- (7) $3 \leq \text{total number of characters in line (R0)}$
(except in non-interlace mode)
 $5 \leq \text{total number of characters in line (R0)}$
(non-interlace mode only)
- (8) Vertical sync position fine adjust (R27) < maximum raster address (R9)
- (9) Smooth scroll (R29) \leq maximum raster address (R9)

System Block Diagram

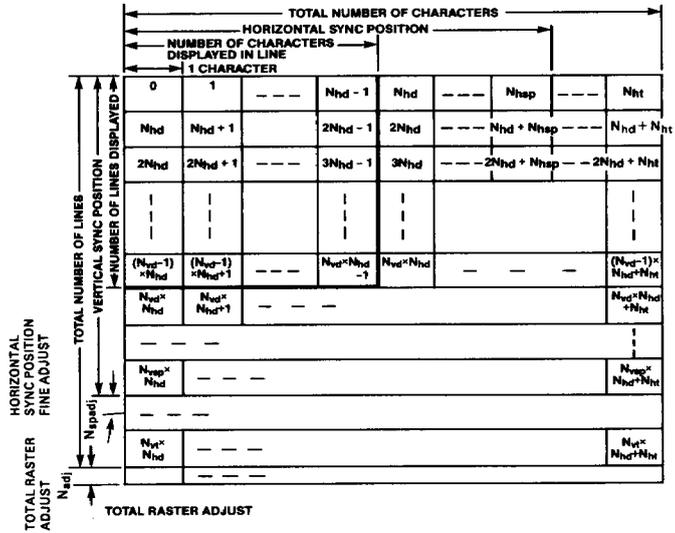


Programmable Values

Programmable values which can be written to registers and their respective symbols are as shown below:

Register Number	Register Name	Programmable Value	Symbol
R0	Total Number of Characters in Line	Characters	Nht
R1	Number of Characters Displayed in Line	Characters	Nhd
R2	Horizontal Sync Position	Characters	Nhsp
R3	Sync Signal Pulse Width	Rasters/Characters	Nvsw/Nhsw
R4	Total Number of Lines	Lines	Nvt
R5	Total Raster Adjust	Rasters	Nadj
R6	Number of Lines Displayed	Lines	Nvd
R7	Vertical Sync Position	Lines	Nvsp
R8	Scan Mode/Skew		
R9	Maximum Raster Address	Rasters	Nr
R10	Cursor Start Raster	Rasters	N _{CSTART}
R11	Cursor End Raster	Rasters	N _{CEND}
R12	Start Address 1		N _{S1}
R13			
R14	Cursor		
R15			
R16	Light Pen		
R17			
R18	Screen 2 Display Start Position	Lines	N _{L2}
R19	Start Address 2		N _{S2}
R20			
R21	Screen 3 Display Start Position	Lines	N _{L3}
R22	Start Address 3		N _{S3}
R23			
R24	Screen 4 Display Start Position	Lines	N _{L4}
R25	Start Address 4		N _{S4}
R26			
R27	Vertical Sync Position Fine Adjust	Rasters	Nspadj
R28	Light Pen Raster		
R29	Smooth Scroll	Rasters	Nradj
R30	Control		
R31	Control/Status		

Screen Format



Line numbers are counted starting at the following addresses:

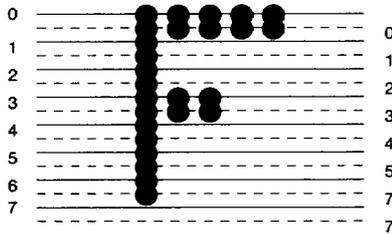
- Line number 0 = starts from memory address 0
- Line number 1 = starts from memory address Nhd
- Line number 2 = starts from memory address 2Nhd

Line number n = starts from memory address (Nvd-1)Nhd

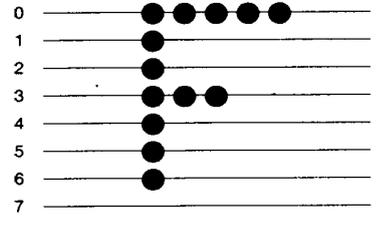
Scan Mode

Examples of format during scan mode:

Interlace Mode



Non-Interlace Mode

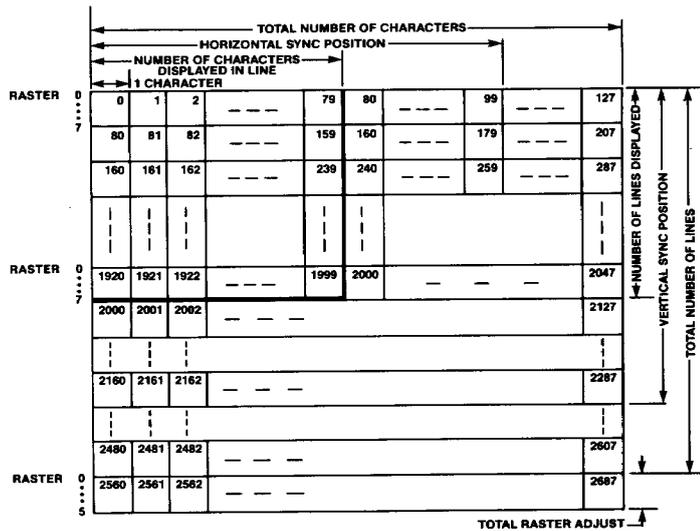


Example of Screen Format

Dot clock rate 16.128 MHz
Horizontal frequency 15.75 kHz
Vertical frequency 60.1145 Hz

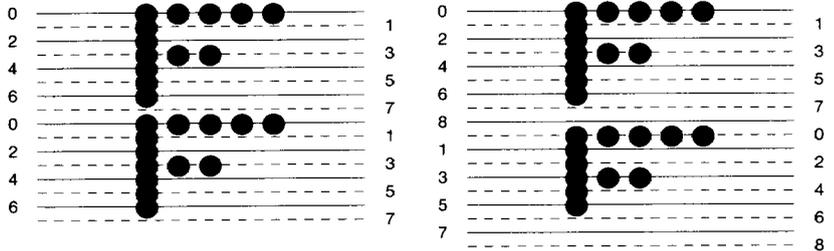
At the following clock rates and register settings, the screen format is as shown in the diagrams below:

Total number of characters in line, Register 0: 127
Number of characters displayed in line, Register 1: 80
Horizontal sync position, Register 2: 99
Sync signal pulse width, Register 3: 8
Total number of lines, Register 4: 31
Total raster adjust, Register 5: 6
Number of lines displayed, Register 6: 25
Vertical sync position, Register 7: 27
Maximum raster address, Register 9: 8



Scan Mode
(Continued)

Interlace & Video Modes

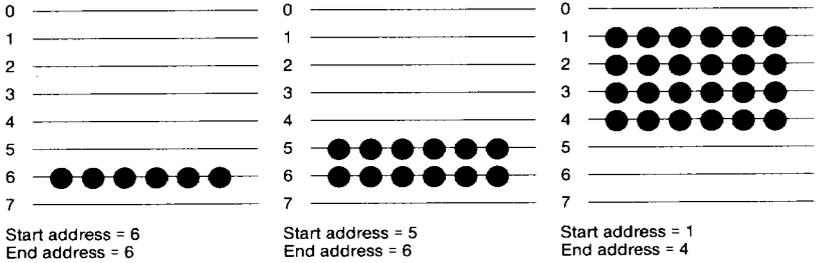


Even number of rasters in a line

Odd number of rasters in a line

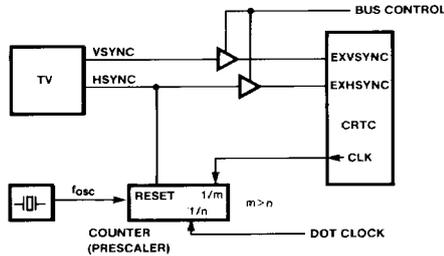
Cursor Control

Examples of settings for the cursor start and end raster registers:



TV Sync Mode

Example of a TV Sync mode circuit:



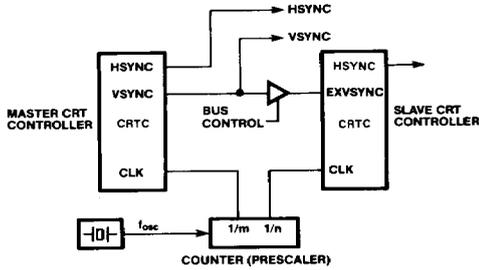
TV sync mode is used to superimpose displays on TV or video signals. In the above example a $1/n$ f_{OSC} dot shift

will occur. Accordingly, an appropriate prescaler should be designed to avoid image resolution problems.

During HSYNC, CLK must be low (stopped).

Master-Slave Mode

Example of a master-slave mode circuit:

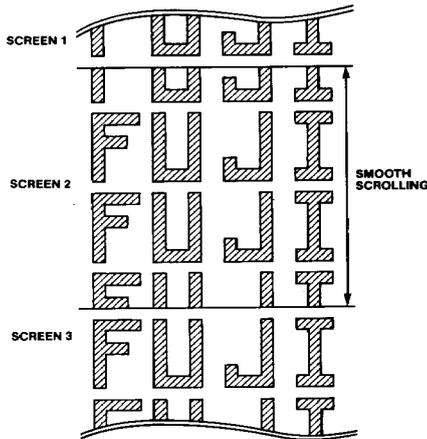


Master-slavemode is used to synchronize master and slave CRT controllers. The screen formats and clock phases of the two CRTCs must match.

Since HSYNC is output, PLL can be used.

Smooth Scroll

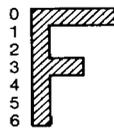
Example of smooth scrolling display:



In the example, screen 2 is being smooth scrolled.

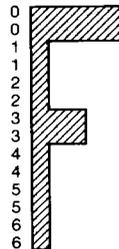
Double-Size Vertical Display

Raster Address



Without raster interpolation function

Raster Address



With raster interpolation function

The vertical size of the display can be doubled using the raster interpolation function as shown in the example.

In raster interpolation, the raster address is updated every second raster.

Refer to item 6 of Notes on Operation.

Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Input Voltage	V _{IN}	-0.3 to +7.0	V
Supply Voltage	V _{CC}	-0.3 to +7.0	V
Operating Ambient Temperature	T _A	-40 to +85	°C
Storage Temperature	T _{STG}	-55 to +150	°C
Power Dissipation	P _D	600	mW

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Parameter	Symbol	Value			Unit
		Min.	Typ.	Max.	
Supply Voltage	V _{CC}	4.5	5.0	5.5	V
	V _{SS}		0.0		V
Input High Voltage	LPSTB, CLK V _{IH1}	2.2		V _{CC}	V
	Other Inputs V _{IH}	2.0		V _{CC}	V
Input Low Voltage	LPSTB, CLK V _{IL1}	-0.3		0.6	V
	Other Inputs V _{IL}	-0.3		0.8	V
Ambient Temperature	T _A	-20	25	+75	°C

DC Characteristics

Recommended operating conditions unless otherwise noted.

Parameter	Symbol	Test Conditions	Value			Unit
			Min	Typ	Max	
Input High Voltage	LPSTB, CLK V _{IH1}		2.2		V _{CC}	V
	Other Inputs V _{IH}		2.0		V _{CC}	V
Input Low Voltage	LPSTB, CLK V _{IL1}		-0.3		0.6	V
	Other Inputs V _{IL}		-0.3		0.8	V
Input Leakage Current	D0 to D7, EXHSYNC, EXVSYNC I _{IL}	V _{IN} = 0.4 V to 2.4 V, V _{CC} = 5.5 V	-10		10	μA
	Other Inputs I _{IL1}	V _{IN} = 0 V to 5.5 V	-2.5		2.5	μA
Output High Voltage	D0 to D7 V _{OH}	I _{OH} = -205 μA	2.4			V
	Other Outputs V _{OH1}	I _{OH} = -100 μA	2.4			V
Output Low Voltage	V _{OL}	I _{OL} = 1.6 mA			0.4	V
Input Capacitance	D0 to D7, EXHSYNC, EXVSYNC C _{IN}	V _{IN} = 0 V			12.5	pF
	Other Outputs C _{IN1}	f = 1.0 MHz			10.0	pF
Output Capacitance	C _{OUT}				10.0	pF
Power Dissipation	P _D	V _{CC} = V _{max} f = 1.0 MHz		10	30	mW

AC Characteristics
Recommended operating conditions unless otherwise noted.

Parameter	Symbol	Conditions	Value			
			Min.	Typ.	Max. Unit	
CRT Controller	Clock Period	t _{CLK}	250		ns	
	Clock High	t _{PWCH}	100		ns	
	Clock Low	t _{PWCL}	100		ns	
	Clock Rise	t _{CR}		20	ns	
	Clock Fall	t _{CF}		20	ns	
	Memory Address Delay	t _{MAD}	(1)	80	ns	
	Raster Address Delay	t _{RAD}		100	ns	
	Display Timing Delay	t _{DTD}		120	ns	
	Cursor Timing Delay	t _{CDD}		120	ns	
	Horizontal Synchronous Delay	t _{HSD}		100	ns	
	Vertical Synchronous Delay	t _{VSD}		120	ns	
External Synchronization	Clock Stop	t _{CLKST}	100		ns	
	External Horizontal Synchronous Signal Width	t _{PWHS}	1000		ns	
	External Horizontal Synchronous Rise	t _{HR}		20	ns	
	External Horizontal Synchronous Fall	t _{HF}		20	ns	
	External Vertical Synchronous Signal Width	*1 t _{PWVS} / t _{PWVSS}	(2)	1220/ 1750	ns	
	External Vertical Synchronous Rise	t _{VR}		20	ns	
	External Vertical Synchronous Fall	t _{VF}		20	ns	
	External Synchronous Setup (Master-slave mode)	t _{VSS}		50	ns	
	Light Pen	Light Pen Strobe Width	t _{PWLP}	60		ns
		Light Pen Strobe Maximum Period	t _{LPDR} / t _{LPDF}		0 70	ns ns
CRT Interface 1	Enable Period	t _E	0.5		μs	
	Enable High	t _{PWEH}	0.22		μs	
	Enable Low	t _{PWEL}	0.21		μs	
	Enable Rise	t _{ER}		20	ns	
	Enable Fall	t _{EF}	[(4) MB89321A only]	20	ns	
	Address Setup	t _{AS}		40	ns	
	Data Delay	t _{DDR}		120	ns	
	Data Access	t _{ACC}		160	ns	
	Address Hold	t _{AH}		10	ns	
	Data Hold	t _H		10	ns	
Data Setup	t _{DSW}		60	ns		

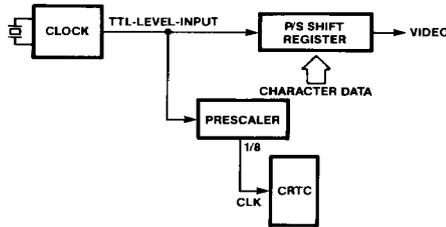
AC Characteristics
(Continued)

Parameter	Symbol	Conditions	Value			Unit	
			Min	Typ	Max		
CPU Interface 2	Read Address Setup	t_{AR}	0			ns	
	Read Low	t_{RR}	160			ns	
	Read Address Hold	t_{RA}	0			ns	
	Write Address Setup	t_{AW}	0			ns	
	Write Low	t_{WW}	{(5)MB89322A only}	190			ns
	Write Address Hold	t_{WA}		0			ns
	Data Delay	t_{RD}			120		ns
	Data Hold	t_{DF}		10			ns
	Data Setup	t_{DW}		60			ns
	Data Hold	t_{WD}		0			ns
	Access Inhibit	t_{DIS}		210			ns
IRQ	Interrupt Delay	t_{IRDF}			150	ns	
	Interrupt Delay *2	t_{IRDR}	(6)		$1/2t_{clk} + 150$	ns	

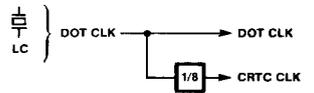
Note: *1. External vertical synchronous signal width $t_{pWVS} = 1000 \text{ ns} + t_{CLK}$ (TV sync mode)
 $t_{pWVS} = 1000 \text{ ns} + 3 t_{CLK}$ (Master slave mode)
 *2. Rising delay time when light pen strobe input in non display time

Clock

A TTL-level input from DC to 4.5 MHz character clock should be used. An example of the clock circuit is shown below.

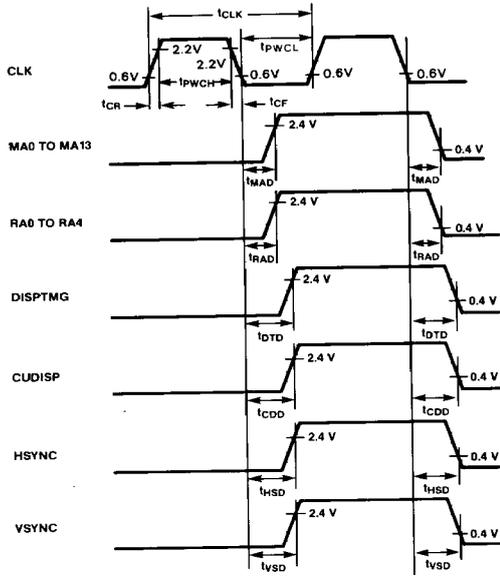


A circuit example for horizontal 8-dot character mode is as follows:

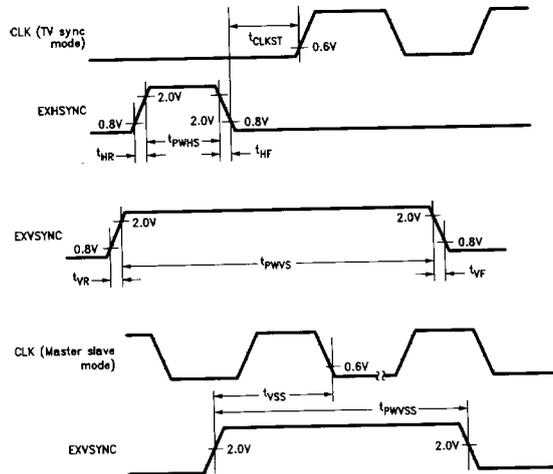


Timing Diagrams

(1) CRT Controller

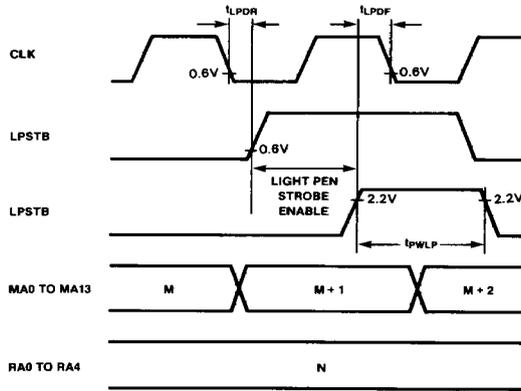


(2) External synchronization



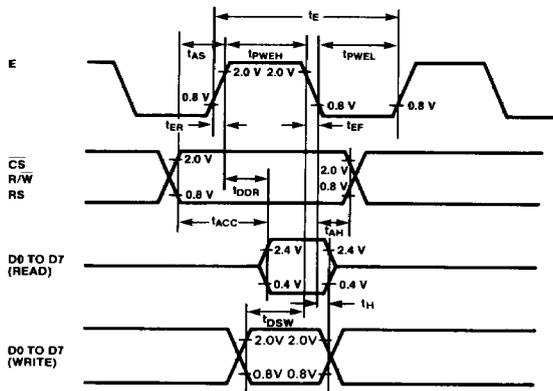
Timing Diagrams
(Continued)

(3) Light Pen



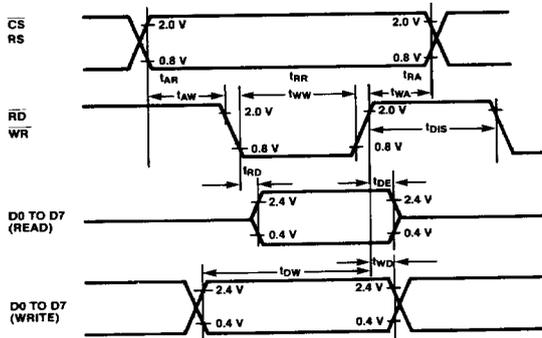
When the light pen strobe is enabled, LPSTB goes high, M+2 is loaded into the light pen raster register, N into the light pen raster register, and the display status bit is set.

(4) CPU Interface 1 (MB89321A only)

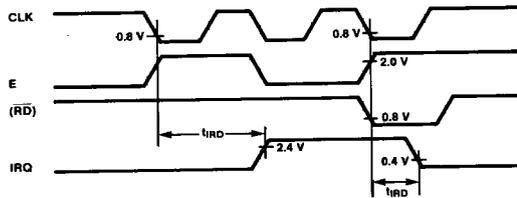


Timing Diagrams
(Continued)

(5) CPU Interface 2 (MB89322A only)

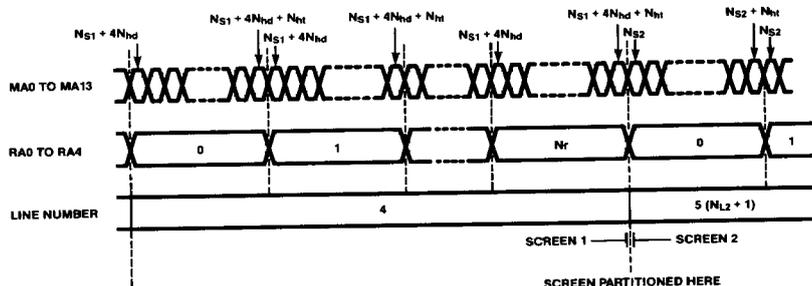


(6) IRQ Timing



Notes on Operation

(1) Screen Partitioning Timing

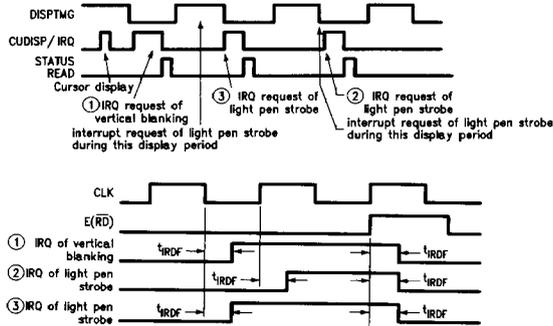


This example shows typical memory addresses and raster addresses of screens 1 and 2 during screen partitioning.

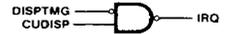
- Nht: Total Number of Characters in Line (R0)
- Nhd: Number of Characters Displayed in Line (R1)
- Nr : Maximum Raster Address (R9)
- Ns1: Start Address 1 (R12, R13)
- NL2: Screen 2 Display Start Position (R18)
- NS2: Start Address 2 (R19, R20)

Notes on Operation
(Continued)

(2) Interrupt Signal Generator Timing

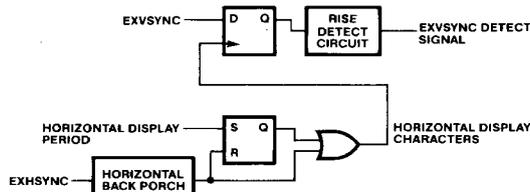


The interrupt signal is output to the CUDISP pin during display blanking. The interrupt signal can be generated as shown in the diagram below.



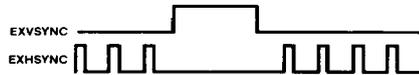
When the cursor is not enabled, the CUDISP pin functions as IRQ.

(3) TV Sync Timing

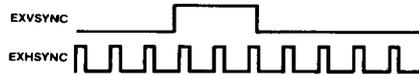


In TV sync mode, EXHSYNC is enabled when a pulse of 1,000 ns or more is applied. Also, during vertical blanking, EXVSYNC is enabled to sync the controller's internal horizontal display period. In order to use the TV sync function, a horizontal display period should be set. The basic circuit required to do this is shown to the left.

Note: Low (enabled) during the horizontal display period.



The TV sync function may not operate under the timing shown here at the immediate left.



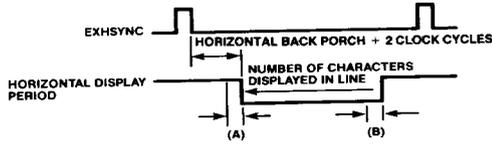
The TV sync function is activated using the timing as shown here.



Notes on Operation
(Continued)

(4) Horizontal Display Period Setting (TV Sync Mode)

The horizontal display period is determined by the timing diagrams below:



(A) and (B) indicate points where EXVSYNC is detected.

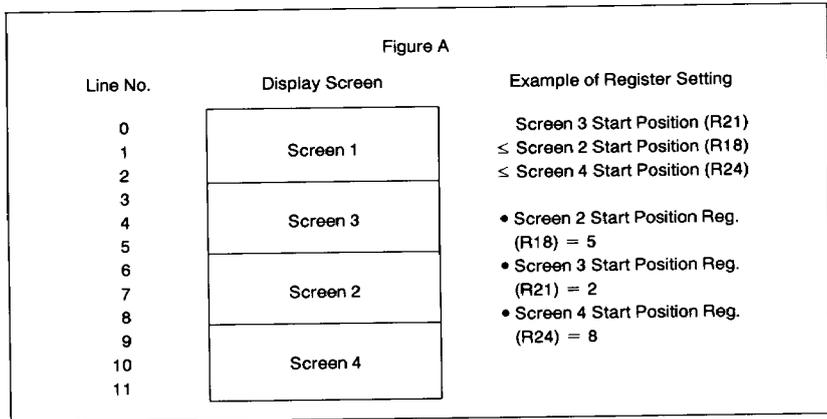
EXVSYNC is normally detected at (B). However, when EXVSYNC is generated during the horizontal display period by an equivalent pulse, detection is at (A).

(A) and (B) require at least 1,000 ns + 1 clock cycle, during which period EXVSYNC must be maintained.

(5) Screen Partitioning

The display order of partitioned screens can be changed by programming the start position registers (R18, R21, and R24) for each partitioned screen, except screen 1, which is always displayed from line 0 on the screen. (See Figure A below.)

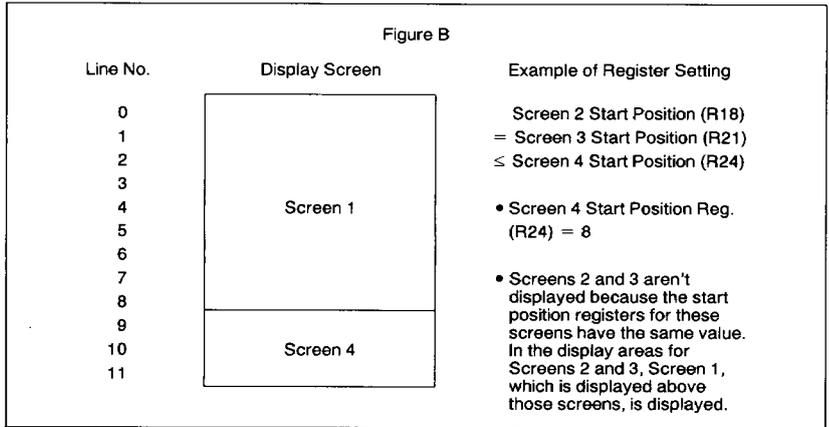
But, when the same values are programmed to the start position registers, the partitioned screens for those start position registers aren't displayed, even if those partitioned screens are enabled by P0 and P1 bits.



Notes on Operation
(Continued)

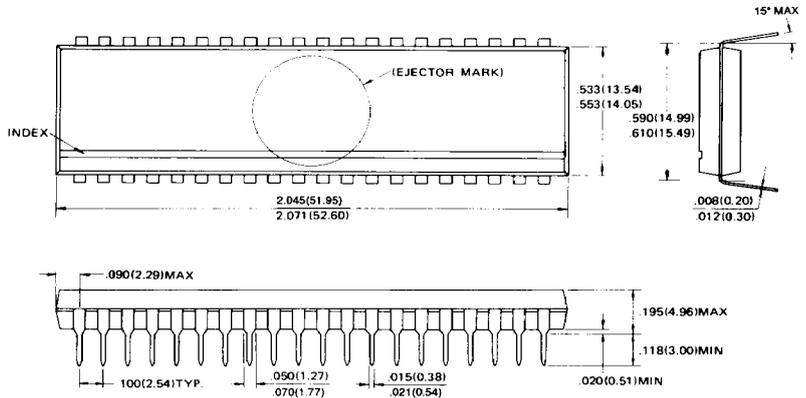
(6) Raster Interpolation

At present, two versions of MB89321A/89322A are provided: One has the raster interpolation function, and another has no raster interpolation function. On MB89321A/89322A without the raster interpolation function, "0" must always be written to RI bit of the control/status register (R31).



Package Dimensions
Dimensions in inches
(millimeters)

**40-Lead Plastic
Dual In-Line Package
(Case No.: DIP-40P-M01)**



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