*Designer's™ Data Sheet*
# TMOS E-FET ™
# High Energy Power FET
# D2PAK for Surface Mount
## N–Channel Enhancement–Mode Silicon Gate

The D2PAK package has the capability of housing a larger die than any existing surface mount package which allows it to be used in applications that require the use of surface mount components with higher power and lower $R_{DS(on)}$ capabilities. The D2PAK contains an advanced TMOS E–FET die designed to withstand high energy in the avalanche mode and switch efficiently. This device is designed for use in low voltage, high speed switching applications such as power supplies, dc/dc converters, PWM motor controls or any application where the MOSFET will be operating into an inductive load.

- Avalanche Energy Capability Specified
- Low Stored Gate Charge for Efficient Switching
- Replace External Zener Transient Suppressor — Absorbs High Energy in the Avalanche Mode
- Specially Designed Leadframe for Maximum Power Dissipation
- Available in 24 mm 13–inch/800 Unit Tape & Reel, Add T4 Suffix to Part Number
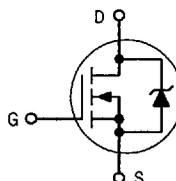
## MTB50N06E
Motorola Preferred Device

**TMOS POWER FET**
**50 AMPERES**
**$R_{DS(on)}$ = 0.025 OHM**
**60 VOLTS**

CASE 418B–02, Style 2
D2PAK

**MAXIMUM RATINGS** ($T_C$ = 25°C unless otherwise noted)

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Drain–Source Voltage | $V_{DSS}$ | 60 | Vdc |
| Drain–Gate Voltage ($R_{GS}$ = 1.0 MΩ) | $V_{DGR}$ | 60 | Vdc |
| Gate–Source Voltage — Continuous | $V_{GS}$ | ±20 | Vdc |
| Drain Current — Continuous<br>— Continuous @ 100°C<br>— Single Pulse ($t_p$ ≤ 10 μs) | $I_D$<br>$I_D$<br>$I_{DM}$ | 50<br>29<br>160 | Adc<br><br>Apk |
| Total Power Dissipation<br>Derate above 25°C<br>Total Power Dissipation @ $T_A$ = 25°C, when mounted with the minimum recommended pad size | $P_D$ | 125<br>1.0<br>2.5 | Watts<br>W/°C<br>Watts |
| Operating and Storage Temperature Range | $T_J$, $T_{stg}$ | –55 to 150 | °C |
| Single Pulse Drain–to–Source Avalanche Energy — Starting $T_J$ = 25°C<br>($V_{DD}$ = 25 Vdc, $V_{GS}$ = 10 Vpk, $I_L$ = 50 Apk, L = 0.32 mH, $R_G$ = 25 Ω ) | $E_{AS}$ | 400 | mJ |
| Thermal Resistance — Junction to Case<br>— Junction to Ambient<br>— Junction to Ambient, when mounted with the minimum recommended pad size | $R_{θJC}$<br>$R_{θJA}$<br>$R_{θJA}$ | 1.0<br>62.5<br>50 | °C/W |
| Maximum Lead Temperature for Soldering Purposes, 1/8" from case for 10 seconds | $T_L$ | 260 | °C |

**Designer's Data for "Worst Case" Conditions** — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

**Preferred** devices are Motorola recommended choices for future use and best overall value.

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## ELECTRICAL CHARACTERISTICS ($T_J$ = 25°C unless otherwise noted)

| Characteristic | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | | |
| Drain–Source Breakdown Voltage ($V_{GS}$ = 0 V, $I_D$ = 250 μAdc) Temperature Coefficient (Positive) | $V_{(BR)DSS}$ | 60 — | — 65 | — — | Vdc mV/°C |
| Zero Gate Voltage Drain Current ($V_{DS}$ = 60 Vdc, $V_{GS}$ = 0) ($V_{DS}$ = 60 Vdc, $V_{GS}$ = 0, $T_J$ = 125°C) | $I_{DSS}$ | — — | — — | 10 100 | μAdc |
| Gate–Body Leakage Current ($V_{GS}$ ±20 Vdc, $V_{DS}$ = 0) | $I_{GSS}$ | — | — | 100 | nAdc |
| **ON CHARACTERISTICS (1)** | | | | | |
| Gate Threshold Voltage ($V_{DS}$ = $V_{GS}$, $I_D$ = 250 μAdc) Temperature Coefficient (Negative) | $V_{GS(th)}$ | 2.0 — | 2.8 7.0 | 4.0 — | Vdc mV/°C |
| Static Drain–Source On–Resistance ($V_{GS}$ = 10 Vdc, $I_D$ = 25 Adc) | $R_{DS(on)}$ | — | 0.020 | 0.025 | Ohm |
| Drain–Source On–Voltage ($V_{GS}$ = 10 Vdc) ($I_D$ = 50 Adc) ($I_D$ = 25 Adc, $T_J$ = 125°C) | $V_{DS(on)}$ | — — | 1.0 0.75 | 1.5 1.35 | Vdc |
| Forward Transconductance ($V_{DS}$ = 15 Vdc, $I_D$ = 25 Adc) | $g_{FS}$ | 17 | 32 | — | mhos |
| **DYNAMIC CHARACTERISTICS** | | | | | |
| Input Capacitance | ($V_{DS}$ = 25 Vdc, $V_{GS}$ = 0, f = 1.0 MHz) See Figure 14 | $C_{iss}$ | — | 2500 | 3500 | pF |
| Output Capacitance | | $C_{oss}$ | — | 1000 | 1400 | |
| Reverse Transfer Capacitance | | $C_{rss}$ | — | 250 | 500 | |
| **SWITCHING CHARACTERISTICS (2)** | | | | | |
| Turn–On Delay Time | ($V_{DD}$ = 25 Vdc, $I_D$ = 50 Adc, $V_{GS}$ = 10 Vdc, $R_G$ = 9.1 Ω) | $t_{d(on)}$ | — | 23 | 46 | ns |
| Rise Time | | $t_r$ | — | 160 | 320 | |
| Turn–Off Delay Time | | $t_{d(off)}$ | — | 70 | 140 | |
| Fall Time | | $t_f$ | — | 120 | 240 | |
| Gate Charge | ($V_{DS}$ = 48 Vdc, $I_D$ = 50 Adc, $V_{GS}$ = 10 Vdc) | $Q_T$ | — | 75 | 100 | nC |
| | | $Q_1$ | — | 15 | — | |
| | | $Q_2$ | — | 45 | — | |
| | | $Q_3$ | — | 30 | — | |
| **SOURCE–DRAIN DIODE CHARACTERISTICS** | | | | | |
| Forward On–Voltage | ($I_S$ = 50 Adc, $V_{GS}$ = 0) ($I_S$ = 50 Adc, $V_{GS}$ = 0, $T_J$ = 125°C) | $V_{SD}$ | — — | 1.2 1.1 | 2.5 — | Vdc |
| Reverse Recovery Time | ($I_S$ = 50 Adc, $V_{GS}$ = 0, $dI_S/dt$ = 100 A/μs) | $t_{rr}$ | — | 120 | — | ns |
| **INTERNAL PACKAGE INDUCTANCE** | | | | | |
| Internal Drain Inductance (Measured from top to center of die) | $L_D$ | — | 3.5 | — | nH |
| Internal Source Inductance (Measured from the source lead 0.1″ from package to source bond pad) | $L_S$ | — | 7.5 | — | nH |

(1)  Pulse Test: Pulse Width ≤ 300 μs max, Duty Cycle ≤ 2%.
(2)  Switching characteristics are independent of operating junction temperature.

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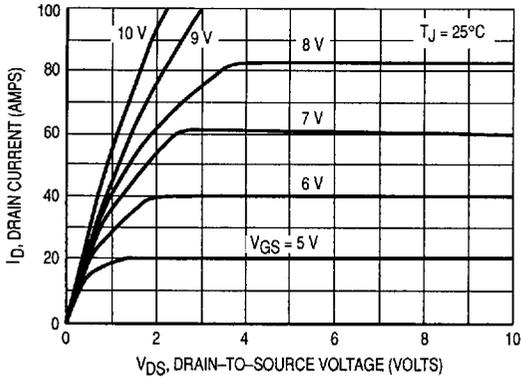## TYPICAL ELECTRICAL CHARACTERISTICS


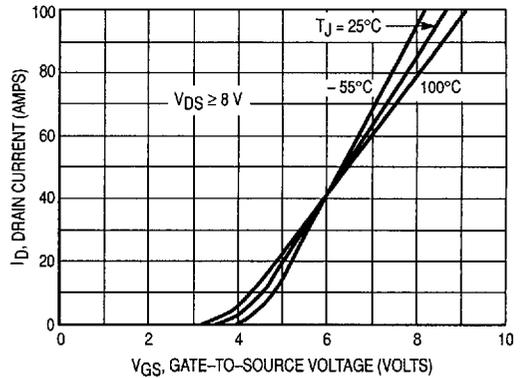
**Figure 1. On–Region Characteristics**



**Figure 2. Transfer Characteristics**
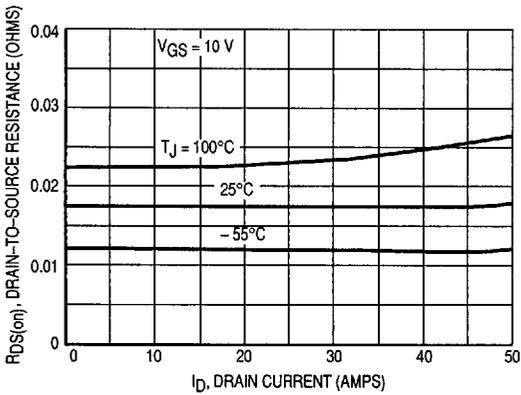


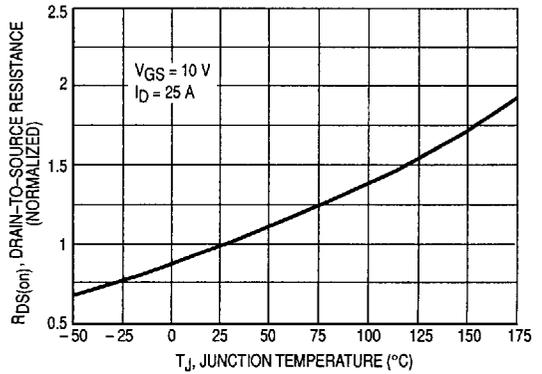**Figure 3. On–Resistance versus Drain Current and Temperature**
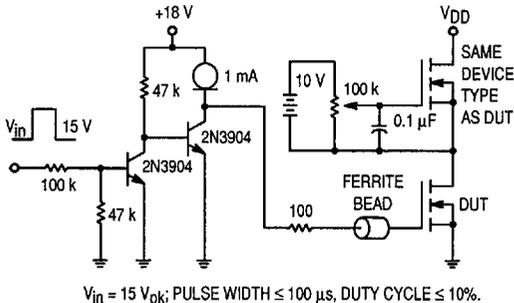


**Figure 4. On–Resistance Variation With Temperature**



$V_{in}$ = 15 $V_{pk}$; PULSE WIDTH ≤ 100 μs, DUTY CYCLE ≤ 10%.

**Figure 5. Gate Charge Test Circuit**
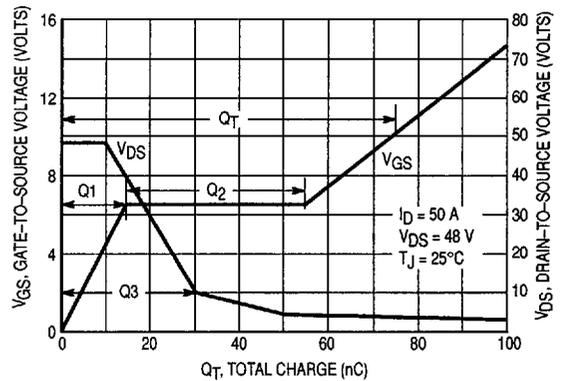


**Figure 6. Gate–to–Source and Drain–to–Source Voltage versus Total Charge**

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## POWER MOSFET SWITCHING

Switching behavior is most easily modeled and predicted by recognizing that the power MOSFET is charge controlled. The lengths of various switching intervals ($\Delta t$) are determined by how fast the FET input capacitance can be charged by current from the generator.

The published capacitance data is difficult to use for calculating rise and fall because drain–gate capacitance varies greatly with applied voltage. Accordingly, gate charge data is used. In most cases, a satisfactory estimate of average input current ($I_{G(AV)}$) can be made from a rudimentary analysis of the drive circuit so that

$$t = Q/I_{G(AV)}$$

During the rise and fall time interval when switching a resistive load, $V_{GS}$ remains virtually constant at a level known as the plateau voltage, $V_{SGP}$. Therefore, rise and fall times may be approximated by the following:

$$t_r = Q_2 \times R_G/(V_{GG} - V_{GSP})$$

$$t_f = Q_2 \times R_G/V_{GSP}$$

where

$V_{GG}$ = the gate drive voltage, which varies from zero to $V_{GG}$

$R_G$ = the gate drive resistance

and $Q_2$ and $V_{GSP}$ are read from the gate charge curve.

During the turn–on and turn–off delay times, gate current is not constant. The simplest calculation uses appropriate values from the capacitance curves in a standard equation for voltage change in an RC network. The equations are:

$$t_{d(on)} = R_G \, C_{iss} \ln [V_{GG}/(V_{GG} - V_{GSP})]$$

$$t_{d(off)} = R_G \, C_{iss} \ln (V_{GG}/V_{GSP})$$

The capacitance ($C_{iss}$) is read from the capacitance curve at a voltage corresponding to the off–state condition when calculating $t_{d(on)}$ and is read at a voltage corresponding to the on–state when calculating $t_{d(off)}$.

At high switching speeds, parasitic circuit elements complicate the analysis. The inductance of the MOSFET source lead, inside the package and in the circuit wiring which is common to both the drain and gate current paths, produces a voltage at the source which reduces the gate drive current. The voltage is determined by Ldi/dt, but since di/dt is a function of drain current, the mathematical solution is complex. The MOSFET output capacitance also complicates the mathematics. And finally, MOSFETs have finite internal gate resistance which effectively adds to the resistance of the driving source, but the internal resistance is difficult to measure and, consequently, is not specified.

The resistive switching time variation versus gate resistance (Figure 8) shows how typical switching performance is affected by the parasitic circuit elements. If the parasitics were not present, the slope of the curves would maintain a value of unity regardless of the switching speed. The circuit used to obtain the data is constructed to minimize common inductance in the drain and gate circuit loops and is believed readily achievable with board mounted components. Most power electronic loads are inductive; the data in the figure is taken with a resistive load, which approximates an optimally snubbed inductive load. Power MOSFETs may be safely operated into an inductive load; however, snubbing reduces switching losses.
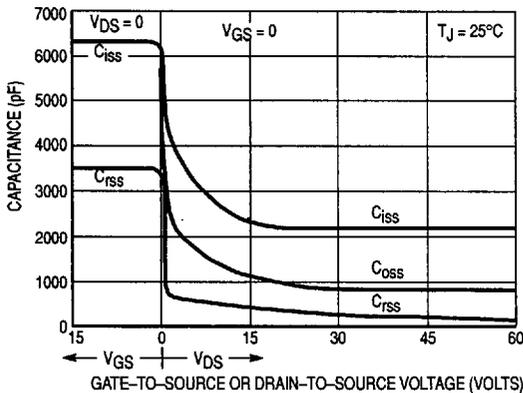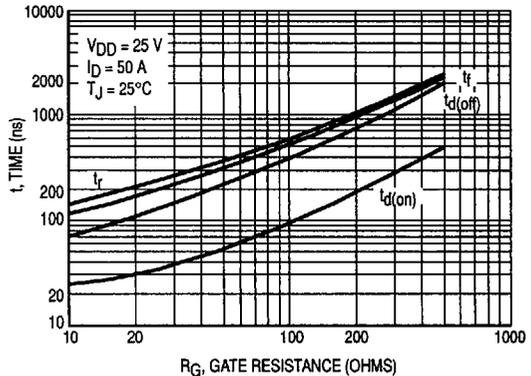


**Figure 7. Capacitance Variation**



**Figure 8. Resistive Switching Time Variation versus Gate Resistance**

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## SAFE OPERATING AREA INFORMATION

### FORWARD BIASED SAFE OPERATING AREA

The FBSOA curves define the maximum drain–to–source voltage and drain current that a device can safely handle when it is forward biased, or when it is on, or being turned on. Because these curves include the limitations of simultaneous high voltage and high current, up to the rating of the device, they are especially useful to designers of linear systems. The curves are based on a case temperature of 25°C and a maximum junction temperature of 150°C. Limitations for repetitive pulses at various case temperatures can be determined by using the thermal response curves. Motorola Application Note, AN569, "Transient Thermal Resistance–General Data and Its Use" provides detailed instructions.
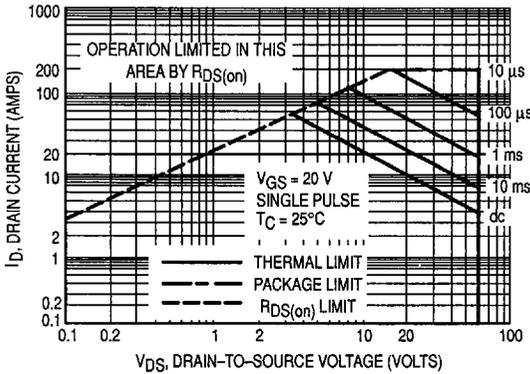


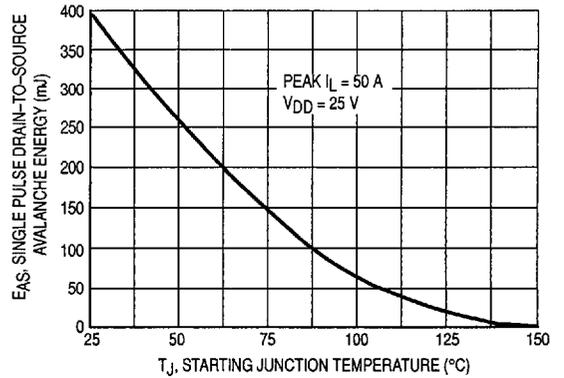Figure 9. Maximum Rated forward Biased Safe Operating Area



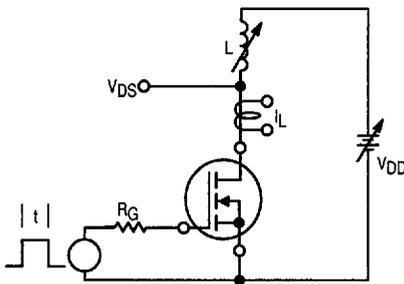Figure 10. Maxium Avalanche Energy versus Starting Junction Temperature
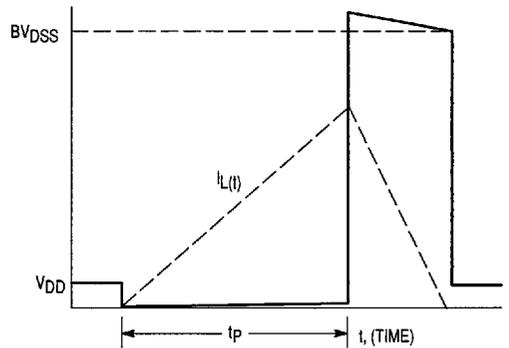


Figure 11. Unclamped Inductive Switching Test Circuit



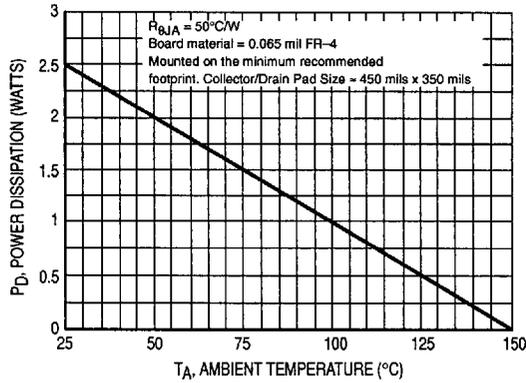Figure 12. Unclamped Inductive Switching Waveforms
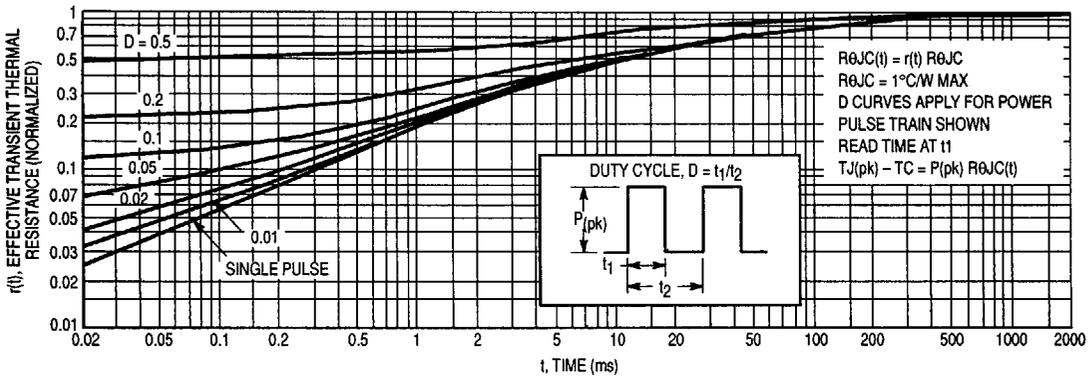
**Figure 13. D²PAK Power Derating Curve**



**Figure 14. Thermal Response**

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