STORAGE

Marvell Solutions

88SM4140

Serial ATA 3.0 Gbps: 1-to-4 Port Multiplier

Preliminary Specifications

Doc No. MV-S101553-00 Rev. G

February 1, 2007

MOVING FORWARD FASTER®

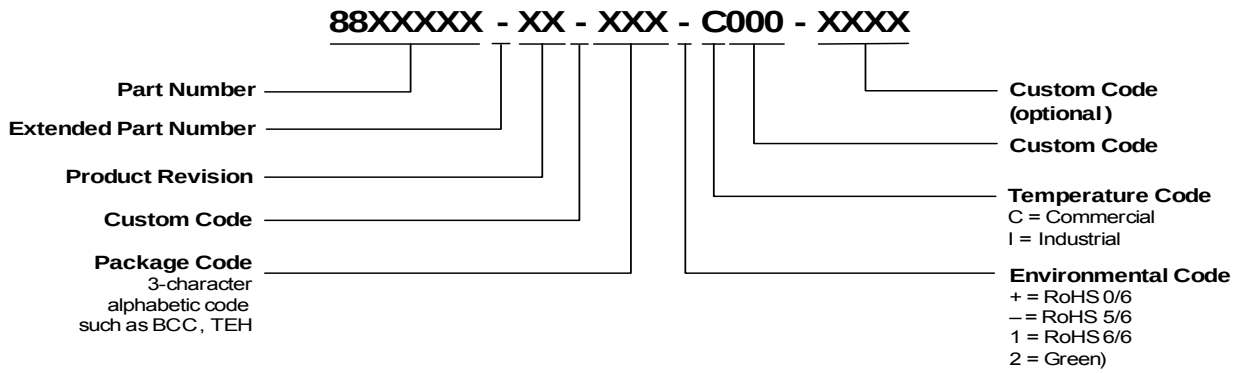
MARVELL®

ORDERING INFORMATION

Ordering Part Numbers and Package Markings

The following figure shows the ordering part numbering scheme for the 88SM4140 part. For complete ordering information, contact your Marvell FAE or sales representative.

Sample Ordering Part Number



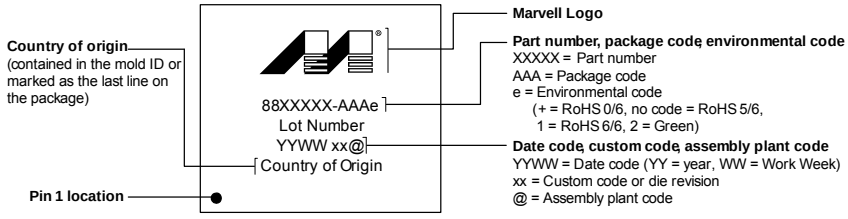
The standard ordering part numbers for the respective solutions are indicated in the following table.

Ordering Part Numbers

Part Number	Description
88SM4140C1-LAD1C000	LQFP 12 mm x 12 mm 80L ePad.

The next figure shows a typical Marvell package marking.

88SM4140 Package Marking and Pin 1 Location



Note: The above drawing is not drawn to scale. The location of markings is approximate. Add-on marks are not represented. Flip chips vary widely in their markings and flip chip examples are not shown here.

THIS PAGE LEFT INTENTIONALLY BLANK

CHANGE HISTORY

The following table identifies the document change history for Rev. G.

Document Changes *

Location	Type	Description	Date
Page 9-18	Update	Added register R0002h S-Control/SM-Control.	09-Jan-07
Page A-13	Update	Corrected the following value in A.4.13, “How Do I Access the SEMB?.” from: TESTMODE[1:0] = 1h to: TESTMODE[1:0] = 2h	18-Jan-07
Page B-1	Update	Replaced Figure B-1 with an updated assembly view.	26-Jan-07
Page B-2	Update	Corrected the pin configuration settings in Table B-2.	26-Jan-07
Page E-1	Update	Added Appendix E.	25-Jan-07

*The type of change is categorized as Param, Rev., or Update. A Param, or parameter, change is one that includes spec value changes. A Rev, or revision, change is one that originated from the chip Revision Notice, and an update change includes all other document updates.

THIS PAGE LEFT INTENTIONALLY BLANK

CONTENTS

THIS PAGE LEFT INTENTIONALLY BLANK

1 OVERVIEW

The 88SM4140 is a Serial ATA (SATA) Port Multiplier (PM) that allows an active host connection to communicate with up to four device ports and one SEMB port. The 88SM4140 is used to consolidate the capacity of storage devices by allowing a single host SATA port to be connected to more than one SATA device. This port multiplier employs Marvell's SATA 3.0 Gbps Physical Layer (Phy) technology.

The 88SM4140 recognizes the SATA-defined OOB sequence and speed negotiation sequence on all five of its SATA ports, and has programmable amplitude and pre-emphasis settings for a range of drive capabilities to support various backplane and cabling environments. The arbiter receives all the requests from the host port, the device ports, and the control port if these ports can transmit a FIS to the host port. The control port has the highest arbitration priority. The priority of the other ports is determined by a fair priority algorithm.

All device ports and the host port can be set up via the host port or UART interface to perform Serial ATA self-tests at the same time.

The PHYTEST module is specifically used to test the Serial ATA Phy. All the test patterns are referenced from SATA Test Patterns and the High Speed Serialized Attachment specification.

Figure 1-1 88SM4140 Overview

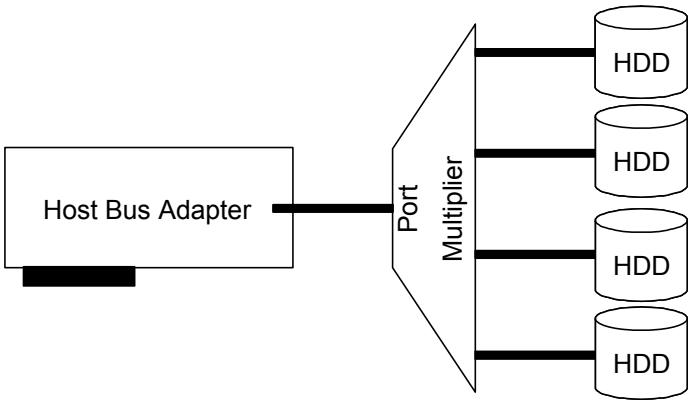
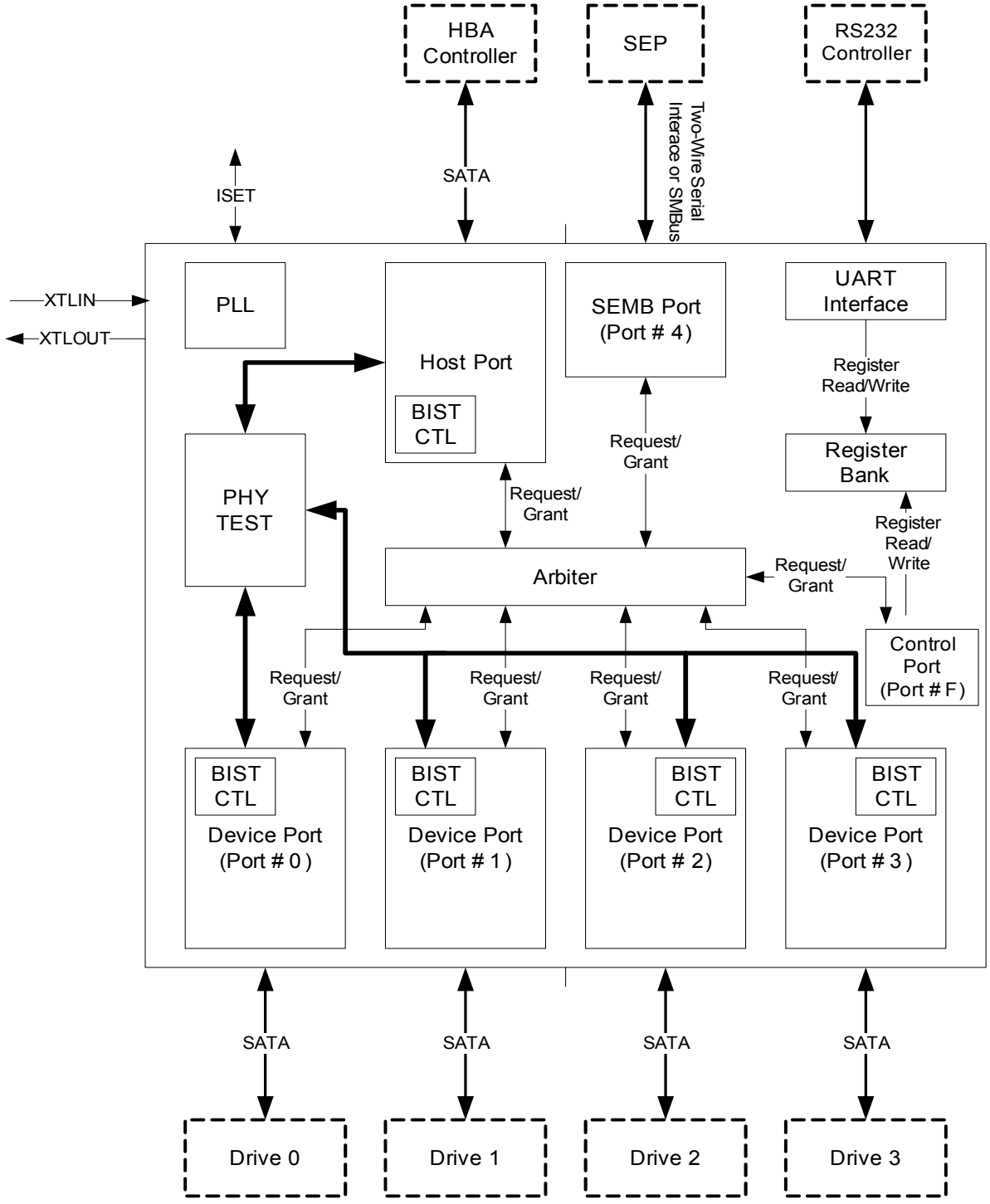


Figure 1-2 88SM4140 Block Diagram



2 FEATURES

2.1 General

- 0.15 µm CMOS technology.
- Supports SATA 1.5 Gbps and SATA 3.0 Gbps communication speed on host and device ports.
- 1.2V and 3.3V power.
- 80-pin LQFP ePad package.
- Phy test mode.
- Full scan for high production test coverage and Phy self-test.
- One host port.
- Four device ports.
- Supports 20 MHz, 25 MHz, 30 MHz, and 40 MHz reference clocks.

2.2 Functional

The 88SM4140 supports the following features:

- Issuing $PMREQ_P$ to host.
- 57600 bps UART access.
- Spread-spectrum clocking transmission.
- Serial ATA BIST over host and device links.
- Asynchronous notification.
- SAF-TE (Enclosure Management).
- FIS-based switching in conjunction with the following Marvell SATA host controllers:
  - 88SX6042
  - 88SX7042
  - 88SE6145
  - 88SE6121
- Marvell Specific Mode (optional).
  - Queued command-based switching mode for Marvell 88SX6041 and 88SX6081.
- One SEMB port/SM bus port (optional).

THIS PAGE LEFT INTENTIONALLY BLANK

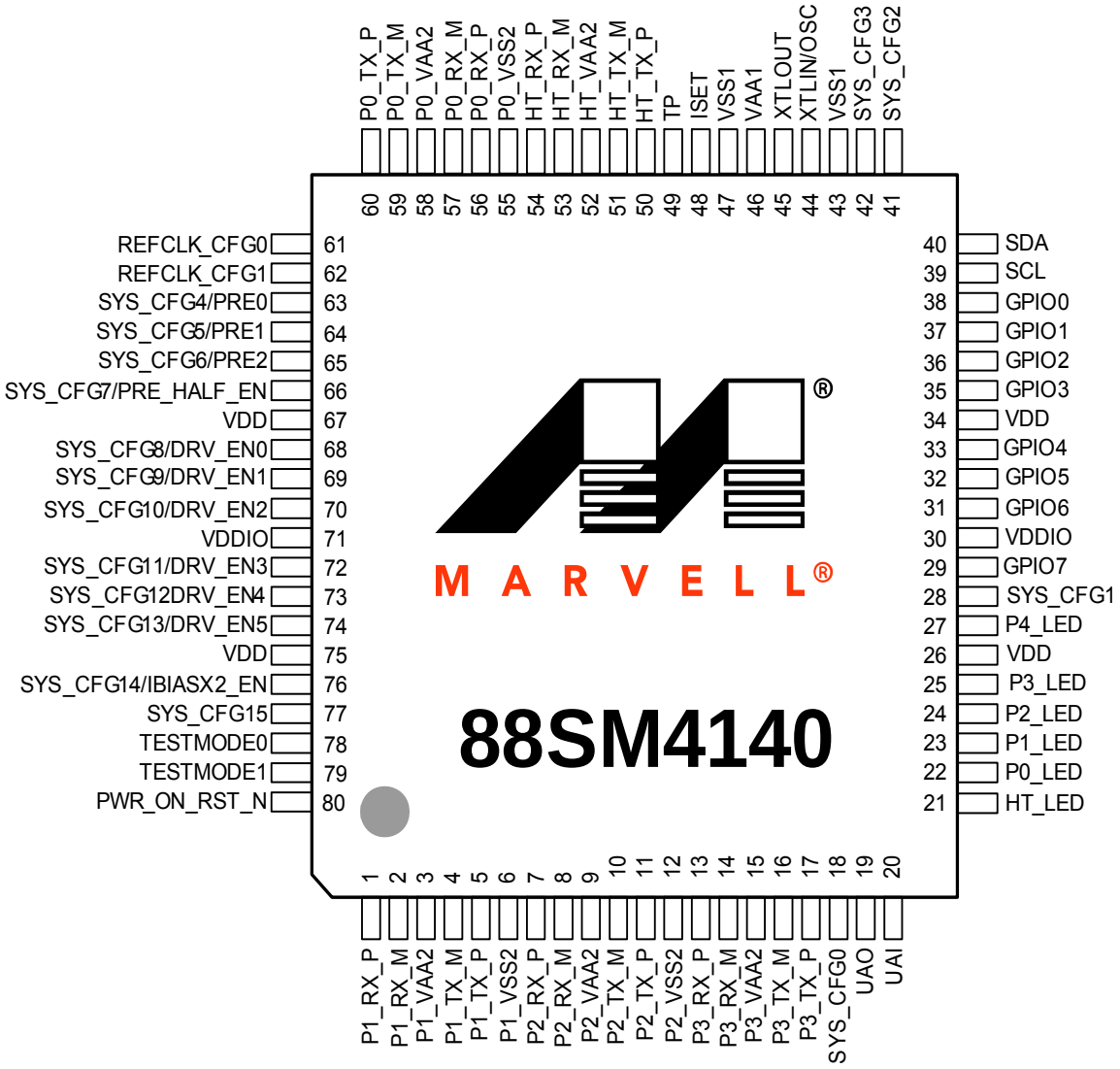
February 1, 2007
Doc No. MV-S101553-00 Rev. G

3 PACKAGE

- Package Pin-Out
- Package Dimensions
- Pin Descriptions

3.1 Package Pin-Out

Figure 3-1 Package Pin-out (80-pin LQFP)



3.2 Package Dimensions

Figure 3-2 Mechanical Dimensions Part 1

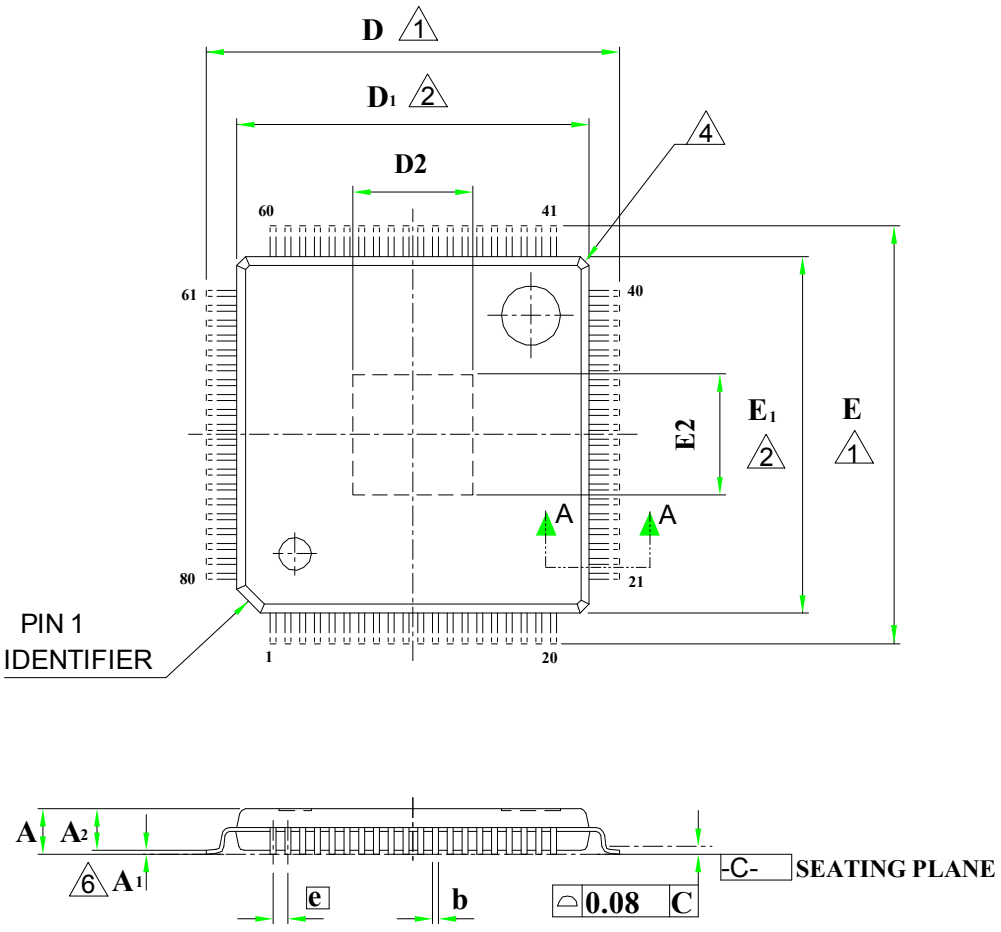


Figure 3-3 Mechanical Dimensions Part 2

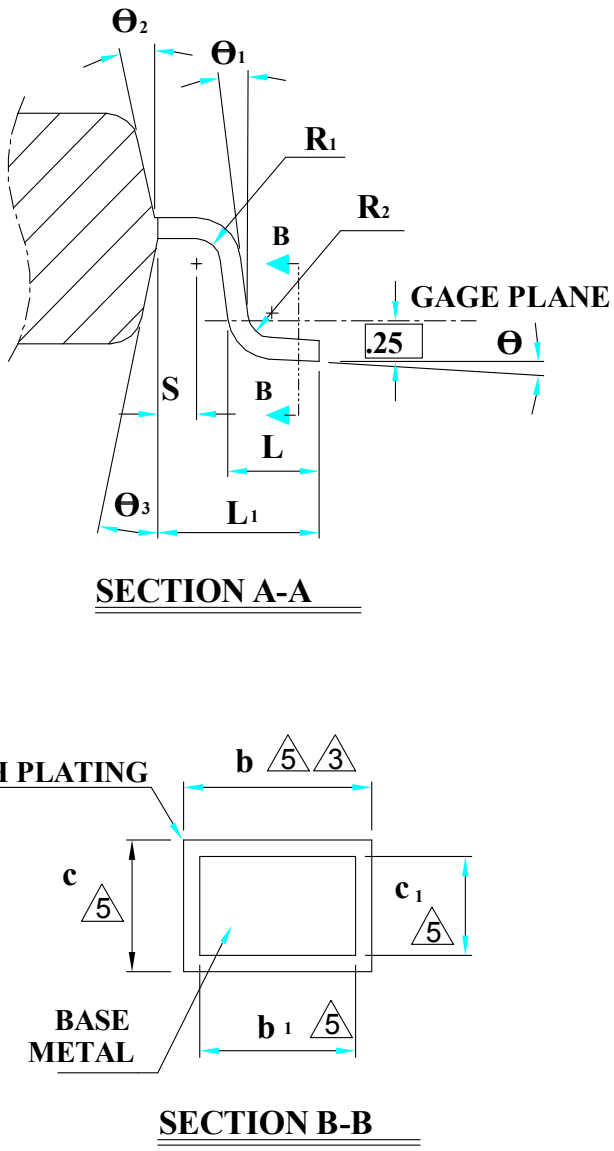


Figure 3-4 Mechanical Dimensions Part 3

Symbol	Dimension in mm			Dimension in inch		
	Min	Nom	Max	Min	Nom	Max
A	—	—	1.60	—	—	0.063
A_1	0.05	—	0.15	0.002	—	0.006
A_2	1.35	1.40	1.45	0.053	0.055	0.057
b	0.17	0.22	0.27	0.007	0.009	0.011
b_1	0.17	0.20	0.23	0.007	0.008	0.009
c	0.09	—	0.20	0.004	—	0.008
c_1	0.09	—	0.16	0.004	—	0.006
D	14.00 BSC			0.551 BSC		
D_1	12.00 BSC			0.472 BSC		
E	14.00 BSC			0.551 BSC		
E_1	12.00 BSC			0.472 BSC		
e	0.50 BSC			0.020 BSC		
L	0.45	0.60	0.75	0.018	0.024	0.030
L_1	1.00 REF			0.039 REF		
R_1	0.08	—	—	0.003	—	—
R	0.08	—	0.20	0.003	—	0.008
S	0.20	—	—	0.008	—	—
θ	0°	3.5°	7°	0°	3.5°	7°
$θ_1$	0°	—	—	0°	—	—
$θ_2$	11°	12°	13°	11°	12°	13°
$θ_3$	11°	12°	13°	11°	12°	13°

Exposed Die Pad Size		
Symbol	Dimension in mm	Dimension in inch
D2	4.06+/-0.20	0.160+/-0.008
E2	4.06+/-0.20	0160+/-0.008

NOTE:

△ 1. TO BE DETERMINED AT SEATING PLANE -C- .

△ 2. DIMENSIONS D 1 AND E 1 DO NOT INCLUDE MOLD PROTRUSION . D1 AND E 1 ARE MAXIMUM PLASTIC BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH .

△ 3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION . DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OF THE FOOT .

△ 4. EXACT SHAPE OF EACH CORNER IS OPTIONAL .

△ 5. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10 mm AND 025 mm FROM THE LEAD TIP .

△ 6. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY .

7. CONTROLLING DIMENSION : MILLIMETER.

8. REFERENCE DOCUMENT : JEDEC MS -026.

3.3 Pin Descriptions

3.3.1 Pin Type Definitions

This section outlines the 88SM4140 pin descriptions. All signals ending with the letter N indicate an active-low signal. Pin type definitions are shown in the following table.

Table 3-1 Pin Type Definitions

Pin Type	Definition
I/O	Input and output
I	Input only
O	Output only
PD	Internal pull-down resistor (100 kΩ)
PU	Internal pull-up resistor (100 kΩ)
mA	DC sink capability
5	5V olerance t

3.3.2 Pin List

Table 3-2 Signal Interface Pins

Signal Name	Signal Number	Type	Description
Port 0 Signal Interface			
P0_TX_P	60	O	Device Port 0. Transmit Data. Differential analog output.
P0_TX_M	59	O	Device Port 0. Transmit Data. Differential analog output.
P0_RX_P	56	I	Device Port 0. Receive Data. Differential analog input.
P0_RX_M	57	I	Device Port 0. Receive Data. Differential analog input.
Port 1 Signal Interface			
P1_TX_P	5	O	Device Port 1. Transmit Data. Differential analog output.
P1_TX_M	4	O	Device Port 1. Transmit Data. Differential analog output.
P1_RX_P	1	I	Device Port 1. Receive Data. Differential analog input.
P1_RX_M	2	I	Device Port 1. Receive Data. Differential analog input.
Port 2 Signal Interface			

Table 3-2 Signal Interface Pins (continued)

Signal Name	Signal Number	Type	Description
P2_TX_P	11	O	Device Port 2. Transmit Data. Differential analog output.
P2_TX_M	10	O	Device Port 2. Transmit Data. Differential analog output.
P2_RX_P	7	I	Device Port 2. Receive Data. Differential analog input.
P2_RX_M	8	I	Device Port 2. Receive Data. Differential analog input.
Port 3 Signal Interface			
P3_TX_P	17	O	Device Port 3. Transmit Data. Differential analog output.
P3_TX_M	16	O	Device Port 3. Transmit Data. Differential analog output.
P3_RX_P	13	I	Device Port 3. Receive Data. Differential analog input.
P3_RX_M	14	I	Device Port 3. Receive Data. Differential analog input.
Host Port Signal Interface			
HT_TX_P	50	O	Host Port: Transmit Data. Differential analog output.
HT_TX_M	51	O	Host Port: Transmit Data. Differential analog output.
HT_RX_P	54	I	Host Port: Receive Data. Differential analog input.
HT_RX_M	53	I	Host Port: Receive Data. Differential analog input.

Table 3-3 Clock Global Signals

Signal Name	Signal Number	Type	Description
PWR_ON_RST_N	80	I-5-4 mA	Global Reset Pin. Active Low.
XTLIN/OSC	44	I	Crystal input, or reference clock input.
XTLOUT	45	O	The ceramic crystal is connected between the XTLIN and XTLOUT pins. XTLOUT should be floated if an external clock source is used.

Table 3-4 UART Two-Wire Serial Interface

Signal Name	Signal Number	Type	Description
UAO	19	O	Data output to UART.
UAI	20	I	Data input from UART.
SCL	39	I/O-5-4 mA	Serial Clock
SDA	40	I/O-5-4 mA	Serial Data

Table 3-5 Configuration Interface Signals

Signal Name	Signal Number	Type	Description
TESTMODE1	79	I-PD-5-4 mA	TESTMODE0 and TESTMODE1
TESTMODE0	78		Configuration mode pins.
HT_LED	21	I/O-PU-5-4 mA	HT LED. HT_LED: When host port is active, drives the LED to blink at a frequency of 20 Hz.
P0_LED	22	I/O-PD-5-4 mA	P0 LED P0_LED: When device port 0 is active, drives the LED to blink at a frequency of 20 Hz.
P1_LED	23	I/O-PD-5-4 mA	P1 LED. P1_LED: When device port 1 is active, drives the LED to blink at a frequency of 20 Hz.
P2_LED	24	I/O-PD-5-4 mA	P2 LED. P2_LED: When device port 2 is active, drives the LED to blink at a frequency of 20 Hz.
P3_LED	25	I/O-PD-5-4 mA	P3 LED. P3_LED: When device port 3 is active, drives the LED to blink at a frequency of 20 Hz.
P4_LED	27	I/O-PD-5-4 mA	P4 LED. P4_LED: When device port 4 is active, drives the LED to blink at a frequency of 20 Hz.

Table 3-6 Configuration and Test Pins

Signal Name	Signal Number	Type	Description
SYS_CFG0/AMP0	18	I/O-PU	System Configuration Pin 0. AMP0: Host port amplitude configuration test pin when defined in bootstrap. ***Note:*** *The setting is outlined in Appendix D.*

Table 3-6 Configuration and Test Pins (continued)

Signal Name	Signal Number	Type	Description
SYS_CFG1/AMP1	28	I/O-PD	System Configuration Pin 1. AMP1: Host port amplitude configuration test pin when defined in bootstrap
SYS_CFG2/AMP2	41	I/O-PU	System Configuration Pin 2. AMP2: Host port amplitude configuration test pin when defined in bootstrap
SYS_CFG3/AMP3	42	I/O-PD	System Configuration Pin 3. AMP3: Host port amplitude configuration test pin when defined in bootstrap.
SYS_CFG4/PRE0	63	I/O-PD	System Configuration Pin 4. PRE0: Host port pre-emphasis configuration test pin when defined in bootstrap
SYS_CFG5/PRE1	64	I/O-PU	System Configuration Pin 5. PRE1: Host port pre-emphasis configuration test pin when defined in bootstrap
SYS_CFG6/PRE2	65	I/O-PD	System Configuration Pin 6. PRE2: Host port pre-emphasis configuration test pin when defined in bootstrap.
SYS_CFG7/PRE_HALF_EN	66	I/O-PU	System Configuration Pin 7. PRE_HALF_EN: Host port pre-emphasis cut in half when defined in bootstrap.
SYS_CFG8/DRV_EN0	68	I/O-PU	System Configuration Pin 8. DRV_EN0: Host port Tx driver configuration pin 0 when defined in bootstrap.
SYS_CFG9/DRV_EN1	69	I/O-PU	System Configuration Pin 9. DRV_EN1: Host port Tx driver configuration pin 1 when defined in bootstrap
SYS_CFG10/DRV_EN2	70	I/O-PU	System Configuration Pin 10. DRV_EN2: Host port Tx driver configuration pin 2 when defined in bootstrap
SYS_CFG11/DRV_EN3	72	I/O-PD	System Configuration Pin 11. DRV_EN3: Host port Tx driver configuration pin 3 when defined in bootstrap
SYS_CFG12/DRV_EN4	73	I/O-PD	System Configuration Pin 12. DRV_EN4: Host port Tx driver configuration pin 4 when defined in bootstrap
SYS_CFG13/DRV_EN5	74	I/O-PD	System Configuration Pin 13. DRV_EN5: Host port Tx driver configuration pin 5 when defined in bootstrap.
SYS_CFG14/IBIASX2_EN	76	I/O-PD	System Configuration Pin 14. IBIASX2_EN: Enable host port Tx driver bias current to be cutin half when defined in bootstrap.

Table 3-6 Configuration and Test Pins (continued)

Signal Name	Signal Number	Type	Description
SYS_CFG15	77	I/O-PD	System Configuration Pin 15.
GPIO7	29	I/O-PD	GPIO 7.
GPIO6	31	I/O	GPIO 6
GPIO5	32	I/O	GPIO 5
GPIO4	33	I/O	GPIO 4
GPIO3	35	I/O	GPIO 3
GPIO2	36	I/O	GPIO 2
GPIO1	37	I/O	GPIO 1
GPIO0	38	I/O	GPIO 0
REFCLK_CFG1	62	I/O-PD	Reference Clock Configuration 1 and 0.
REFCLK_CFG0	61		Used to select reference clock frequency. **00:** 20 MHz. **01:** 25 MHz. **10:** 30 MHz. **11:** 40 MHz.

Table 3-7 Miscellaneous Pins

Signal Name	Signal Number	Type	Description
ISET	48	I	Bias Current Resistor. A 6.04 KΩ ± 1% resistor must be connected between this pin and a via in the digital ground plane.
TP	49	O	Analog Test Point.

Table 3-8 Power Pins

Signal Name	Signal Number	Type	Description
HT_VAA2	52	I	Host Port Phy Analog Power. Connect to 3.3V supply.
P0_VAA2	58	I	Device Port 0 Phy Analog Power. Connect to 3.3V supply.
P1_VAA2	3	I	Device Port 1 Phy analog power. Connect to 3.3V supply.
P2_VAA2	9	I	Device Port 2. Phy analog power. Connect to 3.3V supply.
P3_VAA2	15	I	Device Port 3: Phy analog power. Connect to 3.3V supply.

Table 3-8 Power Pins (continued)

Signal Name	Signal Number	Type	Description
VAA1	46	I	TBG Analog Power. Connect to 3.3V supply.
VSS1	43, 47	I	Analog Ground. Connect to analog ground plane.
P0_VSS2	55	I	Device Port 0 Phy analog ground. Connect to analog ground plane.
P1_VSS2	6	I	Device Port 1 Phy analog ground. Connect to analog ground plane.
P2_VSS2	12	I	Device Port 2 Phy analog ground. Connect to analog ground plane.
VDDIO	30,71 I		Digital Power. Connect to 3.3V supply.
VDD	26,34,67,75	I	Digital Power. Connect to 1.2V supply.

THIS PAGE LEFT INTENTIONALLY BLANK

4 MARVELL-SPECIFIC MODE

4.1 Marvell-Specific Mode

The Marvell-specific Queued Command mode uses a switching type between the FIS-based and command-based switching, also called queued command-based switching, which is not supported by the SATA II specification. This mode is supported by Marvell's 88SX6041 and 88SX6081 controllers.

Queued command-based switching enables host controllers which do not support hardware context switching to issue multiple outstanding NCQ commands. These commands can simultaneously be issued across multiple devices. In this method of switching, the 88SM4140 blocks frames according to the lock and release indicators mechanism to enforce operation of the data transaction associated with the same command. Frames from other ports are blocked while the current data transaction is in progress.

The 88SM4140 recognizes when a data transaction starts on a specific port, and locks the port until the data transaction has ended.

This switching type significantly increases the overall system performance while minimizing complexity in the port multiplier and the host controller.

The lock and release indicators used in the switching are described in Table 4-1:

Table 4-1 Native Command Queuing Lock and Release Indicators

Command Type	Lock FIS (Release previous lock)	Lock FIS Direction	Release FIS	Release FIS Direction
Read/Write FPDMA Queued	Reg H2D	Host to Device	Reg D2H BSY = 0 DRQ = 0	Device to Host
	DMA Setup	Device to Host	Set Device Bits SERV = 0	Device to Host
All others	Reg H2D	Host to Device		

THIS PAGE LEFT INTENTIONALLY BLANK

5 PCB LAYOUT GUIDELINES

This chapter on PCB layout guidelines is for customers designing schematics and printed circuit boards with the 88SM4140-based system, and is intended to aid in PCB design in order to ensure signal integrity.

This chapter is based on recommendations from Marvell Semiconductor design and application engineers familiar with the product, and is intended to aid in PCB design to ensure signal integrity. Whenever possible, the PCB designer should try to adhere to the following guidelines.

- Transmit/Receive Differential Pairs Interface
- DC Power and Ground
- Exposed Die Pad Package Design
- Layer Stack-Up/Signal Return Path
- Design Guidelines

5.1 Transmit/Receive Differential Pairs Interface

The only factor which should be kept in mind when doing the board stack up is that there should be a continuous ground plane beneath the SATA signals. Avoid any cuts in the reference plane below these signals, which cause reflections that increase jitter on these signals.

5.1.1 Differential Impedance

The Transmit (Tx) and Receive (Rx) differential pairs must have a trace geometry differential impedance of 100Ω ± 15%. This differential impedance can be achieved by using various trace geometries. The termination resistors are built into the chip, so no additional external resistors are required on the Tx and Rx pairs.

It is up to the vendors to determine which trace geometry best suits their needs. Use any commonly-available impedance calculator to calculate the stack-up and trace geometries.

Differential signals have very fast rise/fall times (on the order of picoseconds), so these interconnects should be treated as transmission lines rather than simple wire connections. A fundamental property of transmission lines is the characteristic impedance, Z0. The characteristic impedance is determined by the following:

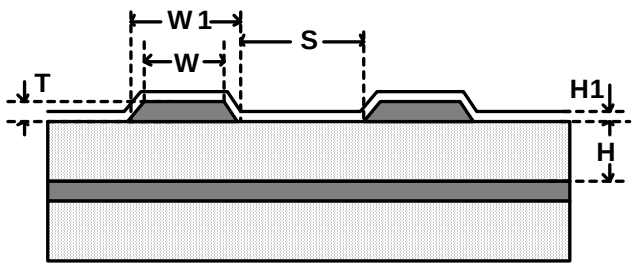
- Relative dielectric constant of the PC board material (Er).
- Thickness of the dielectric.
- Width of the transmission line.

When designing the board layout, first select the transmission line geometry:

- The over-under geometry provides strong coupling between traces, but is not recommended because it requires extra layers, and because the stack-up thickness causes variations in the differential impedance.
- The side-side geometry or the edge-side coupled geometry controls the differential impedance and avoids adjacent layer coupling by using solid ground planes.

5.1.2 Impedance

Figure 5-1 Edge-Coupled Coated Microstrip



The example shown in Figure 5-1 has the following dimensions:

Table 5-1 impedance Example Dimensions

Parameter	Dimension mil
H	20
H1	1
W	15
W1	16
S	9
T	1.4
Er	4.2

With the dimensions shown in Table 5-1, the calculated impedance (Z0) should be 99.09.

Note: Be sure to verify the impedance dimensions with the fab manufacturer.

5.1.3 Minimizing Skew

The trace lengths of the differential pairs (RX_P/RX_M and TX_P/TX_M) need to be same, or at least closely matched. Otherwise, skew performance can be affected. The skew requirement between the RX_P/RX_M or TX_P/TX_M pairs should be limited to less than 1% of the cycle time of 333.33 ps. This means that the skew should be less than 3.33 ps.

Typically, if FR-4 is used as the di-electric material, and the reflective index = 2.0, then by calculation, an electromagnetic wave takes 1 ps to travel 150 µm. The requirement for SATA 3.0 Gbps is 333.3 ps. Extending the calculation above, our skew requirement translates into a maximum difference of 495 µm between the RX_P/RX_M and TX_P/TX_M lines. However, 495 µm is the maximum. So it is preferable to maintain the difference in length to less than 250 µm.

5.1.4 Using Vias With TX/RX Differential Pairs

Vias and their clearance holes in power/ground planes can cause impedance discontinuities in nearby signals. To minimize impedance discontinuities in the power/ground planes, eliminate the usage of vias completely, and keep the differential pair traces on the same side and on the same layer of the PCB.

If vias cannot be eliminated, keep them away from the traces by at least 2.5 times the trace width. Minimize the number of vias as much as possible, because vias increase the capacitive effect. Giving more clearance for vias reduces the capacitive effect.

Each signal in a pair must have the same number of vias.

5.1.5 AC-Coupled SATA Signals

The SATA 1.5 Gbps specification calls for AC or DC coupling of SATA signals, while the SATA 3.0 Gbps specification only requires AC coupling. AC-coupled designs help in removing DC common-mode noise.

The Tx and Rx pairs have to go through a 10 nF, 10%, 0402 package, X7R/NPO type capacitor. Ideally, this capacitor should be very stable.

5.2 DC Power and Ground

5.2.1 VDD Power (1.2V) and GND

The VDD (1.2V) pins are the power source for the core and digital circuitry. All VDD pins must be connected directly to a power plane in the power layer with short and wide traces to minimize power trace inductances.

To connect to this plane, use vias close to VDD pins. Use capacitors with 0.1 µF for each group of VDD and GND with 2.2 µF for main VDD power.

For integrated circuits with ePAD on the package, ePAD should be connected to GND.

5.2.2 VDDIO Power (3.3V) and GND (or ePAD GND)

VDDIO (3.3V) is the power source for the digital I/O pins. VDDIO is the digital I/O supply and can be connected to 3.3V supply through a ferrite bead. Place a via immediately next to the VDDIO pins to connect down to the 3.3V power plane and resist using a long trace on the top layer. Use the following capacitors: 0.1 µF for each group of VDDIO and GND with 2.2 µF for main power.

For an ePAD package integrated circuit, ePAD is GND.

5.2.3 VAA Power (3.3V) and ePAD (VSS)

The VAA (analog power) pins should be separated from the digital power using a ferrite bead which behaves as a “wide band choke,” where the frequency is attenuated by 30 dB or more between 1-650 MHz. The noise levels on these analog power pins should be less than 100 mV. For each group of VAA/VSS pins, use capacitors with the values of 2.2 µF, 0.1 µF, 0.01 µF, and 1000 pF for each group of VAA and ePAD VSS pins.

Proper decoupling has to be provided for the VAA and VDD for normal operation. The decoupling capacitors for the analog power to the chip should be placed between the VAA and the ePAD VSS pins.

5.3 Exposed Die Pad Package Design

As the alternative to ground pins on the package, the exposed metal area on the bottom side of the package must be soldered to a pad with good connections to the ground plane(s) of the board. Using the LQFP exposed-die pad package, offers increased thermal efficiency shielding, and grounding benefits.

Figure 5-2 ePAD Package Chip Power and Ground Schematic

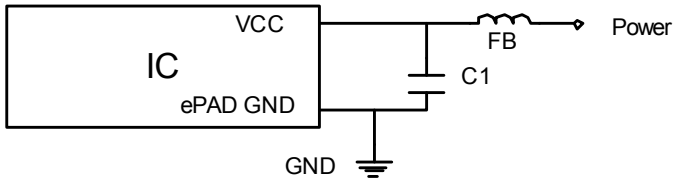


Figure 5-3 ePAD Package Chip on PCB Side View

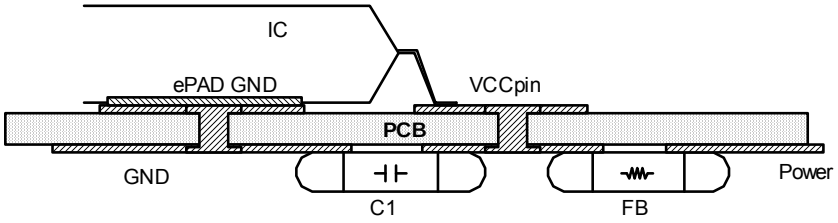


Figure 5-4 Chip Bottom View For ePad

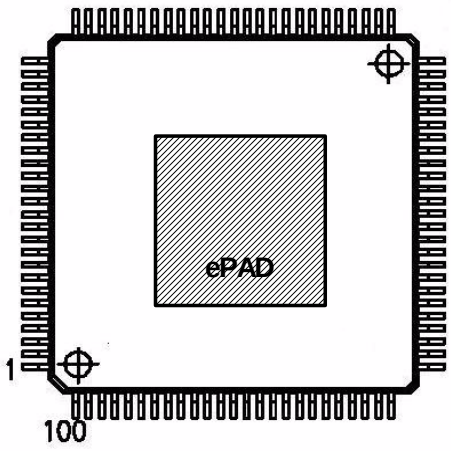
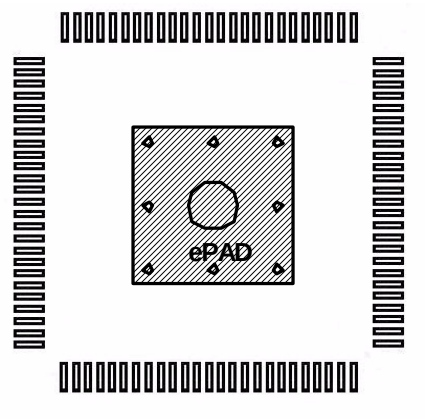


Figure 5-5 PCB Footprint for ePAD



PCB Footprint for ePAD

5.4 Layer Stack-Up/Signal Return Path

Many motherboards use a four layer stack-up, so we only discuss this scenario since adding layers only makes the job easier.

A typical 4-layer board is arranged as follows: signal–ground–power–signal.

With a four-layer PCB, use the following stack-up arrangement:

- Layer 1 – Topside, Parts, Slow and High Speed Signal Routes, and Power Routes.
- Layer 2 – Solid Ground Plane.
- Layer 3 – High Speed Signal Routes and Power Routes.
- Layer 4 – Bottom side, Slow Signal Routes, and Plane Routes.

Every signal requires a return path in order to complete the circuit. A return path should follow the signal route on an adjacent reference plane. If the return path is blocked from following its trace, then EMI and crosstalk problems can occur. While the top layer references a solid ground plane, the bottom layer might reference a cut-up power plane, which might not be very useful as a return path.

One solution to aid in return-path routing is to use return-path caps. Where a trace crosses a split in the plane, place a decoupling cap near that area and tie it to both sides of the split. In general, one cap is needed for every four adjacent traces. Another way to minimize plane splits is to put small power planes or patches on the surface layers.

5.5 Design Guidelines

For improved signal quality and longer practical transmission distances, use the following guidelines:

5.5.1 General

Use surface mount package resistors and capacitors with a smaller package parasitic value (for example, 0603 is better than 0805).

Use rounded corners rather than 90-degree or 45-degree corners.

5.5.2 Vias

Via and their clearance holes in power/ground planes can cause impedance discontinuities in nearby signals. To minimize impedance discontinuities, eliminate the usage of vias completely, and keep the differential pair traces on the same side and on the same layer of the PCB.

If vias cannot be eliminated, keep them away from the traces by at least 2.5 times the trace width. Minimize the number of vias as much as possible, as vias increase the capacitive effect. Giving more clearance for vias reduces the capacitive effect.

Each signal in a pair must have the same number of vias.

5.5.3 Traces

Keep the traces as short as possible. Initial component placement must be carefully considered. Eliminate or reduce stub lengths. Keep high speed traces at least ten times the trace width from any other signals which might cause capacitive couple noise in the signals.

Critical signals should avoid running parallel and close to or directly over a gap, as this would change the impedance of the trace. To avoid crosstalk, allow separation between fast signals. Crosstalk also increases as the parallel traces get longer.

When routing the traces for the decoupling capacitors, make the traces short and thick

5.5.4 Signal Routing

While routing the differential pairs, keep the trace length identical between the two traces. Differences in trace length directly translate into signal skew. In the case of differential signals, signals travel in opposite direction and thus noise cancellation happens due to coupled complementary fields. The field cancellation of differential signals reduces far field emissions. The only source of emissions from differential signals can come from differential skew, so controlling skew through routing is key to reducing EMI levels.

- When routing adjacent to only a power plane, do not cross splits. Route traces only over the power plane that supplies both the driver and the load. Otherwise, provide a decoupling capacitor near the trace at the end that is not supplied by the adjacent power plane.
- Do not route digital signals from other circuits across the area of the transmitter and receiver.
- Minimize the crosstalk between Tx pair and Rx pair signals. For dual strip-line routing, traces should only cross at 90 degree angles to each other. To minimize tandem crosstalk and to better control impedance, avoid more than two routing layers in a row.
- Calculate or model the impedance prior to routing in order to confirm that the proposed trace thickness is usable and that the desired board thickness is obtainable. For more accurate impedance data, consult with your board fabricator.

5.5.5 Planes

Follow these guidelines for designing planes:

- Do not split the ground planes. Keep space between possible sensitive analog circuitry on your board and the digital signals to sufficiently isolate noise. A solid ground plane is necessary to provide a good return path for routing layers. If possible, provide at least one ground plane adjacent to all routing layers.
- Separate analog powers onto opposing planes in order to minimize the coupling area that an analog plane has with an adjacent digital plane.
- To minimize warping, make sure that planes are evenly distributed.

5.5.6 Clock

The reference clock to the 88SM4140 should be highly stable. Place the clock close to the chip in order to minimize the ground noise between chip and clock source.

For best results, select an oscillator with high stability and low jitter. If a clock oscillator is used, then the reference peak-to-peak total jitter should be less than 150 ps. If a quartz crystal is used, then the crystal frequency tolerance and temperature stability should be less than 100 ppm.

A good, low jitter, stable oscillator and crystal provides cost and accuracy benefits for an entire system.

The guidelines for using quartz crystal are outlined in Appendix C.

5.5.7 Bias Current Resistor (ISET)

A 6.04 KΩ (1%) resistor should be connected between the ISET pin and the adjacent top ground plane. This resistor should lie as close as possible to the ISET pin.

5.5.8 Power-on-Reset Signal

RST_N is the active low reset pin and can be connected to a reset switch on the board or other active low reset source. The power-on reset signal needs to stay asserted till all supply voltages have reached full levels.

5.5.9 UART Interface

UAO and UAI are the UART interface pins. These pins are used to read and write to the 88SM4140 internal registers. If the UART interface is not used, then leave the UAO pin open and connect the UAI pin to a 3.3V (digital power input/output) pin using a 10 KΩ resistor.

5.5.10 Ground for SATA Connector

Use the digital ground (GND) to connect to the SATA connector. Do not use the analog ground.

THIS PAGE LEFT INTENTIONALLY BLANK

6 UART INTERFACE

The 88SM4140 supports two UART speeds to access the register. In normal mode, the speed is 57600 bps.

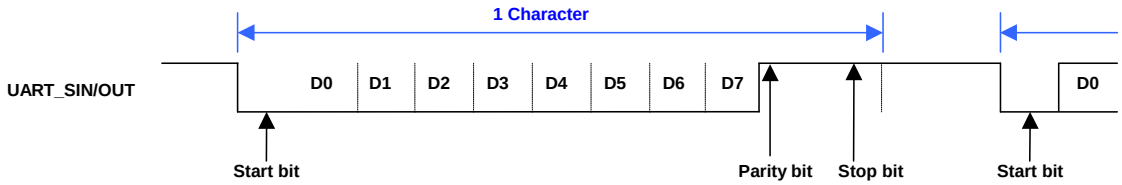
The UART interface is used to access internal registers, including those for each port's S-Status and Serial ATA debug registers.

The UART interface is not required for normal operation. At the fixed baud rate of 57600 bps, the UART interface block is used mostly for debugging purposes. If the UART pins are not used, all UAI pins must be left high for normal operation.

- UART Interface Timing Example
- Register Access Sequence through UART

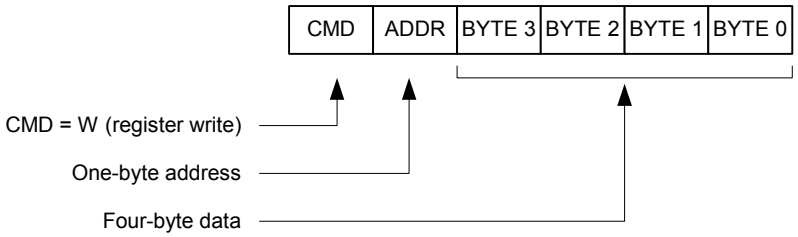
6.1 UART Interface Timing Example

Figure 6-1 UART Signal Timing Example



6.2 Register Access Sequence through UART

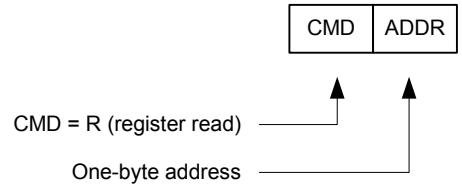
Figure 6-2 Write Command Format



A carriage return (CR) character and a line feed (LF) character are required after a WRITE command for command execution. A zero, a carriage return, and a line feed are returned if the command executes correctly. A question mark (”?”), a carriage return, and a line feed are returned if an error is encountered. All alphabetic characters should be in upper case. The backspace character is not recognized.

For example: W12AD34DF23 + CR + LF means write the value of AS34DF23h to the location R12h. If the UART returns 0 + CR + LF, then the command executed properly. If the UART returns ? + CR + LF, then the command did not execute properly.

Figure 6-3 Read Command Format



The carriage return and line feed characters are required after a READ command. The register value, carriage return, and line feed characters are returned if the command executes correctly. A question mark (“?”), carriage return, and line feed characters are returned if an error is encountered. All alphabetic characters should be in upper case. The backspace character is not recognized.

For example: R12h + CR + LF means read from R12h. If the Register value + CR + LF is returned, then the read command executed properly. If ? + CR + LF is returned from the UART, then the command did not execute properly.

6.2.1 UART Read/Write Command Sequences

Each UART sequence includes the parity bit in the last bit. The following tables detail the register Read/Write sequences for Read and Write commands, with and without errors.

Table 6-1 Read Command, No Error

Byte	Master	Slave	Value
1	CMD(R)		52h
2	ADDR		ASCII (ADDR [7:4])
3			ASCII (ADDR [3:0])
4	CR		0Dh
5	LF		0Ah
6		BYTE3	ASCII (BYTE3 [7:4])
7			ASCII (BYTE3[3:0])
8		BYTE2	ASCII (BYTE2 [7:4])
9			ASCII (BYTE2[3:0])
10		BYTE1	ASCII (BYTE1 [7:4])
11			ASCII (BYTE1[3:0])
12		BYTE0	ASCII (BYTE0 [7:4])
13			ASCII (BYTE0[3:0])
15		CR	0Dh
16		LF	0Ah

Table 6-2 Read Command, Error

Byte	Master	Slave	Value
1	CMD(R)		52h
2	ADDR		ASCII (ADDR [7:4])
3			ASCII (ADDR [3:0])
4	CR		0Dh
5	LF		0Ah
6		?	3Fh
7		CR	0Dh
8		LF	0Ah

Table 6-3 Write Command, No Error

Byte	Master	Slave	Value
1	CMD(W)		57h
2	ADDR		ASCII (ADDR [7:4])
3			ASCII (ADDR [3:0])
4	BYTE3		ASCII (BYTE3 [7:4])
5			ASCII (BYTE3[3:0])
6	BYTE2		ASCII (BYTE2 [7:4])
7			ASCII (BYTE2[3:0])
8	BYTE1		ASCII (BYTE1 [7:4])
9			ASCII (BYTE1[3:0])
10	BYTE0		ASCII (BYTE0 [7:4])
11			ASCII (BYTE0[3:0])
12	CR		0Dh
13	LF		0Ah
14		0	30h
15		CR	0Dh
16		LF	0Ah

Table 6-4 Write Command, Error

Byte	Master	Slave	Value
1	CMD(W)		57h
2	ADDR		ASCII (ADDR [7:4])
3			ASCII (ADDR [3:0])
4	BYTE3		ASCII (BYTE3 [7:4])
5			ASCII (BYTE3[3:0])
6	BYTE2		ASCII (BYTE2 [7:4])
7			ASCII (BYTE2[3:0])
8	BYTE1		ASCII (BYTE1 [7:4])
9			ASCII (BYTE1[3:0])
10	BYTE0		ASCII (BYTE0 [7:4])
11			ASCII (BYTE0[3:0])
12	CR		0Dh
13	LF		0Ah
14		?	3Fh
15		CR	0Dh
16		LF	0Ah

THIS PAGE LEFT INTENTIONALLY BLANK

7 PORTS

This chapter contains the following information about ports in the 88SM4140:

7.1 PM_PORT Field

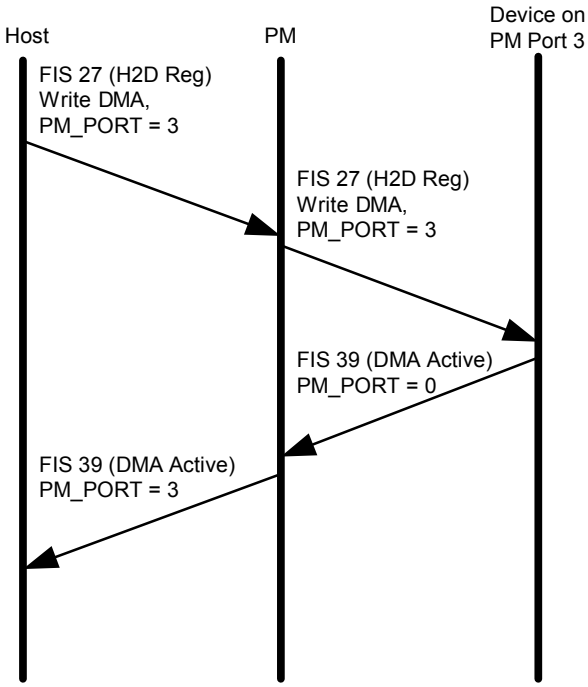
For the port multiplier to function, the host must be able to select each SATA device that is connected to the 88SM4140. To do this, a new field has been added to all SATA FISes (refer to Table 7-1). Before the introduction of the port multiplier, these bits had previously been defined as reserved bits. If the host is port multiplier-enabled, then after the port multiplier's detection and initialization process, the host is able to access each device by changing the value of the PM_PORT field.

Table 7-1 First DWord of All FIS Types

Byte Position	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
DWord 0	(As defined in Serial ATA 1.0a Specification)																				PM_PORT				FIS Type							
Value	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	1	0	1	1	1	0

Figure 7-1 shows an example of communication between a PM-aware host and the port multiplier (PM).

Figure 7-1 Traffic Between a PM-Aware Host and the PM



7.2 Control Ports

Each port multiplier (PM) has a control port which provides some device information to the host, such as the connection status (S-Status), SATA Error (S-Error) and the supported port numbers. In addition, the control port also provides the host with some form of control over the devices. For example, the host can tell the PM to disconnect a port or to engage in SATA BIST activity.

To the host, the control port functions exactly the same as a series of registers. PM registers are categorized into two types:

- General Status and Control Registers (GSCR)
- Port Status and Control Registers (PSCR).

In each port multiplier, there is only one set of GSCR and one set of PSCR for each port.

For more information on the GSCR andPSCR registers, refer to Chapter 9, Registers or the *Serial ATA II: Port Multiplier* specification.

The host can access the PM's control port as port Fh by using the READ BUFFER (E4h) and WRITE BUFFER (E8h) ATA commands. Refer to A.4.9, "How Does the Host Access the PM Registers?" for detail on how these ATA commands can be used with the PM.

7.3 Sample Sequence

The following sections illustrate a typical example of a sequence that occurs between a PM-aware host and the PM.

Note: In the phases below, some of the steps describe accessing the PM registers. Refer to A.4.9, “How Does the Host Access the PM Registers?” for information on how to access the PM registers.

7.3.1 PM Discovery Phase

1. Host selects the control port (Fh) for the operation.
2. Host performs a software reset.
3. Host receives signature. If the signature = 0966901h, then the PM is present.
4. Host checks the number of device ports available on PM. Note that this is not to check the number of drives connected but the number of ports. This can be done using the ATA READ BUFFER command and the information is available in the control port's Port Information (R0002h) register. A typical read command looks like this:

```
# WTASK <Ch> <FE> <SC> <SN> <CL> <CH> <DH> <CMD>

WTASK 0 02 00 00 00 00 0F E4

POLL_ALT 0 50 100

# CTASK <Ch> <ERR> <SC> <SN> <CL> <CH> <DH> <STS>

CTASK 0  00 04 00 00 00 00 50

# Expects 00000004
```

7.3.2 Device Discovery (Device Enumeration) Phase

Now that host has detected the PM and the number of possible devices the PM can be connected to, the host checks if a device is connected to each of the PM's ports. A sample sequence for port 2 is listed in the following section.

1. The host enables the device port by setting the DET field appropriately in the device port's Serial ATA Port (S-Control) register, as specified in section 10.1.3 of the *Serial ATA: High Speed Serialized AT Attachment* specification. The host uses the WRITE PORT MULTIPLIER command to write to the Serial ATA Port (S-Control) register, which enables the device port.

```
# Write Port 2 PSCR02 = 00000001->00000000

# WTASK <Ch> <FE> <SC> <SN> <CL> <CH> <DH> <CMD>

WTASK 0 02 01 00 00 00 02 E8

# WTASK <Ch> <FE> <SC> <SN> <CL> <CH> <DH> <CMD>

WTASK 0 02 00 00 00 00 02 E8
```

2. After enabling a device port, the host should allow for communication to be established and device presence to be detected. Refer to section 6.8.1 of the Serial ATA: High Speed Serialized AT Attachment specification for a description of the host Phy initialization sequence.
3. The host reads the Serial ATA Port S-Status register for the device port using the READ PORT MULTIPLIER command.

   If the (S-Status) register indicates that a device is present, the host queries the Serial ATA Port S-Error register for the device port and clears the X bit to indicate that the device presence has changed.

Note: The X bit must be cleared, otherwise communications between the host and the corresponding device port are not allowed. All FISes from the host are terminated by a SYNC and FIS from the device. The device does not respond with an R_RDY primitive.

```
# Check Port 2 PSCR00 = 00000113
# WTASK <Ch> <FE> <SC> <SN> <CL> <CH> <DH> <CMD>
WTASK 0 00 00 00 00 00 02 E4
# CTASK <Ch> <ERR> <SC> <SN> <CL> <CH> <DH> <STS>
POLL_ALT 0 50 100
CTASK 0 00 13 01 00 00 00 50
# Expects 00000113 (or 00000123)
# Check PSCR 1.x
# WTASK <Ch> <FE> <SC> <SN> <CL> <CH> <DH> <CMD>
WTASK 0 01 00 00 00 00 02 E4
POLL_ALT 0 50 100
RTASK 0
IDLE 100
# Clear PSCR1.x
# WTASK <Ch> <FE> <SC> <SN> <CL> <CH> <DH> <CMD>
WTASK 0 01 FF FF FF FF 02 E8
IDLE 100
POLL_ALT 0 50 100
# Check X-bit cleared
# WTASK <Ch> <FE> <SC> <SN> <CL> <CH> <DH> <CMD>
WTASK 0 01 00 00 00 00 02 E4
POLL_ALT 0 50 100
RTASK 0
```

4. The signature generated by the device from the initial COMRESET to the device port can be discarded if the host does not support context switching, because the BSY bit may be clear when the Register FIS is received by the host. Therefore, to determine the signature of the attached device, the host should issue a software reset to the device port. If a valid signature is returned for a recognized device, the host can then proceed with normal initialization for that device type.

```
# host selects Port 2 for following operation
WB 0 40 68
WD 0 44 00000002
IDLE 1000
# Host issues soft reset
SRST 0
idle 2000
POLL_ALT 0 50 100
# Read signature
# CTASK <Ch> <ERR> <SC> <SN> <CL> <CH> <DH> <STS>
POLL_ALT 0 50 100
CTASK 0 01 01 01 00 00 00 50
# This is HDD signature
```

When the host sends a COMRESET OOB to the PM, the PM propagates the COMRESET OOB onto all of its device ports. As a result, any enumeration process done previously needs to be performed again in order for the host to resume communication with the attached drives.

7.3.3 SATA Enclosure Management Bridge (SEMB)

It is common to find a SATA Enclosure Management Bridge (SEMB) as part of a PM. This feature gives the host the ability to check parameters such as temperature, control fan speed and LEDs using the same SATA connection that is used for data transfer. The 88SM4140 also supports the Storage Enclosure Management Bridge, which uses PM port 4 as its device port.

For more information, refer to “A.4.10, “What is SEMB?”

7.3.4 Cascading the PM

The PM, by definition, should not be cascaded In other words, do not connect a PM to another PM.

THIS PAGE LEFT INTENTIONALLY BLANK

February 1, 2007
Doc No. MV-S101553-00 Rev. G

8 ELECTRICAL SPECIFICATIONS

This chapter contains the following electrical specification information:

- Power Requirements
- Absolute Maximum Ratings
- Recommended/Typical Operating Conditions
- DC Characteristics

8.1 Power Requirements

The following table describes the 88SM4140 power requirements.

Table 8-1 Total Power Dissipation

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Absolute digital I/O pad power supply	I_{VDDIO}				20	mA
Absolute digital power supply	I_{VDD}				100	mA
Absolute analog power supply for TBG	I_{VAA1}				10	mA
Absolute analog power supply for Phy	I_{VAA2}				440	mA

8.2 Absolute Maximum Ratings

Table 8-2 Absolute Maximum Ratings

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Absolute Digital Power Supply Voltage	VDD_{abs}		-0.5		1.29	V
Absolute Digital I/O pad Supply Voltage	$VDDIO_{abs}$		-0.5		3.8	V
Absolute Analog Power Supply Voltage for TBG	$VAA1_{abs}$		-0.5		3.6	V
Absolute Analog Power Supply Voltage for Phy	$VAA2_{abs}$		-0.5		3.6	V
Absolute Input Voltage	Vin_{abs}		-0.4		VDDIO + 0.4	V
Absolute Storage Temperature	$Tstor_{abs}$		-55		+85	°C
Absolute Junction Temperature	$Tjunc_{abs}$				125	°C

8.3 Recommended/Typical Operating Conditions

Table 8-3 Recommended/Typical Operating Conditions

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Ambient Operating Temperature			0		70	°C
Junction Operating Temperature			0		125	°C
Operating Digital Power Supply Voltage	VDD_{OP}		1.2 - 8%	1.2	1.2 + 8%	V
Operating Digital I/O Pad Supply Voltage	$VDDIO_{OP}$		3.3 - 8%	3.3	3.3 + 8%	V
Operating Analog Power Supply Voltage for TBG	$VAA1_{OP}$		3.3 - 8%	3.3	3.3 + 8%	V
Operating Analog Power Supply Voltage for Phy	$VAA2_{OP}$		3.3 - 8%	3.3 3	.3 + 8%	V

8.4 DC Characteristics

Table 8-4 DC Characteristics

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Input Low Voltage	V_{IL}		-0.4		0.8	V
Input High Voltage	V_{IH}		2.0		VDDIO + 0.4	V
Output Low Voltage	V_{OL}	I_{OL}=4 mA, VDDP=3.3V	-0.4	0.13	0.4	V
Output High Voltage	V_{OH}	I_{OL}=-2 mA, VDDP=3.3V	2.4	3.3		V

THIS PAGE LEFT INTENTIONALLY BLANK

9 REGISTERS

Table 9-1 Configuration Information Registers

Register	Default Value	Register Description	Location
R0000h 41	4011ABh	Product Identifier	Page 9-6
R0001h 00	00C10Eh	Revision Information	Page 9-6
R0002h 00	000004h	Port Information	Page 9-7

Table 9-2 Status Information and Control Registers

Register	Default Value	Register Description	Location
R0020h 00	000000h	Error Status	Page 9-7
R0021h 04	00FFFFh	Error Mask	Page 9-7
R0022h	00000000h	Phy Event Counter Control	Page 9-8

Table 9-3 Features Supported Registers

Register	Default Value	Register Description	Location
R0040h 00	00001Fh	Port Multiplier v1.x Optional Features Support	Page 9-9
R0060h 00	000005h	Port Multiplier v1.x Optional Features Enable	Page 9-9

Table 9-4 Vendor Unique Registers

Register	Default Value	Register Description	Location
R0091h 24	9192AFh	Phy Mode 2	Page 9-10
R0092h D2	AA8000h	Phy Mode 3	Page 9-11
R0093h 04	090005h	Phy Mode 4	Page 9-11
R0096h	00002C2Bh	Two-Wire Serial Control	Page 9-12
R009Ah 00	000000h	GPIO Control	Page 9-13
R009Dh 00	780647h	Phy Mode 7	Page 9-13

Table 9-5 Phy Event Counter Registers

Register	Default Value	Register Description	Location
R0100h	00000000h	Host Port Phy Event Counter 1	Page 9-14
R0101h	00000000h	Reserved for Phy Event Counter	Page 9-14
⋮	⋮	⋮	⋮
R08FFh	00000000h	Reserved for Phy Event Counter	Page 9-14
R0900h	00000000h	Reserved for General Status and Control	Page 9-15
⋮	⋮	⋮	⋮
RFFFFh	00000000h	Reserved for General Status and Control	Page 9-15

Table 9-6 Port Status and Control Registers

Register	Default Value	Register Description	Location
R0000h 00	000000h	S-Status	Page 9-16
R0001h 00	000000h	S-Error	Page 9-16
R0002h 00	000004h	S-Control/SM-Control	Page 9-18
R0100h	00000000h	Device Port Phy Event Counter 0	Page 9-20
R0101h	00000000h	Device Port Phy Event Counter 2	Page 9-20
R0102h	00000000h	Reserved for Phy Event Counter	Page 9-21
⋮	⋮	⋮	⋮
R08FFh	00000000h	Reserved for Phy Event Counter	Page 9-21

Table 9-7 Register Map

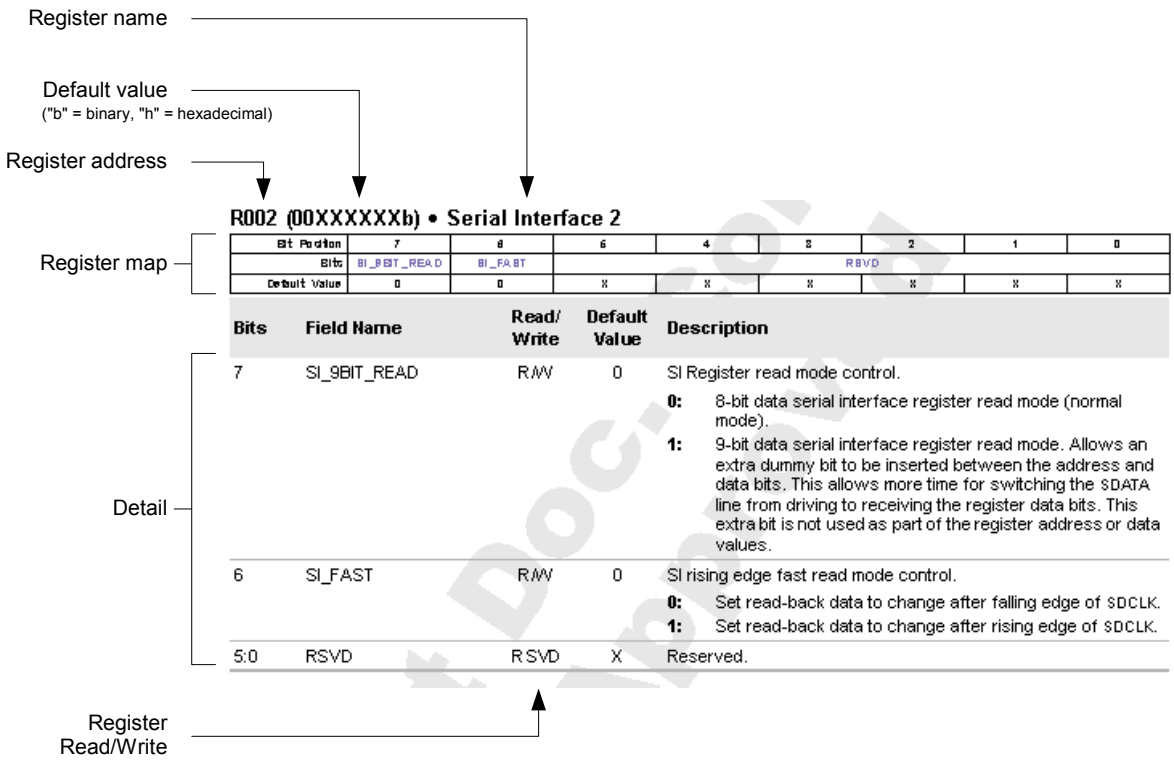
Address	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R0000h	DEV_ID																VED_ID															
R0001h	RSVD																REV_ID								RSVD						SPT_PM_12	SPT_PM_11	SPT_PM_10	RSVD
R0002h	RSVD																														PORT_NUM			
R0020h	RSVD																														PERR_STS			
R0021h	ERR_MASK																																	
R0022h	H_PORT_GLBL_CNT_RST	RSVD											P3_CNT_RST	P2_CNT_RST	P1_CNT_RST	P0_CNT_RST	RSVD																	PHY_EVNT_CNT_EN
R0040h	RSVD																											SPT_PHY_CNT	SPT_NOTIFY	SPT_SSC	SPT_PMREQ	SPT_BIST	
R0060h	RSVD																												NOTIFY_EN	SSC_EN	PMARQ_EN	BIST_EN	
R0091h	RSVD																								TXAMP			TXPRE		RSVD			
R0092h	RSVD																SSC_EN	RSVD															
R0093h	BYPASS_OOB	RSVD																															
R0096h	RSVD				TSC_SM_WR	TSC_SM_ADDR			TSC_SM_RD_DATA / TSC_SM_WR_DATA								RSVD	TSC_SEP_ADDR							RSVD	TSC_SEMB_ADDR							
R009Ah	RSVD												GPIO_IN				RSVD	GPIO_OUT							RSVD	GPIO_OUT_EN							
R009Dh	RSVD																PRE_HALF_EN	IBIAS X2_EN	RSVD						DRV_EN							
R0100h	PHY_EVT_C01																															
R0101h	RSVD																															
⋮	⋮																⋮															
R08FFh	RSVD																															
R0900h	RSVD																															
⋮	⋮																⋮															
RFFFFh	RSVD																															
R0000h	RSVD																				P_IPM_STS				P_SPD_STS				P_DET_STS			
R0001h	RSVD				P_DIAG_X	RSVD			P_DIAG_S	P_DIAG_H	P_DIAG_C	P_DIAG_D	P_DIAG_B	P_DIAG_W	RSVD	P_DIAG_N	RSVD															P_ERR_C	RSVD
R0002hR0002h	RSVD																				P_IPM_CTL				P_SPD_CNTL				P_SPD_CNTL			
	RSVD																														SM_DET_CTL			
R0100h	PHY_EVT_C00																															
R0101h	PHY_EVT_C02																															
R0102h	RSVD																															

Table 9-7 Register Map (continued)

Address	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
⋮																⋮																
R08FFh	RSVD																															

9.1 Notational Conventions

The following illustration shows how to read the register tables in this section.



R002 (00XXXXXXb) • Serial Interface 2

Bit Position	7	6	5	4	3	2	1	0
Bits	SI_9BIT_READ	SI_FAST	RSVD					
Default Value	0	0	X	X	X	X	X	X

Bits	Field Name	Read/ Write	Default Value	Description
7	SI_9BIT_READ	R/W	0	SI Register read mode control. **0:** 8-bit data serial interface register read mode (normal mode). **1:** 9-bit data serial interface register read mode. Allows an extra dummy bit to be inserted between the address and data bits. This allows more time for switching the SDATA line from driving to receiving the register data bits. This extra bit is not used as part of the register address or data values.
6	SI_FAST	R/W	0	SI rising edge fast read mode control. **0:** Set read-back data to change after falling edge of SDCLK. **1:** Set read-back data to change after rising edge of SDCLK.
5:0	RSVD	RSVD	X	Reserved.

9.2 Register Descriptions

Note: All registers not listed are reserved.

9.2.1 Configuration Information Registers

R0000h (414011ABh) • Product Identifier

Bit Position	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bits	DEV_ID																VED_ID															
Default Value	0	1	0	0	0	0	0	1	0	1	0	0	0	0	0	0	0	0	0	1	0	0	0	1	1	0	1	0	1	0	1	1

Bits	Name	Mode	Default Value	Description
31:16	DEV_ID	R	4140h	Device ID. The device ID allocated by the vendor.
15:0	VED_ID	R	11ABh	Vendor ID. The vendor ID allocated by the PCI-SIG.

R0001h (0000C10Eh) • Revision Information

Bit Position	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bits	RSVD																REV_ID								RSVD				SPT_PM_12	SPT_PM_11	SPT_PM_10	RSVD
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	1	0	0	0	0	1	1	1	0

Bits	Name	Mode	Default Value	Description
31:16	RSVD	R	0000h	Reserved.
15:8	REV_ID	R	C1h	Revision ID. Revision number of the 88SM4140.
7:4	RSVD	R	00h	Reserved.
3	SPT_PM_12	R	1h	Port Multiplier 1.2 Support. **0:** Does not support Port Multiplier Specification v1.2. **1:** Supports Port Multiplier Specification v1.2.
2	SPT_PM_11	R	1h	Port Multiplier 1.1 Support. **0:** Does not support Port Multiplier Specification v1.1. **1:** Supports Port Multiplier Specification v1.1.
1	SPT_PM_10	R	1h	Port Multiplier 1.0 Support. **0:** Does not support Port Multiplier Specification v1.0. **1:** Supports Port Multiplier Specification v1.0.
0	RSVD	R	0h	Reserved.

R0002h (00000004h) • Port Information

Bit Position	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bits	RSVD																												PORT_NUM			
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0

Bits	Name	Mode	Default Value	Description
31:4	RSVD	R	0000h	Reserved.
3:0	PORT_NUM	R	5h	Number of Ports. Indicates the number of exposed device fan-out ports. If Two-Wire Serial mode is enabled, then the value of this bit is 5h, to denote the existence of an Storage Evaluation Process (SEP) and four device ports. If Two-Wire Serial mode is disabled, the value of this bit is 4h, to denote just the four device ports..

9.2.2 Status Information and Control Registers

R0020h (00000000h) • Error Status

Bit Position	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bits	RSVD																												PERR_STS			
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Mode	Default Value	Description
31:4	RSVD	R	0000h	Reserved.
3:0	PERR_STS	R	0h	Error Status. GIves the error status for the OR bits in each port's Serial ATA S-Error Register.

R0021h (0400FFFFh) • Error Mask

Bit Position	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bits	ERR_MASK																															
Default Value	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bits	Name	Mode	Default Value	Description
31:0	ERR_MASK	R/W	0400FFFFh	Error Mask.

R0022h (00000000h) • Phy Event Counter Control

Bit Position	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bits	H_PORT_GLBL_CNT_RST	RSVD											P3_CNT_RST	P2_CNT_RST	P1_CNT_RST	P0_CNT_RST	RSVD															PHY_EVNT_CNT_EN
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Mode	Default Value	Description
31	H_PORT_GLBL_CNT_RST	R/W	0h	Host Port Global Counter Reset. If set to 1, results in an immediate reset of all Phy event counters associated with the host port. Once the reset is complete, the bit is cleared to zero automatically. If written to 0, no action is taken.
30:20	RSVD	R	00h	Reserved.
19	P3_CNT_RST	R/W	0h	Port 3 Counter Reset. If set to 1, results in an immediate reset of all Phy event counters associated with the device port. Once the reset is complete, the bit is cleared to zero automatically. If written to 0, no action is taken.
18	P2_CNT_RST	R/W	0h	Port 2 Counter Reset. If set to 1, results in an immediate reset of all Phy event counters associated with the device port. Once the reset is complete, the bit is cleared to zero automatically. If written to 0, no action is taken.
17	P1_CNT_RST	R/W	0h	Port 1Counter Reset. If set to 1, results in an immediate reset of all Phy event counters associated with the device port. Once the reset is complete, the bit is cleared to zero automatically. If written to 0, no action is taken.
16	P0_CNT_RST	R/W	0h	Port 0 Counter Reset. If set to 1, results in an immediate reset of all Phy event counters associated with the device port. Once the reset is complete, the bit is cleared to zero automatically. If written to 0, no action is taken.
15:1	RSVD	R	00h	Reserved.
0	PHY_EVNT_CNT_EN	R/W	0h	Phy Event Counters Enable. **0:** All event counters stop counting and retain their current value. **1:** Enable all Phy event counters.

9.2.3 Features Supported Registers

R0040h (0000001Fh) • Port Multiplier v1.x Optional Features Support

Bit Position	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bits	RSVD																											SPT_PHY_CNT	SPT_NOTIFY	SPT_SSC	SPT_PMREQ	SPT_BIST
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1

Bits	Name	Mode	Default Value	Description
31:5	RSVD	R	0000000h	Reserved.
4	SPT_PHY_CNT	R	1h	Support Phy Event Counters. **0:** Does not support Phy event counters. **1:** Supports Phy event counters.
3	SPT_NOTIFY	R	1h	Notify Support. **0:** Does not support asynchronous Set Device Bit (SDB) notification. **1:** Supports asynchronous SDB notification.
2	SPT_SSC	R	1h	SSC Support. **0:** Does not support dynamic Spread Spectrum Clock (SSC) transmit. **1:** Supports dynamic SSC transmit.
1	SPT_PMREQ	R	1h	PMREQ Support. **0:** Does not support issuing a $PMREQ_P$ to the host. **1:** Supports issuing a $PMREQ_P$ to the host.
0	SPT_BIST	R	1h	BIST Support. **0:** Does not support BIST. **1:** Supports BIST.

R0060h (00000005h) • Port Multiplier v1.x Optional Features Enable

Bit Position	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bits	RSVD																												NOTIFY_EN	SSC_EN	PMARQ_EN	BIST_EN
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1

Bits	Name	Mode	Default Value	Description
31:4	RSVD	R	0000000h	Reserved.
3	NOTIFY_EN	R/W	0h	Asynchronous Set Device Bit Notification Enable. **0:** Asynchronous Set Device Bit (SDB) notification is disabled. **1:** Asynchronous SDB notification is enabled.

Bits	Name	Mode	Default Value	Description
2	SSC_EN	R/W	1h	SSC Enable. **0:** Dynamic SSC transmit is disabled. **1:** Dynamic SSC transmit is enabled.
1	PMARQ_EN	R/W	0h	PMREQ Enable. **0:** Issuing of $PMREQ_P$ to the host is disabled. **1:** Issuing of $PMREQ_P$ to the host is enabled.
0	BIST_EN	R/W	1h	BIST Disable. **0:** BIST support is disabled. **1:** BIST support is enabled.

9.2.4 Vendor Unique Registers

R0091h (249192AFh) • Phy Mode 2

Bit Position	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bits	RSVD																					TXAMP				TXPRE			RSVD			
Default Value	0	0	1	0	0	1	0	0	1	0	0	1	0	0	0	1	1	0	0	1	0	0	1	0	1	0	1	0	1	1	1	1

Bits	Name	Mode	Default Value	Description
31:11	RSVD	R/W	049232h	Reserved. Do not change default value.
10:7	TXAMP	R/W	5h	TX Amplitude. Sets the Tx Driver output amplitude. The final output amplitude is defined by IBIASX2_EN (R009Dh [8]), DRV_EN (R009Dh [5:0]) and TXAMP (R0091h [10:7]). See Table D-1 for more detail.
6:4	TXPRE	R/W	2h	TX Pre-Emphasis Setting. Sets the pre-emphasis voltage level. Formula: (1-a * Z ^ -1), a = 0% ~ 35% (5% increments) See Table D-2 for more detail
3:0	RSVD	R/W	Fh	Reserved. Do not change default value.

R0092h (D2AA8000h) • Phy Mode 3

Bit Position	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bits	RSVD											SSC_EN	RSVD																			
Default Value	1	1	0	1	0	0	1	0	1	0	1	0	1	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Mode	Default Value	Description
31:21	RSVD	R/W	695h	Reserved. Do not change default value.
20	SSC_EN	R/W	0h	SSC Enable. **0:** SSC is disabled. **1:** SSC is enabled. Reading this field returns the current SSC_EN value, and writing a 1 to this field toggles the SSC_EN value.
19:0	RSVD	R/W	A8000h	Reserved. Do not change default value.

R0093h (04090005h) • Phy Mode 4

Bit Position	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bits	BYPASS_OOB	RSVD																														
Default Value	0	0	0	0	0	1	0	0	0	0	0	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1

Bits	Name	Mode	Default Value	Description
31	BYPASS_OOB	R/W	0h	OOB Bypass. When set to 1, the Phy enters PHYREADY state.
30:0	RSVD	R/W	4090005h	Reserved. Do not change default value.

R0096h (00002C2Bh) • Two-Wire Serial Control

Bit Position	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bits	RSVD				TSC_SM_WR	TSC_SM_ADDR			TSC_SM_RD_DATA / TSC_SM_WR_DATA								RSVD	TSC_SEP_ADDR							RSVD	TSC_SEMB_ADDR						
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	1	0	0	0	0	1	0	1	0	1	1

Bits	Name	Mode	Default Value	Description
31:28	RSVD	R	0h	Reserved.
27	TSC_SM_WR	R/W	0h	TSC_SM_WR. The TSC_SM_WR, TSC_SM_ADDR, and SM_RD_DATA/SM_WR_DATA signals provide an interface for software to program the Two-Wire Serial register, so that the software can control the interface of Two-Wire Serial. Refer to the Two-Wire Serial IP Specification for more detail.
26:24	TSC_SM_ADDR	R/W	0h	TSC_SM_ADDR. Refer to the Two-Wire Serial IP Specification for more detail.
23:16	TSC_SM_RD_DATA / TSC_SM_WR_DATA	R/W	00h	TSC_SM Read/Write Data. Refer to the Two-Wire Serial IP Specification for more detail.
15	RSVD	R	0h	Reserved.
14:8	TSC_SEP_ADDR	R/W	2Ch	SEP Two-Wire Serial Address.
7	RSVD	R	0h	Reserved.
6:0	TSC_SEMB_ADDR	R/W	2Bh	SEMB Two-Wire Serial Address.

R009Ah (00000000h) • GPIO Control

Bit Position	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bits	RSVD									GPIO_IN							RSVD	GPIO_OUT							RSVD	GPIO_OUT_EN						
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Mode	Default Value	Description
31:23	RSVD	R	00h	Reserved.
22:16	GPIO_IN	R	00h	GPIO Input. Returns the value of the GPIO[6:0] pins.
15	RSVD	R	0h	Reserved.
14:8	GPIO_OUT	R/W	00h	GPIO Output. If GPIO_OUT_EN is enabled, then the output of GPIO[6:0] is stored in this register.
7	RSVD	R	0h	Reserved.
6:0	GPIO_OUT_EN	R/W	00h	GPIO Output Enable. **0:** Disable GPIO output. **1:** Enable GPIO output. ***Note:*** *Each bit of GPIO_OUT_EN (R009Ah [6:0]) independently enables or disables a different GPIO output.*

R009Dh (00780647h) • Phy Mode 7

Bit Position	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bits	RSVD																						PRE_HALF_EN	IBIASX2_EN	RSVD		DRV_EN					
Default Value	0	0	0	0	0	0	0	0	0	1	1	1	1	0	0	0	0	0	0	0	0	1	1	0	0	1	0	0	0	1	1	1

Bits	Name	Mode	Default Value	Description
31:10	RSVD	R/W	001D01h	Reserved. Do not change default value.
9	PRE_HALF_EN	R/W	1h	Tx Pre-emphasis Halve Enable. When enabled, Tx pre-emphasis is cut in half. ***Note:*** *When using half of the small drivers in order to get small amplitude, this bit has to be enabled.*
8	IBIASX2_EN	R/W	0h	Tx Driver Bias Current Halve. When enabled, Tx driver biasing current is cut in half.
7:6	RSVD	R/W	1h	Reserved. Do not change default value.
5:0	DRV_EN	R/W	07h	Tx Driver Enable. The Tx driver consists of six small drivers. This field can enable or disable these small drivers independently.

9.2.5 Phy Event Counter Registers

R0100h (00000000h) • Host Port Phy Event Counter 1

Bit Position	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bits	PHY_EVT_C01																															
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Mode	Default Value	Description
31:0	PHY_EVT_C01	R/W	00000000h	Phy Event Counter 1. This register contains both the identifier and counter value. Counter identifier: read-only value 00002C01h. Counter: 32-bit counter, contains number of signature D2H register FISes that were transmitted to the host from the control port.

R0101h (00000000h) • Reserved for Phy Event Counter

Bit Position	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bits	RSVD																															
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Mode	Default Value	Description
31:0	RSVD	R	00000000h	Reserved.

⋮ ⋮ ⋮

R08FFh (00000000h) • Reserved for Phy Event Counter

Bit Position	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bits	RSVD																															
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Mode	Default Value	Description
31:0	RSVD	R	00000000h	Reserved.

R0900h (00000000h) • Reserved for General Status and Control

Bit Position	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bits	RSVD																															
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Mode	Default Value	Description
31:0	RSVD	R	00000000h	Reserved.

⋮ ⋮ ⋮

RFFFFh (00000000h) • Reserved for General Status and Control

Bit Position	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bits	RSVD																															
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Mode	Default Value	Description
31:0	RSVD	R	00000000h	Reserved.

9.2.6 Port Status and Control Registers

R0000h (00000000h) • S-Status

Bit Position	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bits	RSVD																				P_IPM_STS				P_SPD_STS				P_DET_STS			
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Mode	Default Value	Description
31:12	RSVD	R/W	00000h	Reserved. Do not change default value.
11:8	P_IPM_STS	R	0h	Port Interface Power Management State. **0h:** Device is not present, or communications not established. **1h:** Device is in active state. **2h:** Device in PARTIAL power management state. **6h:** Device in SLUMBER power management state. All other values are reserved.
7:4	P_SPD_STS	R	0h	Port Negotiated Interface Communications Speed. **0h:** No negotiated speed (device not present, or communication not established. **1h:** Negotiate SATA 1.5 Gbps communication rate. **2h:** Negotiate SATA 3.0 Gbps communication rate. All other values are reserved.
3:0	P_DET_STS	R	0h	Port Interface Device Detection and Phy State. **0h:** Device is not detected, and Phy communications is not established. **1h:** Device is present, but Phy communications is not established. **3h:** Device is present, and Phy communications is established. **4h:** Phy is in offline mode due to the interface being disabled or running in a BIST loopback mode.

R0001h (00000000h) • S-Error

Bit Position	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bits	RSVD					P_DIAG_X	RSVD		P_DIAG_S	P_DIAG_H	P_DIAG_C	P_DIAG_D	P_DIAG_B	P_DIAG_W	RSVD	P_DIAG_N	RSVD																P_ERR_C	RSVD
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Mode	Default Value	Description
31:27	RSVD	R/W	00h	Reserved. Do not change default value.

Bits	Name	Mode	Default Value	Description
26	P_DIAG_X	R/W	0h	Port Diagnostic Exchange. When set to 1, indicates that the device presence has changed since the last time this bit was cleared. The method of detecting that the device presence has changed depends on the vendor. This bit can be set any time a Phy reset initialization sequence occurs, as determined by the reception of the COMINIT signal whether in response to a new device being inserted, in response to a COMRESET having been issued, or in response to power-up.
25:24	RSVD	R/W	0h	Reserved. Do not change default value.
23	P_DIAG_S	R/W	0h	Port Diagnostic Sequence Error. When set to 1, indicates that one or more link state machine error conditions was encountered since the last time this bit was cleared. The Link Layer state machine defines the condition under which the link layer detects an erroneous transition.
22	P_DIAG_H	R/W	0h	Port Diagnostic Handshake Error. When set to 1, this bit indicates that one or more R_ERR handshake responses was received in response to a frame transmission. Such errors can be the result of a CRC error detected by the recipient, a disparity, 10-bit/8-bit decoding error, or other error condition leading to a negative handshake on a transmitted frame.
21	P_DIAG_C	R/W	0h	Port Diagnostic CRC Error. When set to 1, indicates that one or more CRC errors have occurred since the last time the bit was cleared.
20	P_DIAG_D	R/W	0h	Port Diagnostic Disparity Error. When set to 1, indicates that the incorrect disparity was detected one or more times since the last time the bit was cleared.
19	P_DIAG_B	R/W	0h	Port Diagnostic 10-Bit to 8-Bit Decode Error. When set to 1, indicates that one or more 10-bit to 8-bit decoding errors have occurred since the bit was last cleared.
18	P_DIAG_W	R/W	0h	Port Diagnostic Comm Wake. When set to 1, indicates that a COMMWAKE signal was detected by the Phy since the last time this bit was cleared.
17	RSVD	R/W	0h	Reserved. Do not change default value.

Bits	Name	Mode	Default Value	Description
16	P_DIAG_N	R/W	0h	Port Diagnostic Phy Ready Change. When set to 1, indicates that the PHYRDY signal has changed state since the last time this bit was cleared.
15:2	RSVD	R/W	0h	Reserved. Do not change default value.
1	P_ERR_R_C	R/W	0h	Port Recovered Communications Error. When set to 1, indicates that communications between the device and host was temporarily lost, but was re-established. This can arise from a device temporarily being removed, a temporary loss of Phy synchronization, or from other causes, and can be derived from the PHYRDY signal between the Phy and Link Layers. No action is required by the host software, since the operation ultimately succeeded. However, the host software could elect to track such recovered errors in order to gauge overall communications integrity, and potentially step down the negotiated communications speed.
0	RSVD	R/W	0h	Reserved. Do not change default value.

R0002h (00000004h) • S-Control/SM-Control

S-Control

Bit Position	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bits	RSVD																				P_IPM_CTL				P_SPD_CNTL				P_SPD_CNTL			
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0

Bits	Name	Mode	Default Value	Description
31:12	RSVD	R/W	00000h	Reserved. Do not change default value.
11:8	P_IPM_CTL	R/W	0h	Interface Power Control. Enables interface power management state that can be invoked via the SATA interface power management capabilities. **0h:** No interface power management state restrictions. **1h:** Transitions to the PARTIAL power management state are disabled. **2h:** Transitions to the SLUMBER power management state are disabled. **3h:** Transitions to the PARTIAL and SLUMBER power management states are disabled. All other values are reserved.

Bits	Name	Mode	Default Value	Description
7:4	P_SPD_CNTL	R/W	0h	Power Speed Control. The highest allowed communication speed the interface is allowed to negotiate when interface communications speed is established. **0h:** No speed negotiation restriction. **1h:** Limit speed negotiation to a rate not greater than the SATA Generation 1 communications rate. All other values are reserved.
3:0	P_DET_CTL	R/W	4h	Power Detection Control. Controls the device detection and interface initialization. **0h:** No interface power management state restrictions. **1h:** Performs the interface communication initialization sequence to establish communication. Functionally equivalent to a hard reset and results in the interface being reset, and communications re-initialized. **4h:** Disable the SATA interface and put the Phy in offline mode. All other values are reserved.

SM-Control

Bit Position	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bits	RSVD																												SM_DET_CTL			
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0

Bits	Name	Mode	Default Value	Description
31:4	RSVD	R/W	00000h	Reserved. Do not change default value.
3:0	SM_DET_CTL	R/W	4h	Detection Control Status. Controls the device detection and interface initialization. **0h:** No device detection or interface initialization. **1h:** Hardware reset = 1. **4h:** Disable the SEMB interface with SEP. All other values are reserved.

R0100h (00000000h) • Device Port Phy Event Counter 0

Bit Position	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bits	PHY_EVT_C00																															
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Mode	Default Value	Description
31:0	PHY_EVT_C00	R/W	00000000h	Device Port Phy Event Counter 0 This register contains both the identifier and counter value. Counter identifier: 00002C00h Counter: 32-bit counter, contains number of transmitted H2D non-Data FISes to which the port multiplier responded with R_ERR due to collision.

R0101h (00000000h) • Device Port Phy Event Counter 2

Bit Position	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bits	PHY_EVT_C02																															
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Mode	Default Value	Description
31:0	PHY_EVT_C02	R/W	00000000h	Device Port Phy Event Counter 2 This register contains both the identifier and counter value. Counter identifier: 00002C02h Counter: 32-bit counter, contains number of corrupted CRC values that were transmitted to the host.

R0102h (00000000h) • Reserved for Phy Event Counter

Bit Position	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bits	RSVD																															
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Mode	Default Value	Description
31:0	RSVD	R	00000000h	Reserved.

⋮ ⋮ ⋮

R08FFh (00000000h) • Reserved for Phy Event Counter

Bit Position	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bits	RSVD																															
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Mode	Default Value	Description
31:0	RSVD	R	00000000h	Reserved.

THIS PAGE LEFT INTENTIONALLY BLANK

A QUICK START/FREQUENTLY ASKED QUESTIONS

This appendix contains basic information on the following basic topics needed to quickly get the 88SM4140 up and running:

- Using the 88SM4140
- Using Marvell Special Features
- Ports
- Frequently Asked Questions

A.1 Using the 88SM4140

To use the 88SM4140, do the following:

1. Ensure that the 88SM4140 has the settings as shown in Table B-1.
2. Connect the host port to a PM-aware SATA host, such as the Marvell's 88SX60XX series.

   If the OS is to be installed to one of the PM's drives, ensure the drive is connected to port 0.
3. Connect drives to 88SM4140 device ports.
4. Provide power and install the complementing PM-aware driver.

   Reboot the system, if necessary.

Depending on the state of the drive, PM drives might not appear in your operating system. If this is the case, initiate and partition the drives using the disk management software for your operating system. For more information, refer to the online help for your operating system.

A.2 Using Marvell Special Features

To allow for the host bridge (such as the Marvell 88SA8040 and 88SA8050) to switch ports, the 88SM4140 switches ports based on NOP commands. For more information, contact Marvell Customer Support.

A.3 Ports

A.3.1 PM_PORT

For the 88SM4140 port multiplier to function, the host must be able to select each SATA device that is connected to the 88SM4140. To do this, a new field, PM_PORT, has been added to all SATA FISes. The host is able to access each device by changing the value of the PM_PORT field.

For more detail, refer to PM_PORT Field on page 7-2.

A.3.2 Control Ports

Each PM has a control port which provides basic device information to host. In addition, the control port also provides the host with basic control over the devices.

For more detail, refer to Control Ports on page 7-3.

Chapter 7, Ports, also contains a detailed example of the interaction between an PM-aware host and the PM.

February 1, 2007
Doc No. MV-S101553-00 Rev. G

A.4 Frequently Asked Questions

This section lists answers to the following frequently asked questions:

A.4.1 Why Use a Port Multiplier?

One of the most immediate advantages of the 88SM4140 is to increase the number of Serial ATA connections to a system. Figure A-1 and Figure A-2 illustrate this concept.

February 1, 2007
Doc No. MV-S101553-00 Rev. G

Figure A-1 Conventional SATA System

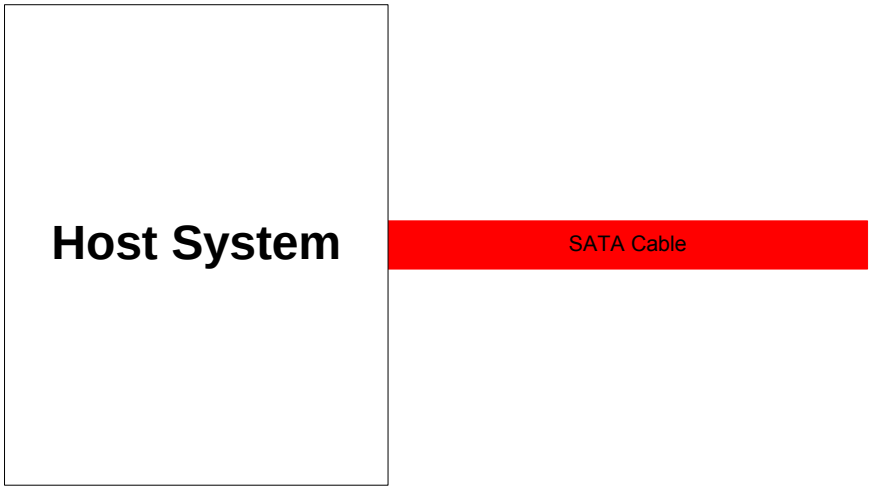
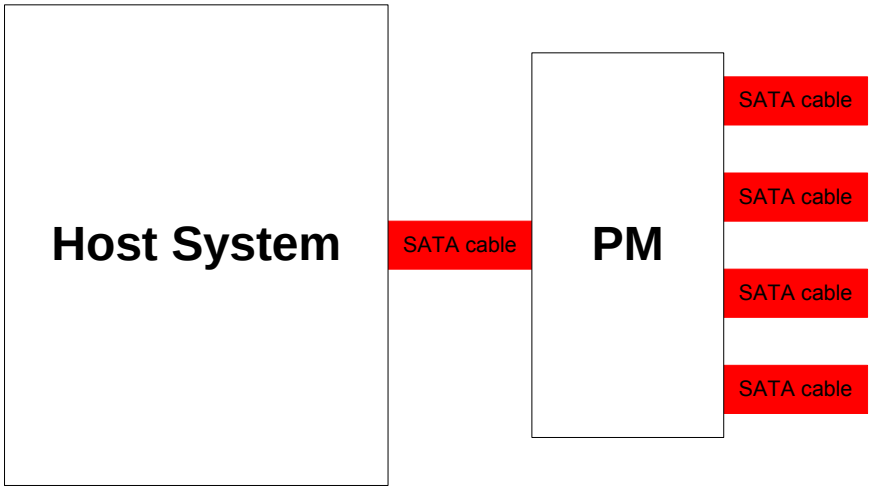


Figure A-2 Conventional SATA System With Port Multiplier



A.4.2 What Is Changed in the Port Multiplier?

In the SATA 1.0 specification, bits 11:8 are normally reserved bits in a Hostto Device Register FIS. The 88SM4140 uses these 4 reserved bits for port selection.

A port multiplier can allow up to 15 device connections, ranging from port 0 (0h) to port 14 (Eh). Port 15 (Fh) is reserved for the PM control port. The host can access the PM control port as port Fh by using the BUFFER READ (E4h) and BUFFER WRITE (E8h) ATA commands.

Refer to the section How Does the Host Access the PM Registers? on page A-9 for detail on how these ATA commands can be used with PM. The PM_PORT field must be programmed to Fh for these commands to reach the control port.

The 88SM4140 can support up to four device connections. If the SEMB feature is enabled, it is set to be device 4 (4h). Refer to the section What is SEMB? on page A-11 for more information on how to enable SEMB in the 88SM4140.

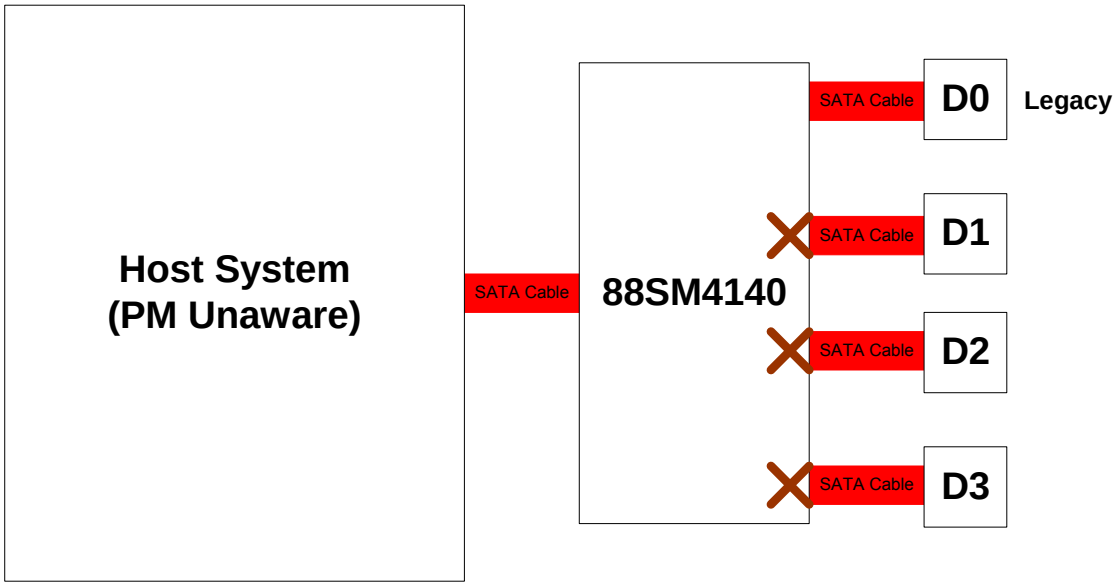
A.4.3 Does the Port Multiplier Work With Existing SATA Products?

The 88SM4140 Port Multiplier is an extension of the SATA 1.0 specification. Thus, existing SATA products are still usable on a PM system. But in order for the host system to access more than one drive on a single SATA channel, additional configuration information must be provided.

A.4.4 What If My SATA Host Does Not Support the Port Multiplier? Or If My SATA Host Supports Port Multiplier But My Driver Does Not?

Then the 88SM4140 Port Multiplier does not add any value, as the host system can only see devices connected to port 0 on the PM. By definition, all PM ports except for port 0 are disabled. If one of the SATA drives connected to 88SM4140 is the boot drive, it should be drive 0. This is known as booting with legacy software. Figure A-3 illustrates this concept.

Figure A-3 PM-Unaware Host/Driver



A.4.5 Do I need PM-Aware SATA drives?

The drives do not need to be PM-aware. For example, when a PM-aware host is sending FISes to the drive connected to port 2 on the PM, bits 11:8 of each FIS = 2h. Once the PM detects this value, it redirects the FISes to the drive that is connected to port 2.

February 1, 2007
Doc No. MV-S101553-00 Rev. G

When the device connected to port 2 sends FISes to the host, bits 11:8 of each FISes are programmed to 0h. It is the PM that sets bits 11:8 of each FIS = 2h.

A.4.6 Why Are the Other PM Ports Disabled?

The other drives are disabled in order to support the staggered spin-up feature. If the proper driver is installed, it tries to detect the PM. Once it has detected that a PM is connected, it proceeds to check for drives on each PM port. Next, the driver enables the ports to which a drive is connected. For a PM-aware host (including driver), all drives are available upon boot up.

Diagrams Figure A-4 through Figure A-9 illustrate the process of staggered spin-up.

Figure A-4 Legacy Software Booting From Drive 0 (Ports 1-3 are disabled)

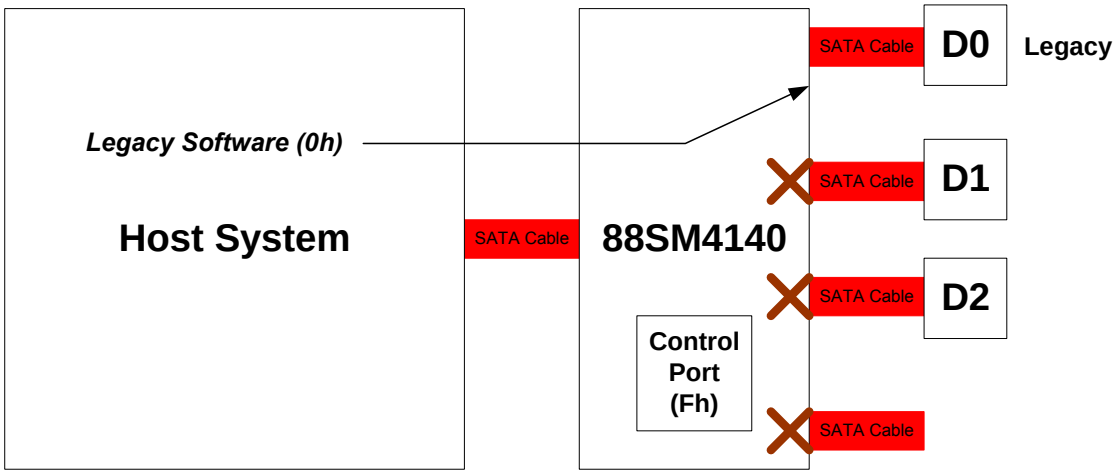


Figure A-5 PM-Aware Driver Present, Driver Accesses Control Port to Enable Drive D1

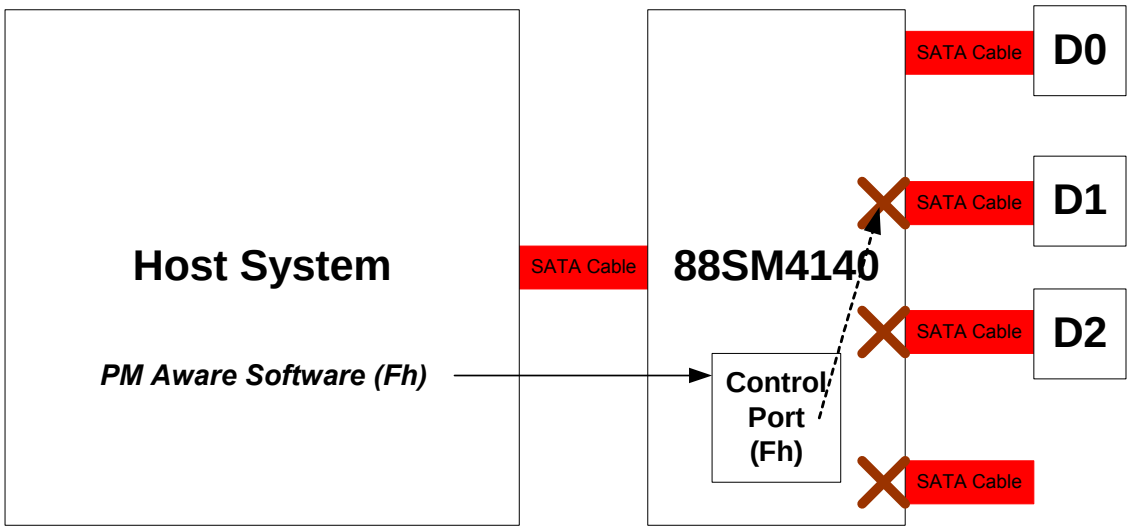


Figure A-6 PM-Aware Driver Present, Driver Accesses Control Port to Enable Drive D2

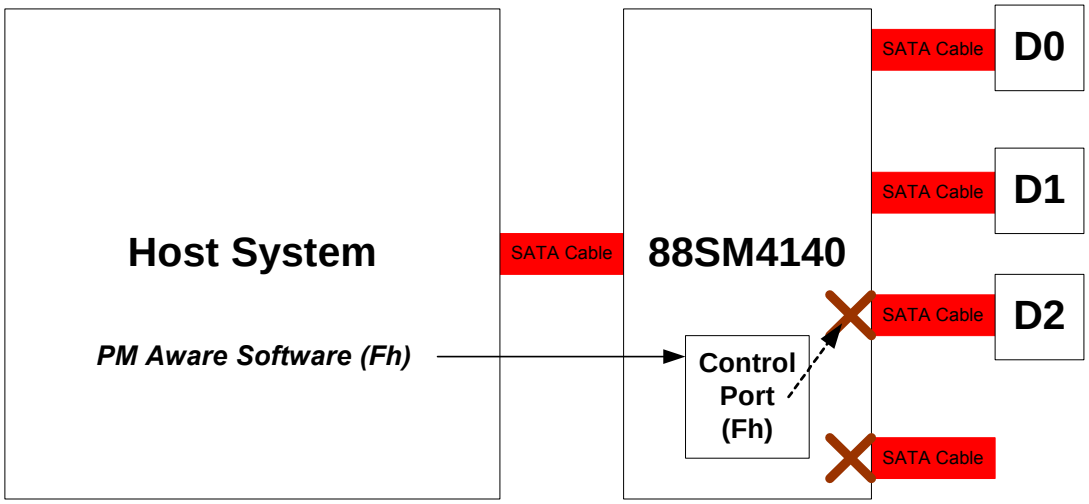


Figure A-7 PM-Aware Driver Present, Driver Accesses Control Port to Enable Drive D3 (which is not present)

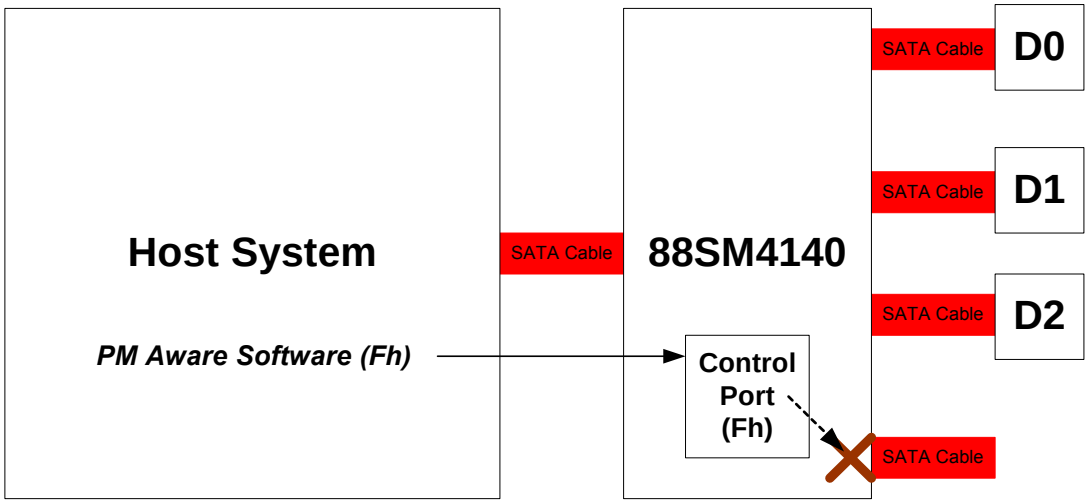


Figure A-8 PM-Aware Driver Present, Driver Can Now Access Drive D1

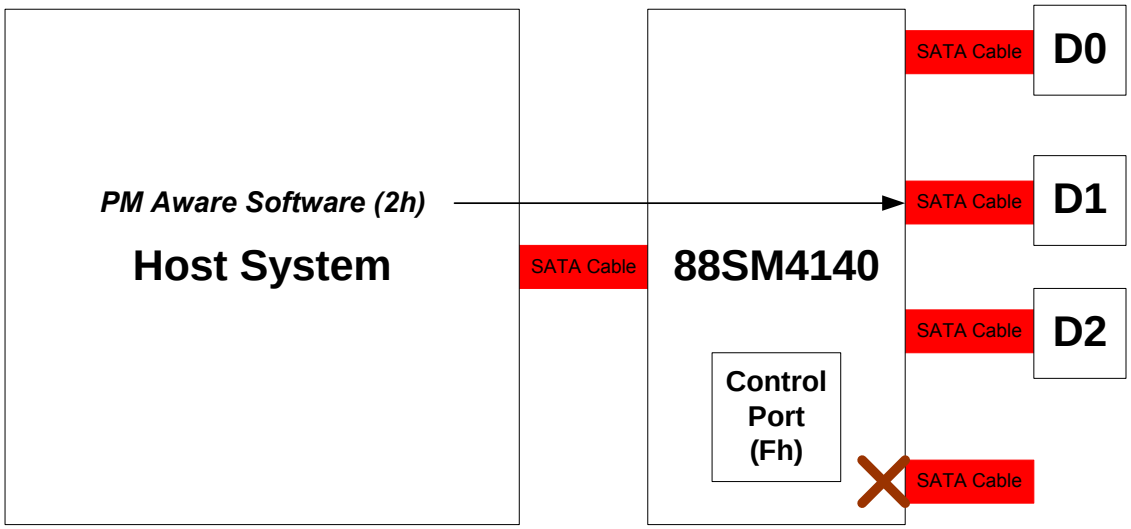
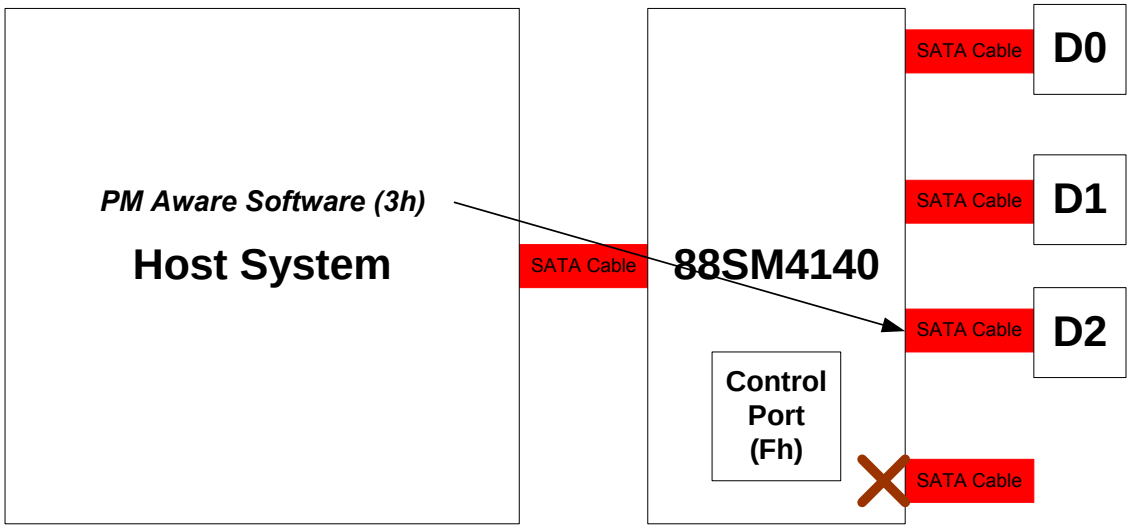


Figure A-9 PM-Aware Driver Present, Driver Can Now Access Drive D2



A.4.7 How Do The Drives Appear in a Windows System?

Drives connected to the PM appear normally as they would in any other setup.

A.4.8 Can I Convert All the PM-Connected Drives Into Just One?

Yes, if Windows 2000 or Windows XP are being used. Simply convert the PM-connected drives to dynamic and configure them as either mirrored or stripped. Refer to your Windows Computer Management online help for more information.

Alternatively, use PM-aware SATA RAID controllers.

A.4.9 How Does the Host Access the PM Registers?

The PM registers (GSCR and PSCR) can be accessed using the ATA BUFFER READ and BUFFER WRITE commands. The following sections from the Serial ATA II: Port Multiplier Specification detail the command definitions used to access the PM registers.

A.4.9.1 Read PM

The format for reading PM registers is given in Table A-1, and the results from this command is given in Table A-2 through Table A-3.

Table A-1 Read PM Registers Command Definition

SATA Register	7	6	5	4	3	2	1	0
Features	RegNum							
Features (expected)	N/A							
Sector Count	Reserved (0)							
Sector Count (expected)	N/A							
Sector Number	Reserved (0)							
Sector Number (expected)	N/A							
Cylinder Low	Reserved (0)							
Cylinder Low (expected)	N/A							
Cylinder High	Reserved (0)							
Cylinder High (expected)	N/A							
Device/Head	N/A				PortNum			
Command	E4h							

Table A-2 Read PM Success Status Result Values

SATA Register	7	6	5	4	3	2	1	0
Error	0							
Sector Count	Value [7:0]							
Sector Count (expected)	N/A							
Sector Number	Value [15:8]							
Sector Number (expected)	N/A							
Cylinder Low	Value [23:16]							
Cylinder Low (expected)	N/A							

Table A-2 Read PM Success Status Result Values

SATA Register	7	6	5	4	3	2	1	0
Cylinder High	Value [31:24]							
Cylinder High (expected)	N/A							
Device/Head	Reserved (0)							
Status	BSY	DRDY	DF	N/A	DRQ	0	0	ERR

Table A-3 Read PM Error Status Result Values

SATA Register	7	6	5	4	3	2	1	0
Error	Reserved (0)					ABRT	REG	PORT
Sector Count	Reserved (0)							
Sector Count (expected)	N/A							
Sector Number	Reserved (0)							
Sector Number (expected)	N/A							
Cylinder Low	Reserved (0)							
Cylinder Low (expected)	N/A							
Cylinder High	Reserved (0)							
Cylinder High (expected)	N/A							
Device/Head	Reserved (0)							
Status	BSY	DRDY	DF	N/A	DRQ	0	0	ERR

A.4.9.2 Write PM

The format for reading PM registers is given in Table A-4, and the results from this command is given in Table A-5 through Table A-6.

Table A-4 Write PM Registers Command Definition

SATA Register	7	6	5	4	3	2	1	0
Features	RegNum							
Features (expected)	N/A							
Sector Count	Value [7:0]							
Sector Count (expected)	N/A							
Sector Number	Value [15:8]							
Sector Number (expected)	N/A							
Cylinder Low	Value [23:16]							
Cylinder Low (expected)	N/A							
Cylinder High	Value [31:24]							
Cylinder High (expected)	N/A							
Device/Head	N/A					PortNum		
Command	E8h							

Table A-5 Write PM Success Status Result Values

SATA Register	7	6	5	4	3	2	1	0
Error	0							
Sector Count	Reserved (0)							
Sector Count (expected)	N/A							
Sector Number	Reserved (0)							
Sector Number (expected)	N/A							
Cylinder Low	Reserved (0)							
Cylinder Low (expected)	N/A							
Cylinder High	Reserved (0)							
Cylinder High (expected)	N/A							
Device/Head	Reserved (0)							
Status	BSY	DRDY	DF	N/A	DRQ	0	0	ERR

Table A-6 Write PM Error Status Result Values

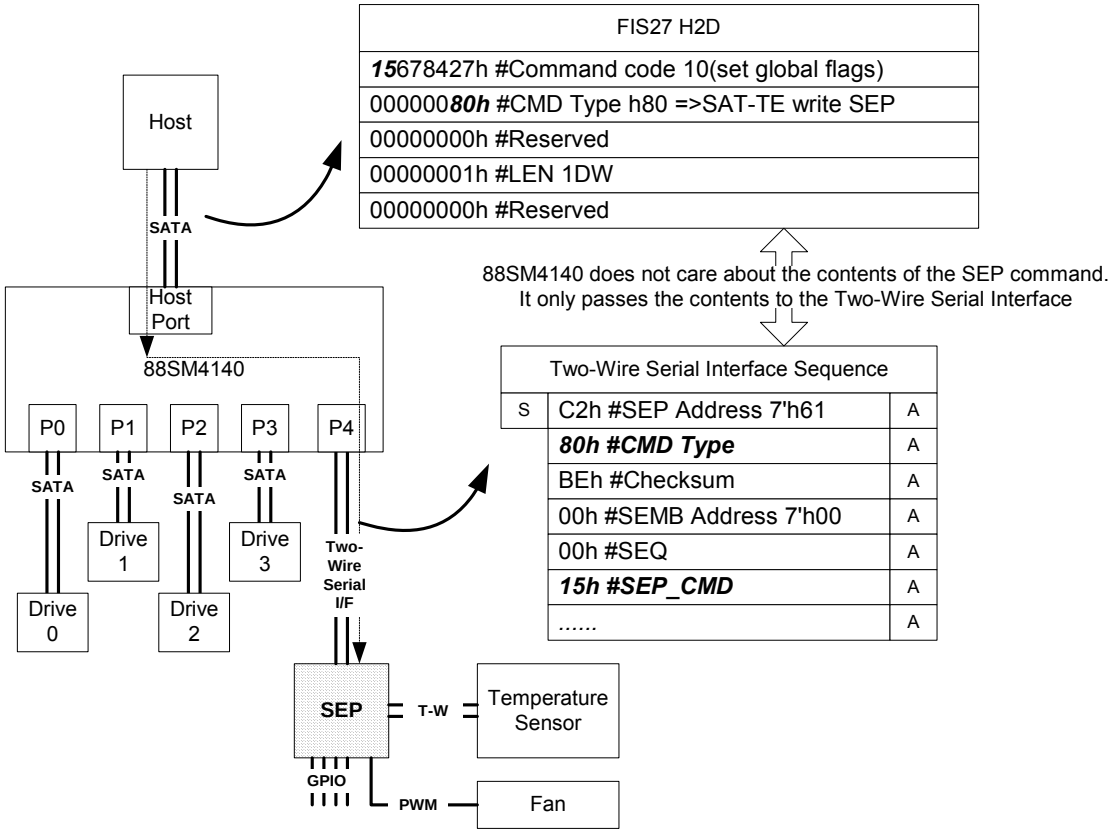
SATA Register	7	6	5	4	3	2	1	0
Error	Reserved (0)					ABRT	REG	PORT
Sector Count	Reserved (0)							
Sector Count (expected)	N/A							
Sector Number	Reserved (0)							
Sector Number (expected)	N/A							
Cylinder Low	Reserved (0)							
Cylinder Low (expected)	N/A							
Cylinder High	Reserved (0)							
Cylinder High (expected)	N/A							
Device/Head	Reserved (0)							
Status	BSY	DRDY	DF	N/A	DRQ	0	0	ERR

A.4.10 What is SEMB?

The Serial ATA Enclosure Management Bridge (SEMB) translates information on the SATA bus to a serial bus that controls devices such as the LED, the fan, and the sensors.

The 88SM4140 supports the Storage Enclosure Management Bridge service as part of the topology shown in Figure A-10. The SEMB inside the 88SM4140 consists of controller logic that bridges the Two-Wire Serial interface to the Serial ATA interface using a logical ATA command block register. The host sends commands to the SEP through the SATA interface to the 88SM4140, and the 88SM4140 then translates to the Two-Wire Serial interface which connects with the SEP. The SEP provides the embedded functions needed for monitoring and managing storage enclosure. Figure A-10 illustrates this concept.

Figure A-10 SEP Architecture



Functionality such as door lock sense, PWM fan control, device present detection, and temperature sensing can be provided by the SEP.

Refer to the *Serial ATA II: Extensions to Serial ATA1.0a* specification for more information.

A.4.11 Is SEMB Compatible WIth All Versions of the SAF-TE or SES Commands?

Yes. The SEMB service is transparent to SCSI Access Fault-Tolerant Enclosures (SAF-TE) and SCSI Enclosure Spaces (SES) command content.

A.4.12 How Do I Detect If a Port is SEMB?

The host can check the device signature by sending a Soft Reset. The SEMBhas a signature of C33C0101h. Table A-7 shows the command reference for the SEMB.

Table A-7 SEMB Signature Command Reference

SATA Register	7	6	5	4	3	2	1	0
Error					00h			
Sector Count					01h			
Sector Count (expected)					00h			
Sector Number					01h			
Sector Number (expected)					00h			
Cylinder Low					3Ch			
Cylinder Low (expected)					00h			
Cylinder High					C3h			
Cylinder High (expected)					00h			
Device/Head					00h			
Status	BSY	DRDY	DF	N/A	DRQ	0	0	ERR

A.4.13 How Do I Access the SEMB?

To use the SEMB feature, set TESTMODE [1:0] = 2h. Once this is done, the SEMB can be accessed through port 4. In this case, PORT_NUM (R0002h [3:0]) = 5h.

1. Select the PM control port
2. Read the number of ports on PM

For example:

```
# WTASK <CH> <FE> <SC> <SN> <CL> <CH> <DH> <CMD>
wtask 0 2 0 0 0 0 f e4
# CTASK <CH> <ERR> <SC> <SN> <CL> <CH> <DH> <STS>
ctask 0 0 5 0 0 0 0 50
# expected 5 (including Two-Wire Serial Interface)
```

3. Change to port 4 (Two-Wire Serial Interface port).
4. The SRST bit gets the Two-Wire Serial Interface master signature.

For example:

```
# Soft Reset Channel 0
srst 0
# CTASK <CH> <ERR> <SC> <SN> <CL> <CH> <DH> <STS>
ctask 0 0 1 1 3c c3 0 50
# Expected C33C0101
```

A.4.14 How Do I Program the SEMB and SEP Address?

The default Two-Wire Serial Interface address for SEMB and SEP are 2Bh and 2Ch, respectively.

The address for SEP can be changed via TSC_SEP_ADDR (R0096h [14:8]).

To change the SEMB address, program TSC_SEMB_ADDR (R0096h [6:0]) and set TSC_SM_WR (R0096h [27]) to 1, TSC_SM_ADDR (R0096h [26:24]) to 0, and TSC_SM_RD_DATA / TSC_SM_WR_DATA (R0096h [23:16]) to TSC_SEMB_ADDR.

A.4.15 How Do I Access Storage Enclosure Process (SEP) Using SEMB?

In order to start using the 88SM4140 SEMB, its SEP and SEMB addresses must first be initialized. The host should use the DMA protocol for transferring data between itself and the SEMB.

Once the SEMB address has been initialized, the host can begin sending commands acceptable by the SEP device. Host-to-SEP commands should be in the form as specifiedin Table A-8.

Table A-8 Command Block Register Fields Used in SEP Communications

SATA Register	7	6	5	4	3	2	1	0
Features	SEP_CMD							
Features (expected)	Reserved.							
Sector Count	LEN							
Sector Count (expected)	Reserved							
Sector Number	CMD_TYPE							
Sector Number (expected)	Reserved							
Cylinder Low	Reserved							
Cylinder Low (expected)	Reserved							
Cylinder High	Reserved							
Cylinder High (expected)	Reserved							
Device/Head	0	1	0	0	Reserved			
Command	SEP_ATTN (67h)							

Table A-9 details the SEP command codes.

Table A-9 SEP Commands

Command	Description
SEP_CMD	Specifies the SAF-TE or SES command code to be issued. See the SCSI Accessed Fault-Tolerant Enclosures (SAF-TE) and SCSI Enclosure Surfaces (SES) references for the command codes and their functions.
LEN	The transfer length of the data transfer phase of the command in Dword units. Valid values are 1-255 (yielding a maximum transfer length of 1020 bytes). Data transfers that are not a multiple of four bytes are padded by the transmitter with zeros to the next 4-byte (Dword) granularity.

Table A-9 SEP Commands

Command	Description
CMD_TYPE	Flag indicating whether the issued SEP command is a SAF-TE command code or an SES command code, and whether the data transfer protocol is from SEP-to-host or host-to-SEP. The encoding of the field is as follows: **00h**: SAF-TE command code with SEP-to-host data transfer (SAF-TE Read Buffer). **02h**: SES command code with SEP-to-host data transfer (SES Receive Diagnostic). **80h**: SAF-TE command code with host-to-SEP data transfer (SAF-TE Write Buffer). **82h**: SES command code with host-to-SEP data transfer (SES Send Diagnostic). All other values are reserved.

A.4.15.1 Two-Wire Serial Interface Read/Write

Figure A-11 and Figure A-12 illustrate the Two-Wire Serial Interface traffic for both Read and Write SEP activity.

Figure A-11 Two-Wire Serial Interface Transactions for Read SEP Command

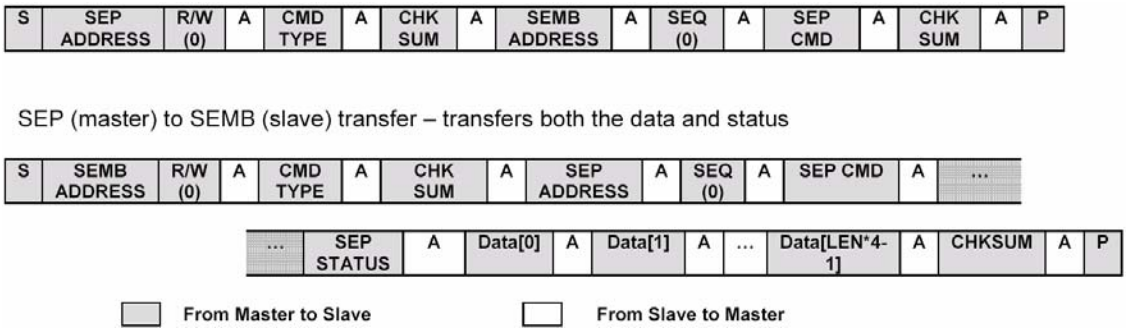
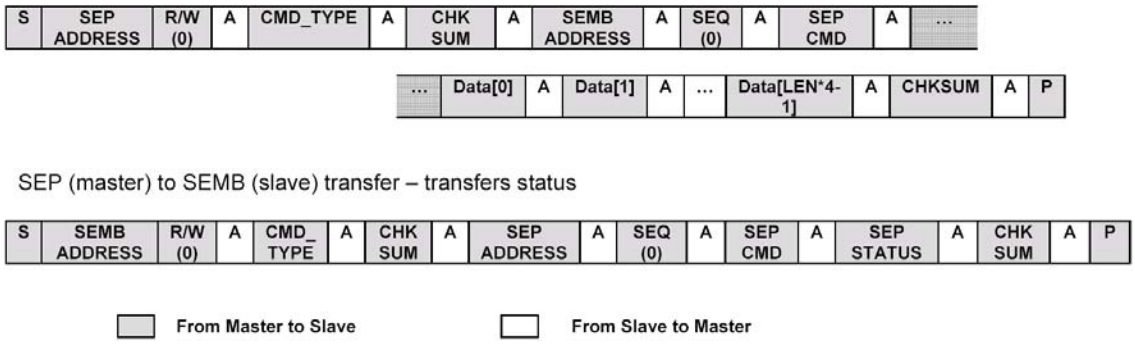


Figure A-12 Two-Wire Serial Interface Transactions for Write SEP Command



The following shows the PM port switch operation:

```
#######################
# Switch to PM port F #
#######################

################################################
# Setup SEMB addr = 0000h and SEP addr = 0061h #
################################################
# WTASK <Ch> <FE> <SC> <SN> <CL> <CH> <DH> <CMD>
wtask 0 96 00 61 00 08 0F E8

###################################
# Switch to PM port 4 (SEMB port) #
###################################

################################################
# Send SAF-TE read cmd "ID SEP" to Q-Logic SEP #
################################################
# WTASK <Ch> <FE> <SC> <SN> <CL> <CH> <DH> <CMD>
wtask 0 EC 10 00 00 00 40 67
# RSEP <Ch> <Sz in DW> ... this is a read DMA for stated number of
Dwords
rsep 0 10
# Dump read buffer for visual check
drb 0 10

############################################################
# Send SAF-TE read cmd "READ GLOBAL FLAGS" to Q-Logic SEP #
############################################################
# WTASK <Ch> <FE> <SC> <SN> <CL> <CH> <DH> <CMD>
wtask 0 05 03 00 00 00 40 67
```

```
# RSEP <Ch> <Sz in DW> ... this is a read DMA for stated number of
Dwords
rsep 0 3
# Dump read buffer for visual check
drb 0 10

################################################################
# Send SAF-TE write cmd "SEND GLOBAL FLAGS" to Q-Logic SEP #
################################################################
# WTASK <Ch> <FE> <SC> <SN> <CL> <CH> <DH> <CMD>
wtask 0 15 03 80 00 00 40 67
# WSEP <Ch> <Sz in DW> ... this is a write DMA for stated number of
Dwords
wsep 0 3 FFFFFFFF FFFFFFFF FFFFFFFF
```

A.4.16 How do I Access Windbond WD83792 Hardware Monitor IC Using SEMB?

This special feature is vendor-unique and is defined in 88SM4140. The value in the Sector Number field, either 8'h0F or 8'h8F, designates the vendor-unique commands. 8'h0F and 8'h8F are the read and write register commands to WD83792, respectively. The detailed command transfer is outlined below.

A.4.16.1 Write Register

CMD_TYPE 8Fh is a specific command to write register data to WD83792.

Figure A-13 Write Windbond Command

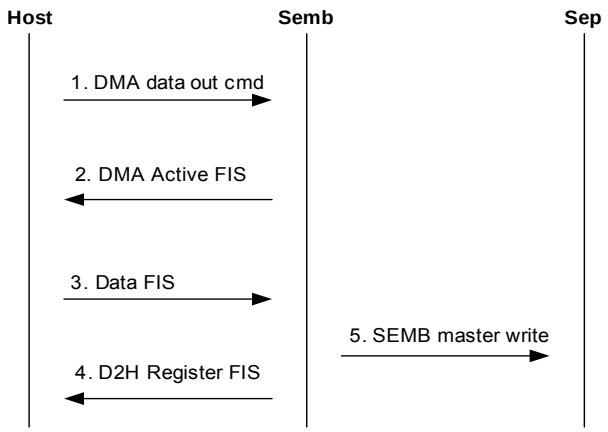


Table A-10 DMA Data Out Command

Byte Position	Byte 3	Byte 2	Byte 1	Byte 0
DWORD0	Features (REG_ ADDR)	Command (SEP_ADDN:67h)	Reserved (84h)	FIS (27h)
DWORD1	Dev/Head (00h)	Cyl High (00h)	Cyl Low (00h)	Sector Number (CMD_TYPE:8Fh)
DWORD2	Exp Feautres (00h)	Exp Cyl High (00h)	Exp Cyl Low (00h)	Exp Sector Number (00h)
DWORD3	Control (00h)	Reserved (00h)	Exp Sector Count (00h)	Sector Count (02h)
DWORD4	Reserved (00h)	Reserved (00h)	Reserved (00h)	Reserved (00h)

Table A-11 DMA Active FIS

Byte Position	Byte 3	Byte 2	Byte 1	Byte 0
DWORD0	Reserved (00h)	Reserved (00h)	Reserved (04h)	FIS (39h)

Table A-12 Data FIS

Byte Position	Byte 3	Byte 2	Byte 1	Byte 0
DWORD0	Reserved (00h)	Reserved (00h)	Reserved (00h)	FIS (46h)
DWORD1	Reserved (00h)	Reserved (00h)	Reserved (00h)	Data (REG WR DATA)

Table A-13 D2H Register FIS

Byte Position	Byte 3	Byte 2	Byte 1	Byte 0
DWORD0	Error (84h/00h)	Status (SEP_STATUS)	Reserved (04h)	FIS (34h)
DWORD1	Dev/Head (00h)	Cyl High (Reserved:00h)	Cyl Low (Reserved:00h)	Sector Number (Reserved:00h)
DWORD2	Exp Feautres (00h)	Exp Cyl High (00h)	Exp Cyl Low (00h)	Exp Sector Number (00h)
DWORD3	Reserved (00h)	Reserved (00h)	Exp Sector Count (00h)	Sector Count (00h)
DWORD4	Reserved (00h)	Reserved (00h)	Reserved (00h)	Reserved (00h)

Table A-14 SEMB Master Write

Byte	SEMB (88SM4140)	7 6 5 4 3 2 1 0	SEP (WD83792)	
	I2C Protocol	I2C Data	I2C Protocol	I2C Data
BYTE 0	Start	SEP ADDR 0		
			ACK	
BYTE 1		REG ADDR		
			ACK	
BYTE 2		REG WR DATA		
			ACK	
	Stop			

A.4.16.2 Read Register

CMD_TYPE 8Fh is a specific command to read register data from WD83792.

Figure A-14 Read Windbond Command

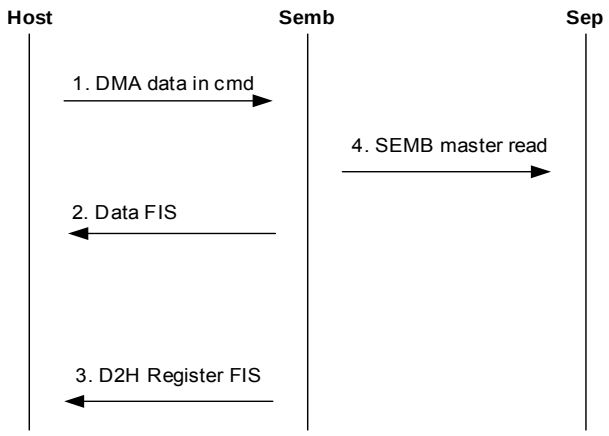


Table A-15 DMA Data In Command

Byte Position	Byte 3	Byte 2	Byte 1	Byte 0
DWORD0	Features (REG_ ADDR)	Command (SEP_ADDN:67h)	Reserved (84h)	FIS (27h)
DWORD1	Dev/Head (00h)	Cyl High (00h)	Cyl Low (00h)	Sector Number (CMD_TYPE:8Fh)
DWORD2	Exp Feautres (00h)	Exp Cyl High (00h)	Exp Cyl Low (00h)	Exp Sector Number (00h)
DWORD3	Control (00h)	Reserved (00h)	Exp Sector Count (00h)	Sector Count (02h)
DWORD4	Reserved (00h)	Reserved (00h)	Reserved (00h)	Reserved (00h)

February 1, 2007
Doc No. MV-S101553-00 Rev. G

Table A-16 Data FIS

Byte Position	Byte 3	Byte 2	Byte 1	Byte 0
DWORD0	Reserved (00h)	Reserved (00h)	Reserved (00h)	FIS (46h)
DWORD1	Data (00h)	Reserved (00h)	Reserved (00h)	REG RD DATA

Table A-17 D2H Register FIS

Byte Position	Byte 3	Byte 2	Byte 1	Byte 0
DWORD0	Error (84h/00h)	Status (51h/50h)	Reserved (04h)	FIS (34h)
DWORD1	Dev/Head (00h)	Cyl High (Reserved:00h)	Cyl Low (Reserved:00h)	Sector Number (Reserved:00h)
DWORD2	Exp Feautres (00h)	Exp Cyl High (00h)	Exp Cyl Low (00h)	Exp Sector Number (00h)
DWORD3	Reserved (00h)	Reserved (00h)	Exp Sector Count (00h)	Sector Count (00h)
DWORD4	Reserved (00h)	Reserved (00h)	Reserved (00h)	Reserved (00h)

Table A-18 SEMB Master Read

Byte	SEMB (88SM4140)	7 6 5 4 3 2 1 0	SEP (WD83792)	
	I2C Protocol	I2C Data	I2C Protocol	I2C Data
BYTE 0	Start	SEP ADDR 0		
			ACK	
BYTE 1		REG ADDR		
			ACK	
BYTE 0	Start	SEP ADDR 1		
			ACK	
BYTE 2				REG RD DATA
	Nack			
			STOP	

A.4.17 Is the UART Debug Port Found on Marvell SATA Products Still Available?

Yes.

A.4.18 Does 88SM4140 Support ATAPI?

Yes, the content does not matter to the 88SM4140.

A.4.19 Does 88SM4140 Support Device Hot Plug?

Yes. The host can program the ERR_MASK (R0021h [0]) bits to set the error status shown in Error Status (R0020h). The host software queries Error Status (R0020h) regularly for the status of each port.

If the host supports SDB notification, it can enable NOTIFY_EN (R0060h [3]). Thus, if there is an error which causes the error status bits to be asserted, the host is automatically notified.

Table A-19 and Table A-20 show the format of the SDB FIS.

Table A-19 SDB FIS: DWord 0

Byte Position	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
DWord 0	Error								RS VD	STA_HI			RS VD	STA_LO			N	I	R		PM_PORT				FIS Type							
Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	1	1	1	1	1	0	1	0	0	0	0	1

Table A-20 SDB: DWord 1

Byte Position	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
DWord 1	SActive																															
Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

A.4.20 What If There is a Problem With the Host-PM Connection?

When the host detects that a PM device connection has been lost, the host should check the Serial ATA S-Status register for the SATA link status until the SATA connection has been re-established. Once the connection has been re-established, the host need to perform then enumeration process again, and then can continue or recover the last operation.

A.4.21 Can the Current Bus Analyzer (Data Transit) be used for PM Debugging?

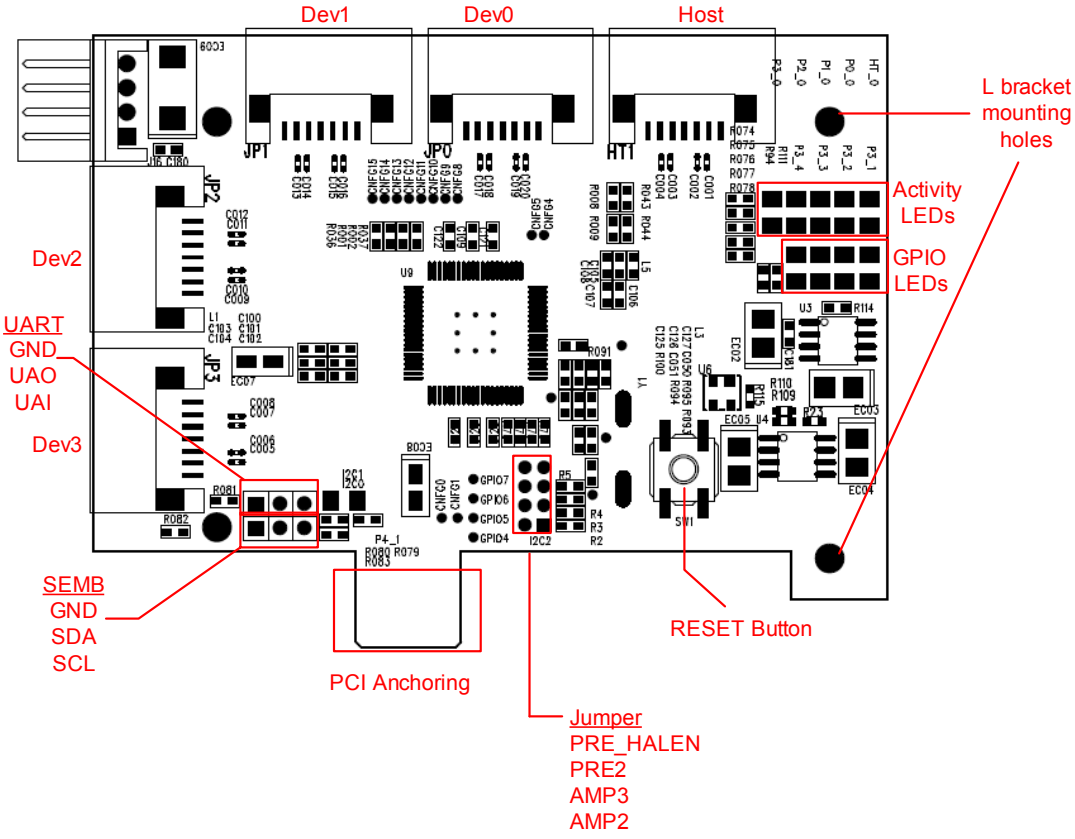
Yes.

THIS PAGE LEFT INTENTIONALLY BLANK

B EVALUATION BOARD

The evaluation board is detailed in Figure B-1.

Figure B-1 Assembly View



The configuration pin settings for the SATA interfaces are listed in Table B-1.

Table B-1 Bootstrap Pins

Pin	Bootstrap		Port LED
	0 (Pulled low)	1 (Pulled High)	
P3URT	Default value.	Reserved.	Blinks when DEV3 is active.
P2LOK	Default value.	Reserved.	Blinks when DEV2 is active.
P1NOP	Disable Marvell NOP command (Default value).	NOP command to indicate port ID.	Blinks when DEV1 is active.
P0ALL	Default PM configuration (Default value).	Forced enable to all device ports.	Blinks when DEV0 is active.
HTSSC	Disable SSC on all ports (Default value).	Enable SSC on all ports.	Blinks when HOST is active.

The configuration pin settings for the low-speed serial interfaces are listed in Table B-2.

Table B-2 Bootstrap Pins

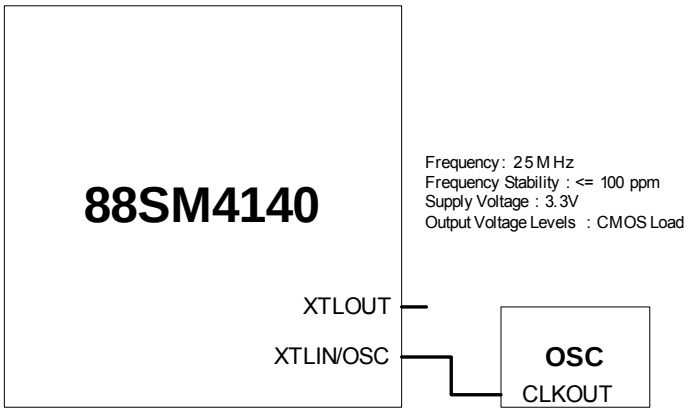
Test Mode 0		Test Mode 1		Mode
0:	R037 = 10 KΩ R02 = NC	0:	R36 = 10 KΩ R01 = NC	Normal UART (default)
0:	R037 = 10 KΩ R02 = NC	1:	R36 = NC R01 = 10 KΩ	Normal Two-Wire Serial Interface

C USING QUARTZ CRYSTAL INSTEAD OF AN OSCILLATOR

The 88SM4140 can operate on either an oscillator or quartz crystal.

The connection of an oscillator is shown in Figure 3-1.

Figure 3-1 Oscillator Connection Setup



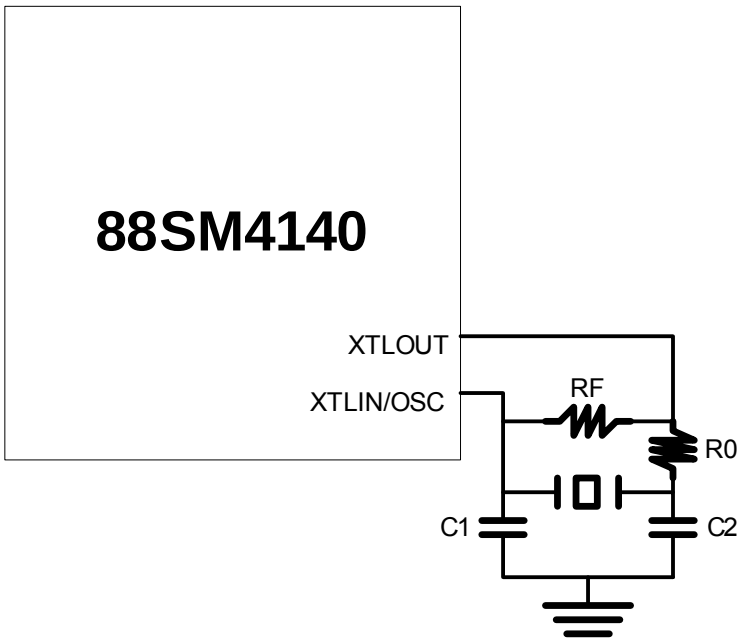
Place the oscillator close to the 88SM4140 and be sure to minimize the GND difference between the oscillator and the 88SM4140 ground. Minimizing the GND difference helps to reduce the reference clock phase jitter at 88SM4140 XTLIN/OSC pin.

Table 3-1 Crystal Requirements

Parameters	Min	Typ	Max	Units
Mode of Oscillation		Fundamental		
Cut		AT-Cut		
Frequency		20/25/30/40		MHz
Shunt Capacitance		5	7	pF
Load Capacitance	10	12	20	pF
Frequency Stability	-50		+50	ppm
Operating Temperature Range	0		70	°C
Aging			±5	ppm/year
Equivalent Series Resistance (ESR)		30	50	Ohms
Drive Level			0.1	mW

The connection of a quartz crystal is shown in Figure 3-2.

Figure 3-2 Quartz Crystal Connection Setup



For the system to operate properly, the 88SM4140 Reset pin should only be released at a ramped and stable power setting of 1.2V/3.3V, and when the clock is toggling at full amplitude.

The values of C1,C2, R0 and RF should be optimized with the specific quartz crystal specification. Place the quartz crystal close to the 88SM4140 and be sure to minimize the GND difference between the crystal and the 88SM4140 ground.

D TX AMPLITUDE AND PRE-EMPHASIS SETTINGS

The Tx amplitude and pre-emphasis settings listed below are for reference only—not all settings are listed. The actual results may vary, and depend on PCB design, trace, process, and temperature of the environment.

Table D-1 is an example of Tx amplitude settings.

Table D-1 Low Tx Amplitude Settings

DRV_EN (R009Dh [5:0])	TXAMP (R0091h [0])	Tx Amplitude (mV) IBIASX2_EN (R009Dh [8]) = 0
111111	0000	900
111111	0001	960
111111	0010	1020
111111	0011	1080
111111	0100	1140
111111	0101	1200
111111	0110	1260
111111	0111	1320
111111	1000	1380
111111	1001	1440
111111	1010	1500
111111	1011	1560
111111	1100	1620
101010	0000	450
101010	0001	480
101010	0010	510
101010	0011	540
101010	0100	570
101010	0101	600
101010	0110	630
101010	0111	660
101010	1000	690
101010	1001	720
101010	1010	750
101010	1011	780
101010	1100	810
100001	0000	300
100001	0001	320
100001	0010	340

Table D-1 Low Tx Amplitude Settings (continued)

DRV_EN (R009Dh [5:0])	TXAMP (R0091h [0])	Tx Amplitude (mV) IBIASX2_EN (R009Dh [8]) = 0
100001	0011	360
100001	0100	380
100001	0101	400
100001	0110	420
100001	0111	440
100000	0101	200
100000	0110	210
100000	0111	220
100000	1000	230
100000	1001	240
100000	1010	250
100000	1011	260
100000	1100	270

Table D-2 is an example of Tx pre-emphasis settings.

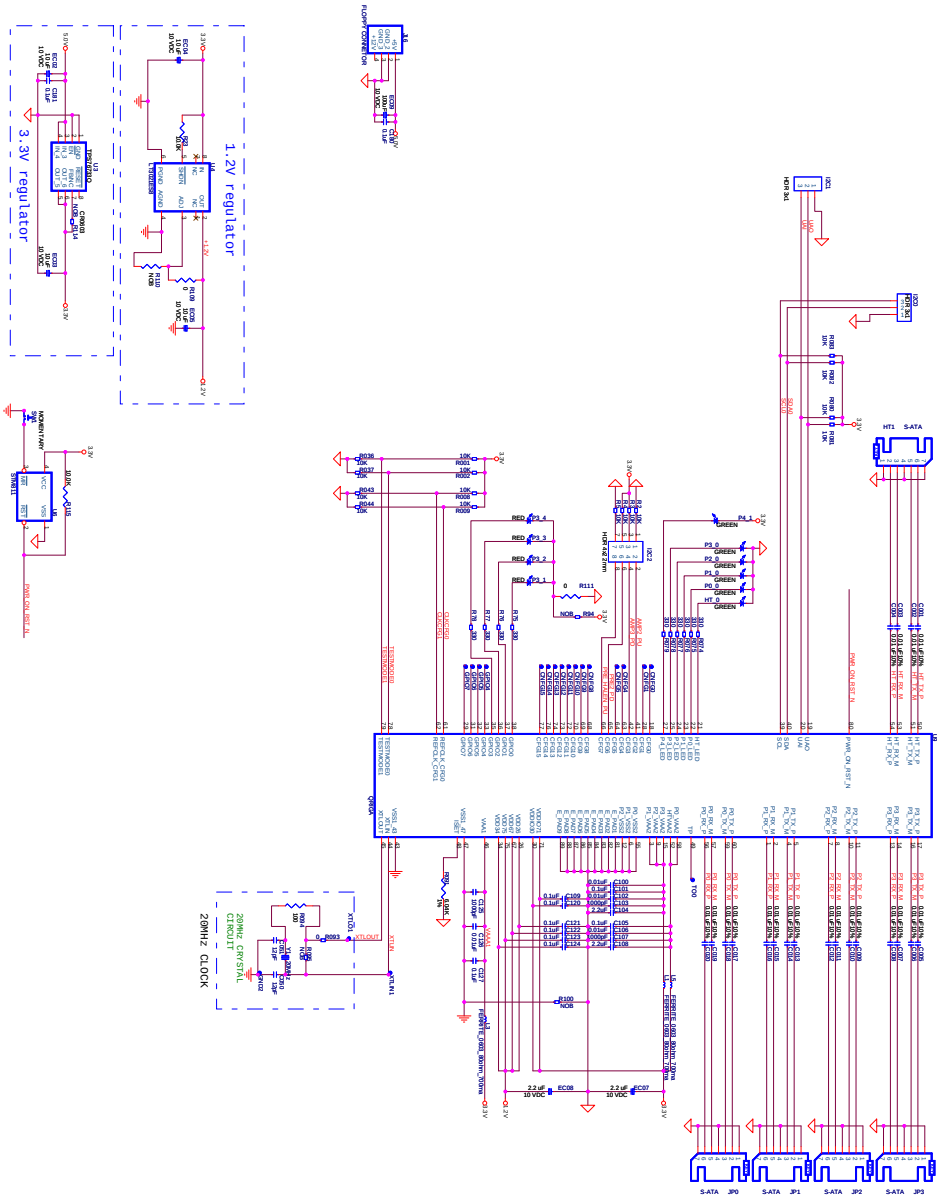
Table D-2 Tx Pre-emphasis Settings

DRV_EN (R009Dh [5:0])	PRE_HALF_EN (R009Dh [9])	TXPRE (R0091h [0]) (%)							
		000	001	010	011	100	101	110	111
111111	0:	0	4.17	8.34	12.51	16.68	20.85	25.02	29.19
	1:	0	2.085	4.17	6.255	8.34	10.425	12.51	14.595
101010	0:	0	8.34	16.68	25.02	33.36	41.7	50.04	58.38
	1:	0	4.17	8.34	12.51	16.68	20.85	25.02	29.19
100001	0:	0	12.5	25	37.5	-	-	-	-
	1:	0	6.25	12.5	18.75	25	31.25	-	-
100000	0:	0	25	-	-	-	-	-	-
	1:	0	12.5	25	-	-	-	-	-

E REFERENCE SCHEMATIC

The reference schematic for 88SM4140 is detailed in Figure E-1.

Figure E-1 Oscillator Connection Setup



THIS PAGE LEFT INTENTIONALLY BLANK

MARVELL®

MOVING FORWARD FASTER®

Marvell Semiconductor, Inc.

5488 Marvell Lane
Santa Clara, CA 95054, USA

Tel: 1.408.222.2500
Fax: 1.408.752.9028

www.marvell.com

Worldwide Corporate Offices

Marvell Semiconductor, Inc.
5488 Marvell Lane
Santa Clara, CA 95054, USA
Tel: 1.408.222.2500
Fax: 1.408.752.9028

Marvell Asia Pte, Ltd.
151 Lorong Chuan, #02-05
New Tech Park, Singapore 556741
Tel: 65.6756.1600
Fax: 65.6756.7600

Marvell Japan K.K.
Shinjuku Center Bldg. 44F
1-25-1, Nishi-Shinjuku, Shinjuku-ku
Tokyo 163-0644, Japan
Tel: 81.3.5324.0355
Fax: 81.3.5324.0354

Marvell Semiconductor Israel, Ltd.
6 Hamada Street
Mordot HaCarmel Industrial Park
Yokneam 20692, Israel
Tel: 972.4.909.1500
Fax: 972.4.909.1501

Marvell Semiconductor Korea, Ltd.
Rm. 1603, Korea Trade Center 159-1
Samsung-Dong, Kangnam-Ku
Seoul, Korea 135-729
Tel: 82.2.551-6070-6079
Fax: 82.2.551.6080

Radlan Computer Communications, Ltd.
Atidim Technological Park, Bldg. #4
P O Box 58179
Tel Aviv 61580, Israel
Tel: 972.3.645.8555
Fax: 972.3.645.8544

Worldwide Sales Offices

Western US

Marvell
5488 Marvell Lane
Santa Clara, CA 95054, USA
Tel: 1.408.222.2500
Fax: 1.408.752.9028
Sales Fax: 1.408.752.9029

Central US

Marvell
9600 North MoPac Drive, Suite #215
Austin, TX 78759, USA
Tel: 1.512.343.0593
Fax: 1.512.340.9970

Eastern US/Canada

Marvell
Parlee Office Park
1 Meeting House Road, Suite 1
Chelmsford, MA 01824 , USA
Tel: 1.978.250.0588
Fax: 1.978.250.0589

Europe

Marvell
c/o Harts CA
3 Churchgates
Church Lane
Berkhamsted
Hertfordshire, HP4 2UB
United Kingdom
Tel: 44.1442.263341
Fax: 44.1442.211543

Israel

Marvell
6 Hamada Street
Mordot HaCarmel Industrial Park
Yokneam 20692, Israel
Tel: 972.4.909.1500
Fax: 972.4.909.1501

China

Marvell
10J, No. 1800, Zhong Shan West Road
Shanghai, PRC 200235
Tel: 86.21.6440.1350
Fax: 86.21.6440.1705

Marvell
Rm. 1102/1103, Jintai Fudi Mansion
#9 An Ning Zhuang West Rd.
Qing He, Haidian District
Beijing, PRC 100085
Tel: 86.10.8274.3831
Fax: 86.10.8274.3830

Japan

Marvell
Shinjuku Center Bldg. 44F
1-25-1, Nishi-Shinjuku, Shinjuku-ku
Tokyo 163-0644, Japan
Tel: 81.3.5324.0355
Fax: 81.3.5324.0354

Taiwan

Marvell
2Fl., No.1, Alley 20, Lane 407, Sec. 2
Ti-Ding Blvd., Nei Hu District
Taipei, Taiwan, 114, R.O.C
Tel: 886.2.8177.7071
Fax: 886.2.8752.5707

Korea

Marvell
Rm. 1603, Korea Trade Center 159-1
Samsung-Dong, Kangnam-Ku
Seoul, Korea 135-729
Tel: 82.2.551-6070-6079
Fax: 82.2.551.6080

For more information, visit our website at: www.marvell.com