



3.3V CMOS Static RAM for Automotive Applications 1 Meg (64K x 16-Bit)

IDT71V016SA

Features

- ◆ 64K x 16 advanced high-speed CMOS Static RAM
- ◆ Equal access and cycle times
— Automotive: 12/15/20ns
- ◆ One Chip Select plus one Output Enable pin
- ◆ Bidirectional data inputs and outputs directly LVTTTL-compatible
- ◆ Low power consumption via chip deselect
- ◆ Upper and Lower Byte Enable Pins
- ◆ Single 3.3V power supply
- ◆ Available in 44-pin Plastic SOJ, 44-pin TSOP, and 48-Ball Plastic FBGA packages

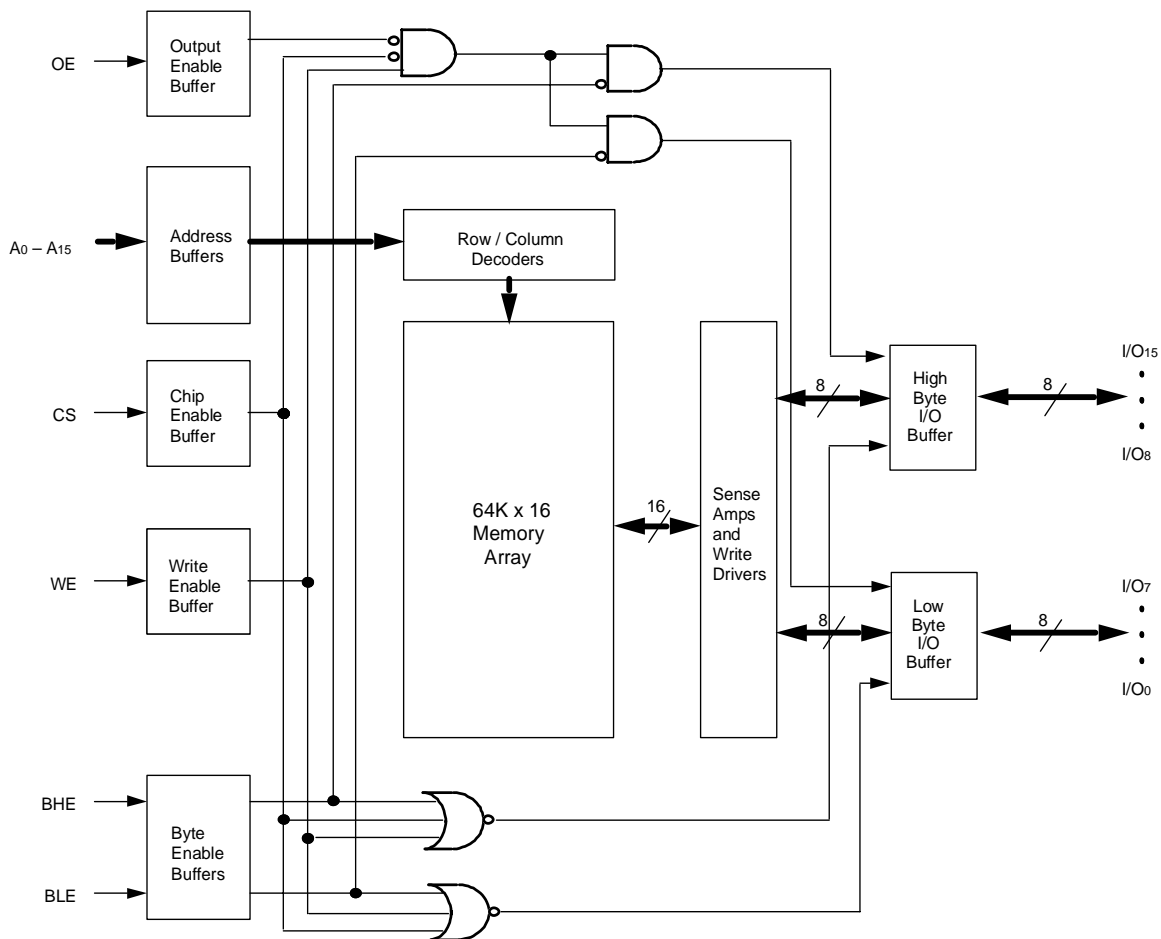
Description

The IDT71V016 is a 1,048,576-bit high-speed Static RAM organized as 64K x 16. It is fabricated using IDT's high-performance, high-reliability CMOS technology. This state-of-the-art technology, combined with innovative circuit design techniques, provides a cost-effective solution for high-speed memory needs and automotive applications.

The IDT71V016 has an output enable pin which operates as fast as 5ns, with address access times as fast as 10ns. All bidirectional inputs and outputs of the IDT71V016 are LVTTTL-compatible and operation is from a single 3.3V supply. Fully static asynchronous circuitry is used, requiring no clocks or refresh for operation.

The IDT71V016 is packaged in a JEDEC standard 44-pin Plastic SOJ, a 44-pin TSOP Type II, and a 48-ball plastic 7 x 7 mm FBGA.

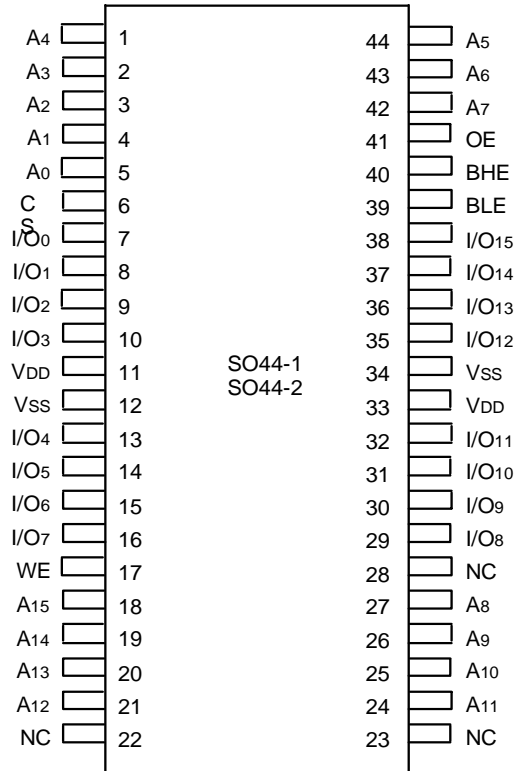
Functional Block Diagram



6818 drw 01

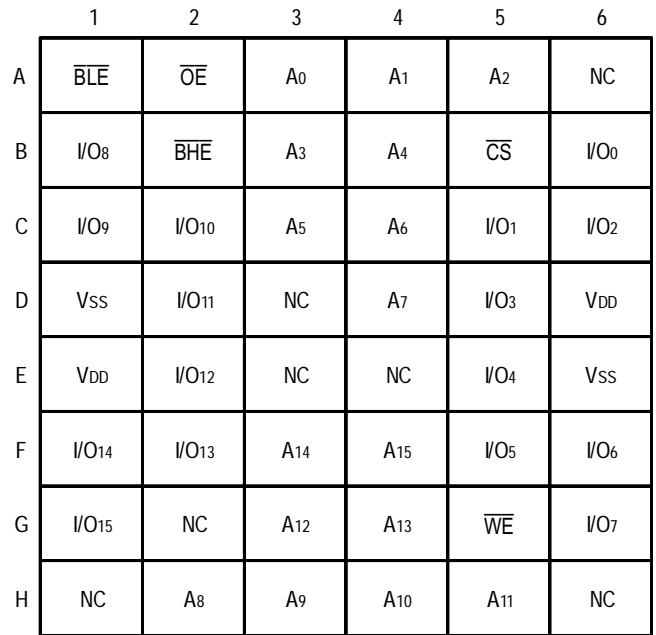
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Pin Configurations



SOJ/T SOP
Top View

6818 drw 02



FBGA (BF48-1)
Top View

6818 tbl 02a

Pin Description

Truth Table⁽¹⁾

\overline{CS}	\overline{OE}	\overline{WE}	\overline{BLE}	\overline{BHE}	I/O ₀ -I/O ₇	I/O ₈ -I/O ₁₅	Function
H	X	X	X	X	High-Z	High-Z	Deselected – Standby
L	L	H	L	H	DATA _{OUT}	High-Z	Low Byte Read
L	L	H	H	L	High-Z	DATA _{OUT}	High Byte Read
L	L	H	L	L	DATA _{OUT}	DATA _{OUT}	Word Read
L	X	L	L	L	DATA _{IN}	DATA _{IN}	Word Write
L	X	L	L	H	DATA _{IN}	High-Z	Low Byte Write
L	X	L	H	L	High-Z	DATA _{IN}	High Byte Write
L	H	H	X	X	High-Z	High-Z	Outputs Disabled
L	X	X	H	H	High-Z	High-Z	Outputs Disabled

NOTE:

1. H = V_H, L = V_L, X = Don't care.

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Absolute Maximum Ratings⁽¹⁾

Symbol	Rating	Value	Unit
V _{DD}	Supply Voltage Relative to V _{SS}	-0.5 to +4.6	V
V _{IN} , V _{OUT}	Terminal Voltage Relative to V _{SS}	-0.5 to V _{DD} +0.5	V
T _{BIAS}	Temperature Under Bias	-55 to +125	°C
T _J	Junction Temperature Page	-40 to +150	°C
T _{STG}	Storage Temperature	-65 to +150	°C
P _T	Power Dissipation	1.25	W
I _{OUT}	DC Output Current	50	mA

NOTE: 6818 tbl 03

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Capacitance

(T_A = +25°C, f = 1.0MHz, SOJ/TSOP package)

Symbol	Parameter ⁽¹⁾	Conditions	Max.	Unit
C _{IN}	Input Capacitance	V _{IN} = 3dV	6	pF
C _{VO}	I/O Capacitance	V _{OUT} = 3dV	7	pF

NOTE: 6818 tbl 06

- This parameter is guaranteed by device characterization, but not production tested.

DC Electrical Characteristics

(V_{DD} = Min. to Max., Automotive Temperature Ranges)

Symbol	Parameter	Test Conditions	Automotive Temperature Grade	IDT71V016SA		Unit
				Min.	Max.	
I _L	Input Leakage Current	V _{DD} = Max., V _{IN} = V _{SS} to V _{DD}	1 and 2	—	5	μA
			3 and 4	—	1	
I _O	Output Leakage Current	V _{DD} = Max., \overline{CS} = V _{IH} , V _{OUT} = V _{SS} to V _{DD}	1 and 2	—	5	μA
			3 and 4	—	1	
V _{OL}	Output Low Voltage	I _{OL} = 8mA, V _{DD} = Min.	—	0.4	V	
V _{OH}	Output High Voltage	I _{OH} = -4mA, V _{DD} = Min.	2.4	—	V	

6818 tbl 07

Recommended Operating Temperature and Supply Voltage

Grade	Temperature	V _{SS}	V _{DD}
Automotive Grade 1	-40°C to +125°C	0V	See Below
Automotive Grade 2	-40°C to +105°C	0V	See Below
Automotive Grade 3	-40°C to +85°C	0V	See Below
Automotive Grade 4	0°C to +70°C	0V	See Below

6818 tbl 04

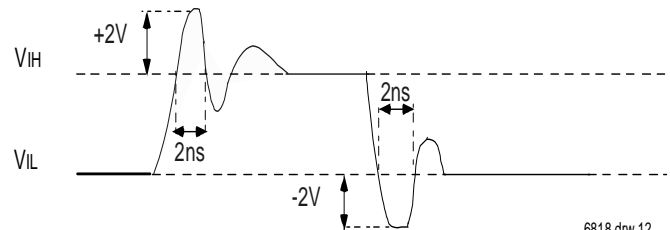
Recommended DC Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit
V _{DD}	Supply Voltage	3.0	3.3	3.6	V
V _{SS}	Ground	0	0	0	V
V _{IH}	Input High Voltage	2.0	—	V _{DD} +0.3 ⁽¹⁾	V
V _{IL}	Input Low Voltage	-0.3 ⁽¹⁾	—	0.8	V

6818 tbl 05

- NOTE:
- Refer to maximum overshoot/undershoot diagram below. The measured voltage at device pin should not exceed half sinusoidal wave with 2V peak and half period of 2ns.

Maximum Overshoot/Undershoot



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DC Electrical Characteristics^(1,2)

(V_{DD} = Min. to Max., V_{LC} = 0.2V, V_{HC} = V_{DD} - 0.2V, Automotive Temperature Ranges)

Symbol	Parameter	71V016SA12			71V016SA15			71V016SA20			Unit	
		Automotive Grade			Automotive Grade			Automotive Grade				
		1	2	3 and 4	1	2	3 and 4	1	2	3 and 4		
I _{CC}	Dynamic Operating Current CS ≤ V _{LC} , Outputs Open, V _{DD} = Max., f = f _{MAX} ⁽³⁾	Max.	110	100	90	80	80	80	80	80	mA	
		Typ. ⁽⁴⁾	75	75	75	70	70	70	70	70		
I _{SB}	Dynamic Standby Power Supply Current CS ≥ V _{HC} , Outputs Open, V _{DD} = Max., f = f _{MAX} ⁽³⁾		45	45	35	35	35	30	30	30	30	mA
I _{SB1}	Full Standby Power Supply Current (static) CS ≥ V _{HC} , Outputs Open, V _{DD} = Max., f = 0 ⁽³⁾		5	5	2	5	5	2	5	5	2	mA

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NOTES:

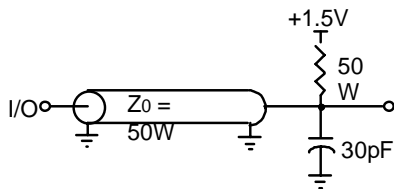
1. All values are maximum guaranteed values.
2. All inputs switch between 0.2V (Low) and V_{DD} - 0.2V (High).
3. f_{MAX} = 1/t_{RC} (all address inputs are cycling at f_{MAX}); f = 0 means no address input lines are changing.
4. Typical values are measured at 3.3V, 25°C and with equal read and write cycles. These parameter is guaranteed by device characterization but is not production tested.

AC Test Conditions

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	1.5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
AC Test Load	See Figure 1, 2 and 3

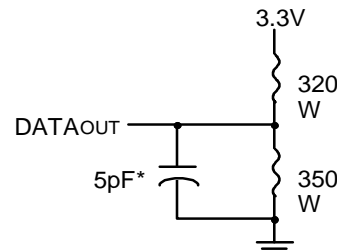
6818 tbl 09

AC Test Loads



6818 drw 03

Figure 1. AC Test Load



*Including jig and scope capacitance.

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Figure 2. AC Test Load
(for t_{CLZ}, t_{OLZ}, t_{CHZ}, t_{OHZ}, t_{OW}, and t_{WHZ})

Figure 3. Output Capacitive Derating

AC Electrical Characteristics (VDD = Min. to Max., Automotive Temperature Ranges)

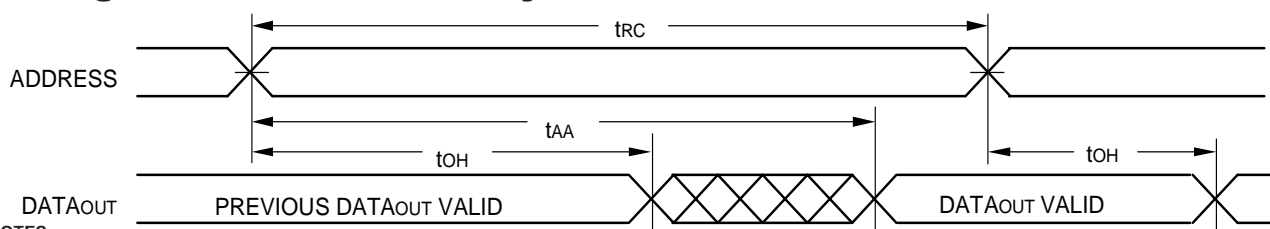
Symbol	Parameter	71V016SA12		71V016SA15		71V016SA20		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE								
t _{RC}	Read Cycle Time	12	—	15	—	20	—	ns
t _{AA}	Address Access Time	—	12	—	15	—	20	ns
t _{ACS}	Chip Select Access Time	—	12	—	15	—	20	ns
t _{CLZ} ^(1,2)	Chip Select Low to Output in Low-Z	4	—	5	—	5	—	ns
t _{CHZ} ^(1,2)	Chip Select High to Output in High-Z	—	6	—	6	—	8	ns
t _{OE}	Output Enable Low to Output Valid	—	6	—	6	—	8	ns
t _{OLZ} ^(1,2)	Output Enable Low to Output in Low-Z	1	—	1	—	1	—	ns
t _{OHZ} ^(1,2)	Output Enable High to Output in High-Z	—	6	—	6	—	8	ns
t _{OH}	Output Hold from Address Change	4	—	4	—	4	—	ns
t _{BE}	Byte Enable Low to Output Valid	—	6	—	6	—	8	ns
t _{BLZ} ^(1,2)	Byte Enable Low to Output in Low-Z	1	—	1	—	1	—	ns
t _{BHZ} ^(1,2)	Byte Enable High to Output in High-Z	—	6	—	6	—	8	ns
t _{PU} ⁽³⁾	Chip Select Low to Power Up	0	—	0	—	0	—	ns
t _{PD} ⁽³⁾	Chip Select High to Power Down	—	12	—	15	—	20	ns
WRITE CYCLE								
t _{WC}	Write Cycle Time	12	—	15	—	20	—	ns
t _{AW}	Address Valid to End of Write	8	—	10	—	12	—	ns
t _{CW}	Chip Select Low to End of Write	8	—	10	—	12	—	ns
t _{BW}	Byte Enable Low to End of Write	9	—	10	—	12	—	ns
t _{AS}	Address Set-up Time	0	—	0	—	0	—	ns
t _{WR}	Address Hold from End of Write	0	—	0	—	0	—	ns
t _{WP}	Write Pulse Width	8	—	10	—	12	—	ns
t _{DW}	Data Valid to End of Write	6	—	8	—	9	—	ns
t _{DH}	Data Hold Time	0	—	0	—	0	—	ns
t _{OW} ^(1,2)	Write Enable High to Output in Low-Z	3	—	3	—	3	—	ns
t _{WHZ} ^(1,2)	Write Enable Low to Output in High-Z	—	6	—	6	—	8	ns

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NOTES:

1. At any given temperature and voltage condition, t_{CHZ} is less than t_{CLZ}, t_{OHZ} is less than t_{OLZ}, and t_{WHZ} is less than t_{OW} for any given device.
2. This parameter is guaranteed with the AC Load (Figure 2) by device characterization, but is not production tested.
3. This parameter is guaranteed by design and not production tested.

Timing Waveform of Read Cycle No. 1^(1,2,3)

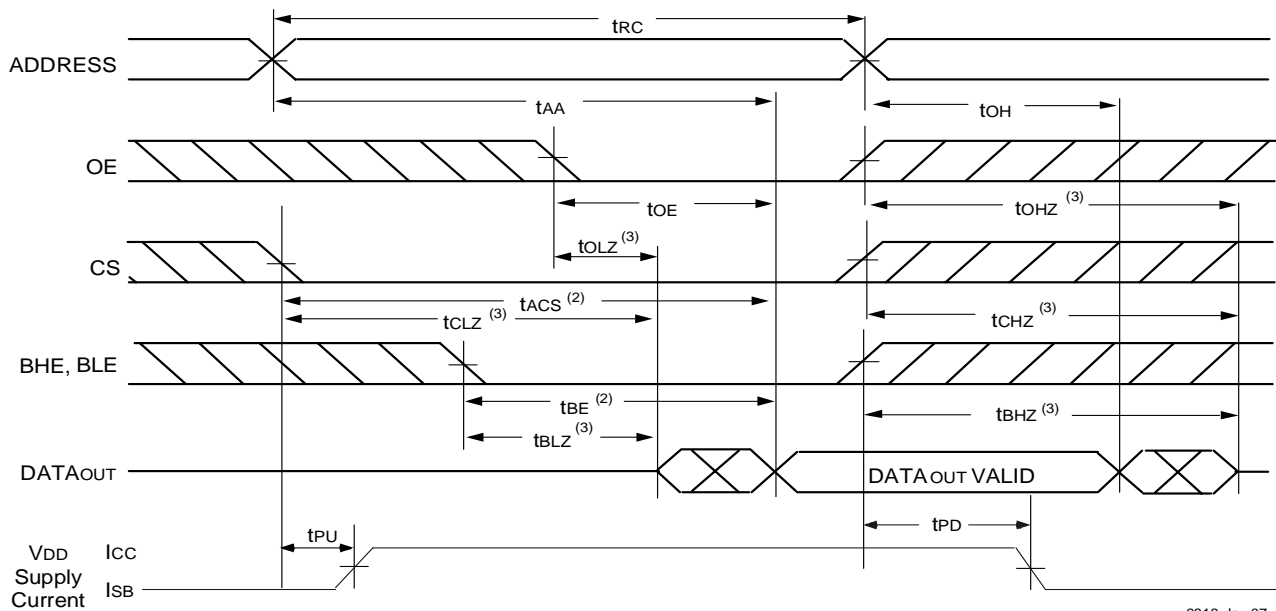


NOTES:

1. \overline{WE} is HIGH for Read Cycle.
2. Device is continuously selected, \overline{CS} is LOW.
3. \overline{OE} , \overline{BHE} , and \overline{BLE} are LOW.

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Timing Waveform of Read Cycle No. 2⁽¹⁾

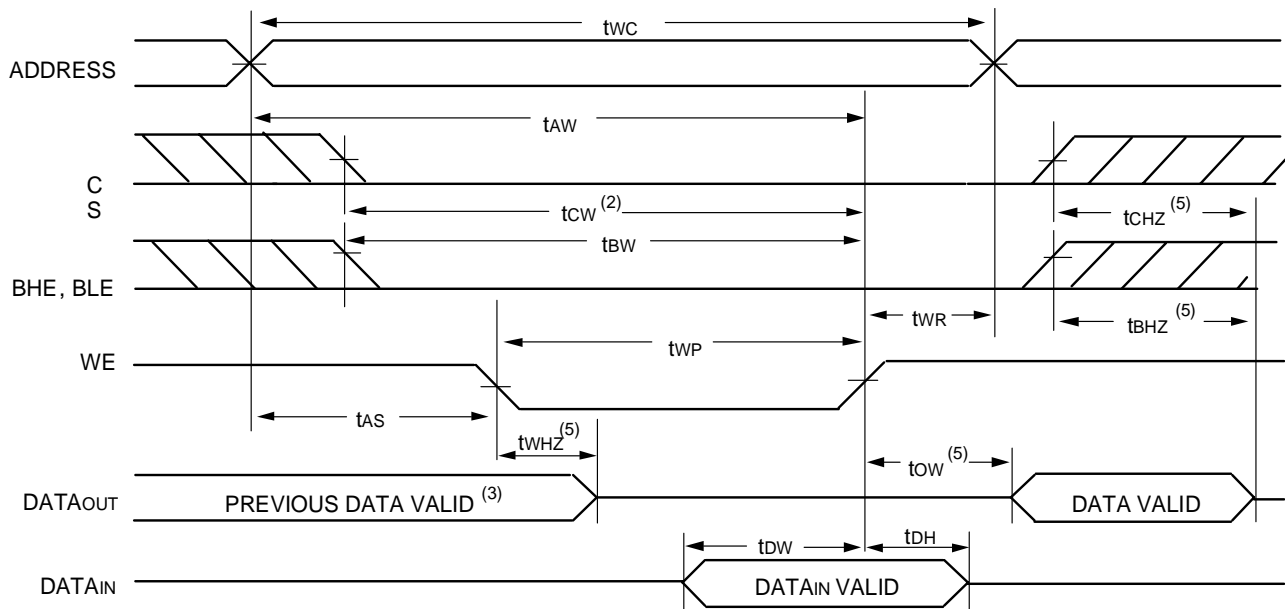


6818 drw 07

NOTES:

1. \overline{WE} is HIGH for Read Cycle.
2. Address must be valid prior to or coincident with the later of \overline{CS} , \overline{BHE} , or \overline{BLE} transition LOW; otherwise t_{AA} is the limiting parameter.
3. Transition is measured $\pm 200\text{mV}$ from steady state.

Timing Waveform of Write Cycle No. 1 (\overline{WE} Controlled Timing)^(1,2,4)

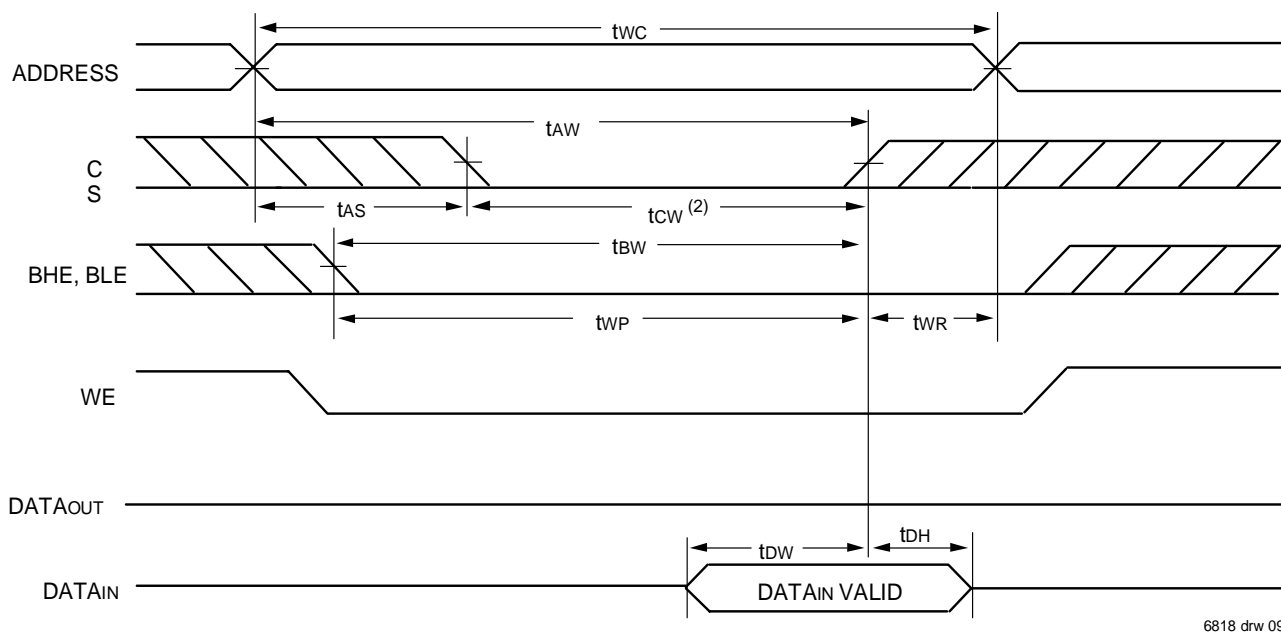


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NOTES:

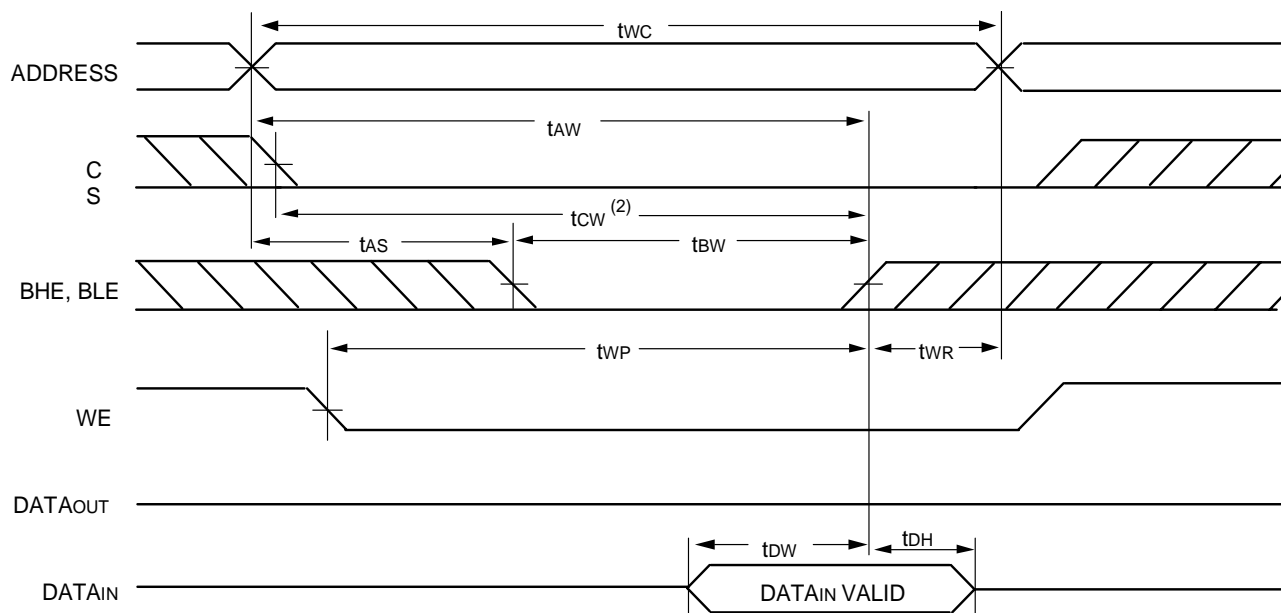
1. A write occurs during the overlap of a LOW \overline{CS} , LOW \overline{BHE} or \overline{BLE} , and a LOW \overline{WE} .
2. \overline{OE} is continuously HIGH. If during a \overline{WE} controlled write cycle \overline{OE} is LOW, t_{WP} must be greater than or equal to $t_{WHZ} + t_{OW}$ to allow the I/O drivers to turn off and data to be placed on the bus for the required t_{OW} . If \overline{OE} is HIGH during a \overline{WE} controlled write cycle, this requirement does not apply and the minimum write pulse is as short as the specified t_{WP} .
3. During this period, I/O pins are in the output state, and input signals must not be applied.
4. If the \overline{CS} LOW or \overline{BHE} and \overline{BLE} LOW transition occurs simultaneously with or after the \overline{WE} LOW transition, the outputs remain in a high-impedance state.
5. Transition is measured $\pm 200\text{mV}$ from steady state.

Timing Waveform of Write Cycle No. 2 (\overline{CS} Controlled Timing)^(1,4)



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Timing Waveform of Write Cycle No. 3 (\overline{BHE} , \overline{BLE} Controlled Timing)^(1,4)

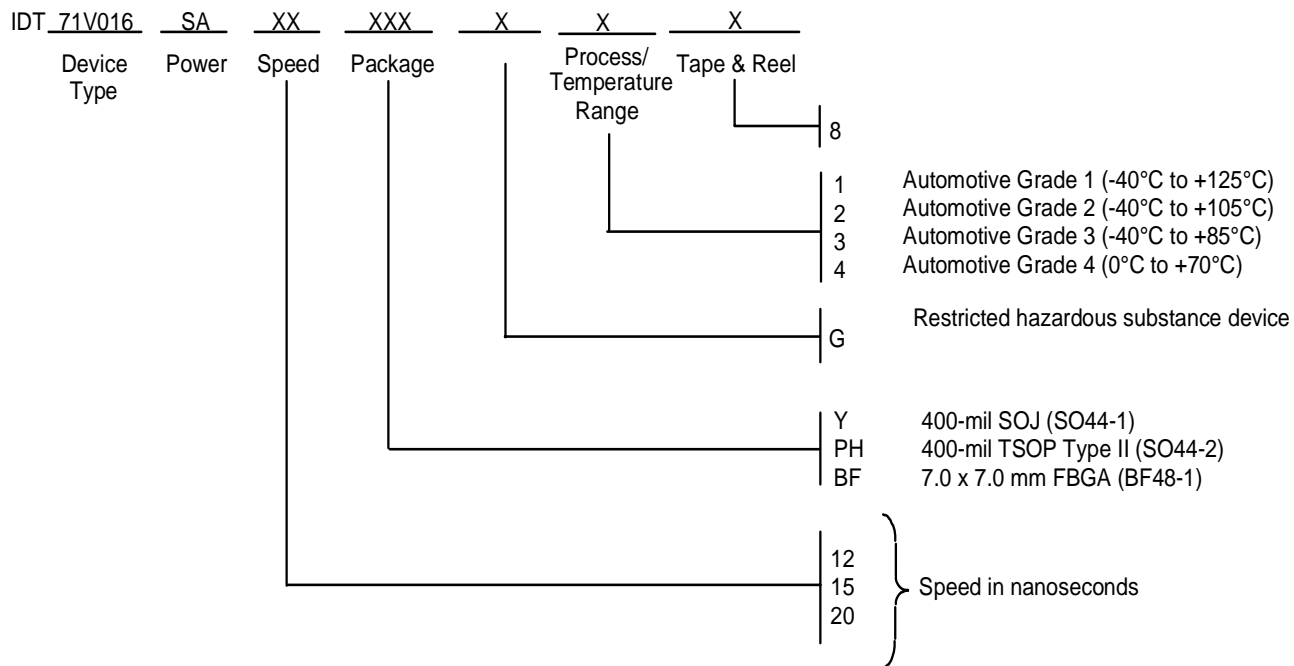


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NOTES:

1. A write occurs during the overlap of a LOW \overline{CS} , LOW \overline{BHE} or \overline{BLE} , and a LOW \overline{WE} .
2. \overline{OE} is continuously HIGH. If during a \overline{WE} controlled write cycle \overline{OE} is LOW, t_{WP} must be greater than or equal to $t_{WHZ} + t_{BW}$ to allow the I/O drivers to turn off and data to be placed on the bus for the required t_{BW} . If \overline{OE} is HIGH during a \overline{WE} controlled write cycle, this requirement does not apply and the minimum write pulse is as short as the specified t_{WP} .
3. During this period, I/O pins are in the output state, and input signals must not be applied.
4. If the \overline{CS} LOW or \overline{BHE} and \overline{BLE} LOW transition occurs simultaneously with or after the \overline{WE} LOW transition, the outputs remain in a high-impedance state.
5. Transition is measured $\pm 200\text{mV}$ from steady state.

Ordering Information



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Datasheet Document History

<u>Rev</u>	<u>Date</u>	<u>Page</u>	<u>Description</u>
0	12/17/04	p. 1-8	Released Automotive datasheet



CORPORATE HEADQUARTERS
6024 Silver Creek Valley Road
San Jose, CA 95138

for SALES:
800-345-7015 or
408-284-8200
fax: 408-284-2775
www.idt.com

for Tech Support:
ipchelp@idt.com
800-345-7015

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