

GD54/74LS74A

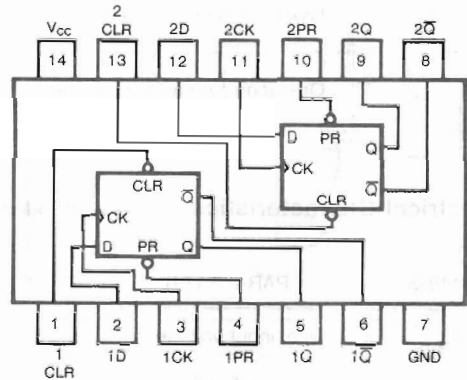
DUAL D-TYPE POSITIVE EDGE-TRIGGERED FLIP-FLOPS WITH PRESET AND CLEAR

Description

This device contains two independent D-type positive edge triggered flip-flops.

A low level at the preset or clear inputs sets or resets the outputs regardless of the levels of the other inputs. When preset and clear are inactive (high), data at the D input meeting the setup time requirements are transferred to the outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a voltage level and is not directly related to the rise time of the clock pulse. Following the hold time interval, data at the D input may be changed without affecting the levels at the outputs.

Pin Configuration



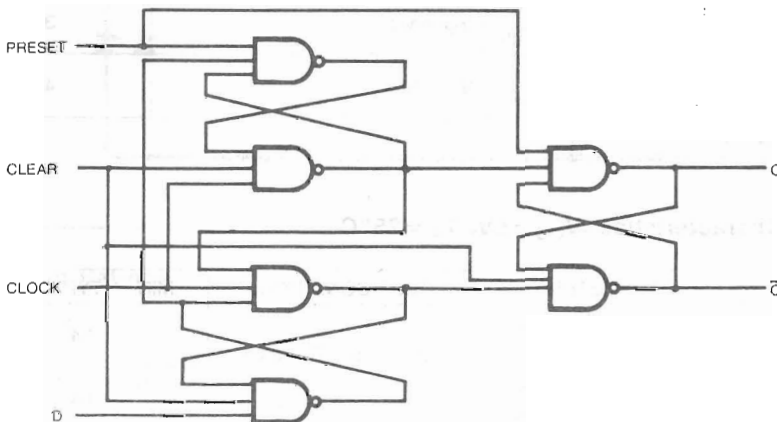
Suffix-Blank: Plastic Dual In Line Package
 Suffix-J : Ceramic Dual In Line Package

Function Table

- * The output levels in this configuration are not guaranteed to meet the minimum levels for V_{OH} if the lows at preset and clear are near V_{IL} maximum. Furthermore, this configuration is nonstable; that is it will not persist when either preset or clear returns to its inactive (high) level.

INPUTS				OUTPUTS	
PRESET	CLEAR	CLOCK	D	Q	\bar{Q}
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H*	H*
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q_0	\bar{Q}_0

Function Block Diagram

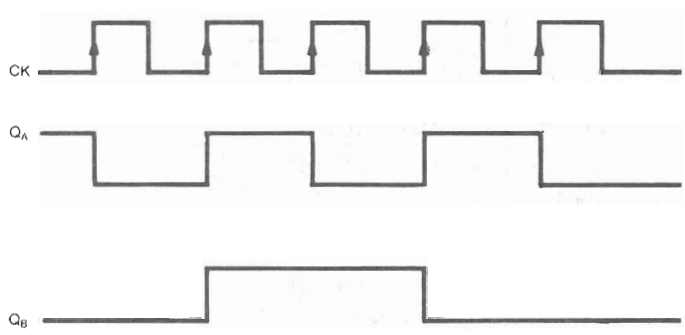
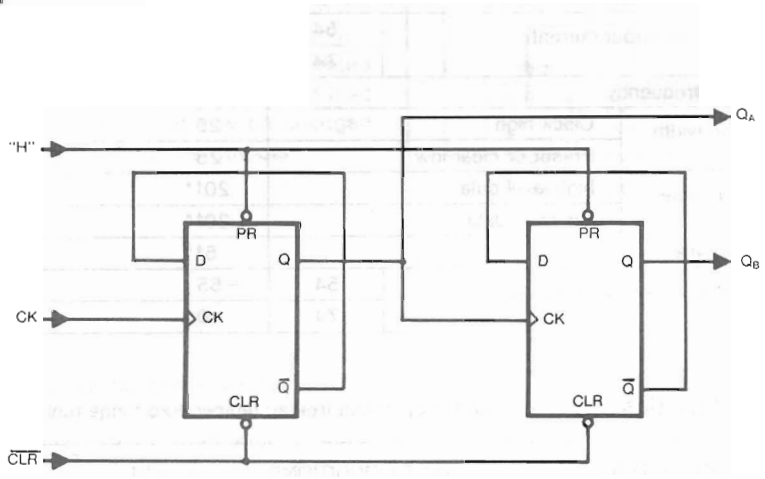


Switching Characteristics, $V_{CC} = 5V$, $T_A = 25^\circ C$

SYMBOL*	FROM (INPUT)	TO (OUTPUT)	TEST CONDITION#	MIN	TYP	MAX	UNIT
f_{max}			$C_L = 15pF$ $R_L = 2K\Omega$	25	33		MHz
t_{PLH}	Clear, preset or Clock (as appropriate)	Q or \bar{Q}			13	25	ns
t_{PHL}					25	40	

- * f_{max} = maximum clock frequency
- * t_{PLH} = propagation delay time, low-to-high-level output.
- * t_{PHL} = propagation delay time, high-to-low-level output.
- # For load circuit and voltage waveforms, see page 3-11.

Application Example
1/4 divider



For load circuit and voltage waveforms, see page 3-12.