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DESCRIPTION

The 80C552/83C552/87C552 (hereafter generically referred to as 8XC552) Single-Chip 8-Bit Microcontroller is manufactured in an advanced CMOS process and is a derivative of the 80C51 microcontroller family. The 8XC552 has the same instruction set as the 80C51. Three versions of the derivative exist:

- 83C552 — 8k bytes mask programmable ROM
- 80C552 — ROMless version of the 83C552
- 87C552 — 8k bytes EPROM

The 8XC552 contains a non-volatile 8k x 8 read-only program memory (83C552) EPROM (87C552), a volatile 256 x 8 read/write data memory, five 8-bit I/O ports, one 8-bit input port, two 16-bit timer/event counters (identical to the timers of the 80C51), an additional 16-bit timer coupled to capture and compare latches, a 15-source, two-priority-level, nested interrupt structure, an 8-input ADC, a dual DAC pulse width modulated interface, two serial interfaces (UART and I²C-bus), a "watchdog" timer and on-chip oscillator and timing circuits. For systems that require extra capability, the 8XC552 can be expanded using standard TTL compatible memories and logic.

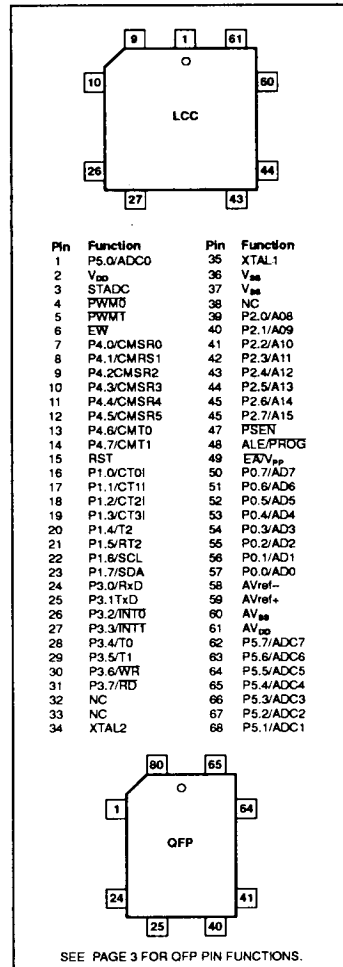
In addition, the 8XC552 has two software selectable modes of power reduction—idle mode and power-down mode. The idle mode freezes the CPU while allowing the RAM, timers, serial ports, and interrupt system to continue functioning. The power-down mode saves the RAM contents but freezes the oscillator, causing all other chip functions to be inoperative.

80C552/83C552/87C552

Single-chip 8-bit microcontroller with 10-bit A/D, capture/compare timer, high-speed outputs, PWM

FEATURES

- 80C51 central processing unit
- 8k x 8 ROM expandable externally to 64k bytes
- An additional 16-bit timer/counter coupled to four capture registers and three compare registers
- Two standard 16-bit timer/counters
- 256 x 8 RAM, expandable externally to 64k bytes
- Capable of producing 8 synchronized, timed outputs
- A 10-bit ADC with 8 multiplexed analog inputs
- Two 8-bit resolution, pulse width modulation outputs
- Five 8-bit I/O ports plus one 8-bit input port shared with analog inputs
- I²C-bus serial I/O port with byte oriented master and slave functions
- Full-duplex UART compatible with the standard 80C51
- On-chip watchdog timer
- Two speed ranges:
 - 12MHz
 - 16MHz
- Extended temperature ranges
- OTP package available

PIN CONFIGURATION

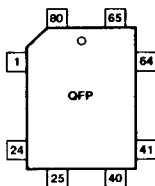
Single-chip 8-bit microcontroller**80C552/83C552/87C552****PART NUMBER SELECTION**

PHILIPS		PHILIPS COMPONENTS-SIGNETICS			TEMPERATURE °C AND PACKAGE	FREQ. MHz
ROMless	ROM	ROMless	ROM	EPROM		
				S87C552-1A68	0 to +70, PLCC 68	12
				S87C552-1K68	0 to +70, CLCC 68	12
				S87C552-1B80	0 to +70, PQFP 80	12
				S87C552-2A68	-40 to +85, PLCC 68	12
				S87C552-2K68	-40 to +85, CLCC 68	12
				S87C552-2B80	-40 to +85, PQFP 80	12
PCB80C552-4WP	PCB83C552-4WP	S80C552-1A68	S83C552-1A68	S87C552-4A68	0 to +70, PLCC 68	16
				S87C552-4K68	0 to +70, CLCC 68	16
PCB80C552-4H	PCB83C552-4H	S80C552-1B80	S83C552-1B80	S87C552-4B80	0 to +70, PQFP 80	16
PCF80C552-4WP	PCF83C552-4WP	S80C552-2A68	S83C552-2A68	S87C552-5A68	-40 to +85, PLCC 68	16
				S87C552-5K68	-40 to +85, CLCC 68	16
PCF80C552-4H	PCF83C552-4H	S80C552-2B80	S83C552-2B80	S87C552-5B80	-40 to +85, PQFP 80	16
PCA80C552-4WP	PCA83C552-4WP	S80C552-6A68	S83C552-6A68		-40 to +125, PLCC 68	16
PCA80C552-4H	PCA83C552-4H	S80C552-6B80	S83C552-6B80		-40 to +125, PQFP 80	16

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QFP PIN FUNCTIONS



Pin	Function	Pin	Function
1	P4.1/CMSR1	41	P2.3/A11
2	P4.2/CMSR2	42	P2.4/A12
3	NC	43	NC
4	P4.3/CMSR3	44	NC
5	P4.4/CMSR4	45	P2.5/A13
6	P4.5/CMSR5	46	P2.6/A14
7	P4.6/CMT0	47	P2.7/A15
8	P4.7/CMT1	48	PSEN
9	RST	49	ALE
10	P1.0/CT01	50	EA
11	P1.1/CT11	51	P0.7/AD7
12	P1.2/CT21	52	P0.6/AD6
13	P1.3/CT31	53	P0.5/AD5
14	P1.4/T2	54	P0.4/AD4
15	P1.5/RT2	55	P0.3/AD3
16	P1.6/SCL	56	P0.2/AD2
17	P1.7/SDA	57	P0.1/AD1
18	P3.0/RXD	58	P0.0/AD0
19	P3.1/TXD	59	AVref-
20	P3.2/INT0	60	AVref+
21	NC	61	AV _{ss}
22	NC	62	NC
23	P3.3/INTT	63	AV _{DD}
24	P3.4/T0	64	P5.7/ADC7
25	P3.5/T1	65	P5.6/ADC6
26	P3.6/WR	66	P5.5/ADC5
27	P3.7/RD	67	P5.4/ADC4
28	NC	68	P5.3/ADC3
29	NC	69	P5.2/ADC2
30	NC	70	P5.1/ADC1
31	XTAL2	71	P5.0/ADC0
32	XTAL1	72	V _{DD}
33	IC	73	IC
34	V _{ss}	74	STADC
35	V _{ss}	75	PWM0
36	V _{ss}	76	PWM1
37	NC	77	EW
38	P2.0/A08	78	NC
39	P2.1/A09	79	NC
40	P2.2/A10	80	P4.0/CMSR0

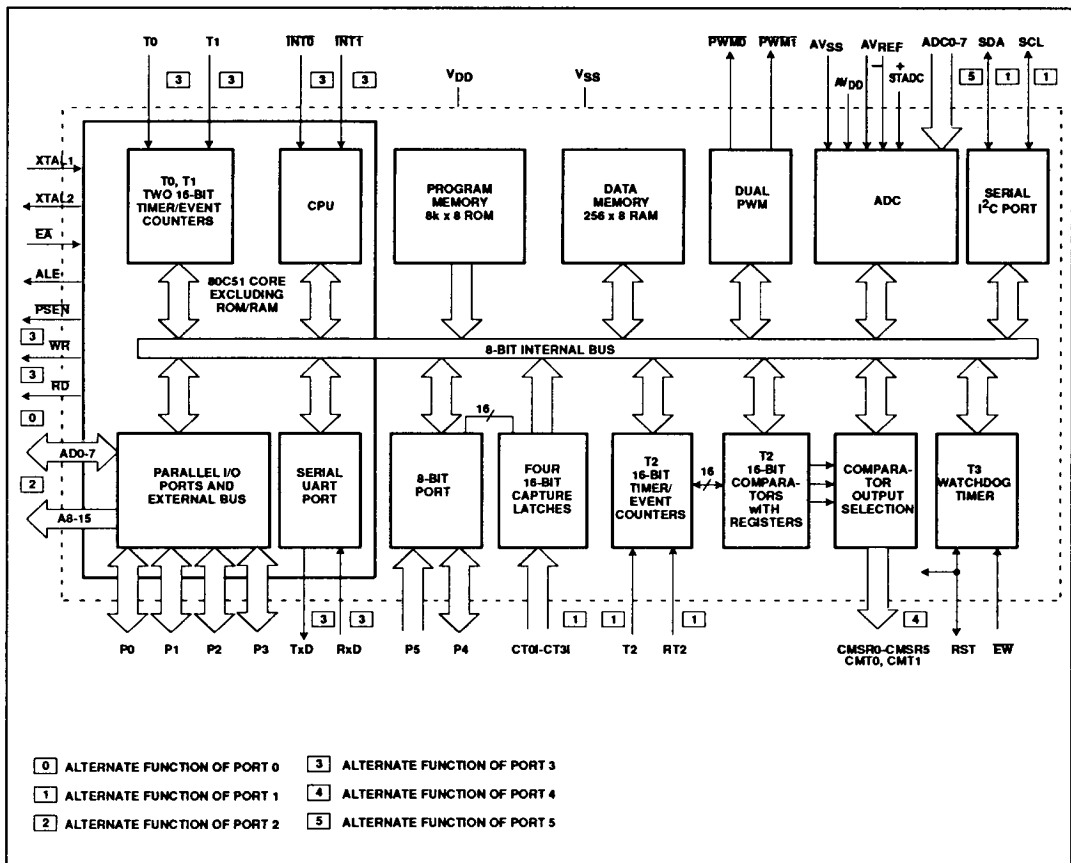
NC = not connected

IC = internally connected (do not use)

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BLOCK DIAGRAM



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PIN DESCRIPTION

MNEMONIC	PIN NO.		TYPE	NAME AND FUNCTION
	PLCC	QFP		
V _{DD}	2	72	I	Digital Power Supply: +5V power supply pin during normal operation, idle and power-down mode.
STADC	3	74	I	Start ADC Operation: Input starting analog to digital conversion (ADC operation can also be started by software).
PWM0	4	75	O	Pulse Width Modulation: Output 0.
PWM1	5	76	O	Pulse Width Modulation: Output 1.
EW	6	77	I	Enable Watchdog Timer: Enable for T3 watchdog timer and disable power-down mode.
P0.0-P0.7	57-50	58-51	I/O	Port 0: Port 0 is an 8-bit open-drain bidirectional I/O port. Port 0 pins that have 1s written to them float and can be used as high-impedance inputs. Port 0 is also the multiplexed low-order address and data bus during accesses to external program and data memory. In this application it uses strong internal pull-ups when emitting 1s. Port 0 is also used to input the code byte during programming and to output the code byte during verification.
P1.0-P1.7	16-23	10-17	I/O	Port 1: 8-bit I/O port. Alternate functions include:
	16-21	10-15	I/O	(P1.0-P1.5): Quasi-bidirectional port pins.
	22-23	16-17	I/O	(P1.6, P1.7): Open drain port pins.
	16-19	10-13	I	CT0I-CT3I (P1.0-P1.3): Capture timer input signals for timer T2.
	20	14	I	T2 (P1.4): T2 event input
	21	15	I	RT2 (P1.5): T2 timer reset signal. Rising edge triggered.
	22	16	I/O	SCL (P1.6): Serial port clock line I ² C-bus.
	23	17	I/O	SDA (P1.7): Serial port data line I ² C-bus.
P2.0-P2.7	39-46	38-42, 45-47	I/O	Port 2: 8-bit quasi-bidirectional I/O port. Alternate function: High-order address byte for external memory (A08-A15). Port 2 is also used to input the upper order address during EPROM programming and verification. A8 is on P2.0, A9 on P2.1, through A12 on P2.4.
P3.0-P3.7	24-31	18-20, 23-27	I/O	Port 3: 8-bit quasi-bidirectional I/O port. Alternate functions include:
	24	18		RxD (P3.0): Serial input port.
	25	19		TxD (P3.1): Serial output port.
	26	20		INT0 (P3.2): External interrupt.
	27	23		INTT (P3.3): External interrupt.
	28	24		T0 (P3.4): Timer 0 external input.
	29	25		T1 (P3.5): Timer 1 external input.
	30	26		WR (P3.6): External data memory write strobe.
	31	27		RD (P3.7): External data memory read strobe.
P4.0-P4.7	7-14	80, 1-2, 4-8	I/O	Port 4: 8-bit quasi-bidirectional I/O port. Alternate functions include:
	7-12	80, 1-2, 4-6	O	CMSR0-CMSR5 (P4.0-P4.5): Timer T2 compare and set/reset outputs on a match with timer T2.
	13, 14	7, 8	O	CMT0, CMT1 (P4.6, P4.7): Timer T2 compare and toggle outputs on a match with timer T2.
P5.0-P5.7	68-62, 1	71-64,	I	Port 5: 8-bit input port. ADC0-ADC7 (P5.0-P5.7): Alternate function: Eight input channels to ADC.
RST	15	9	I/O	Reset: Input to reset the 87C552. It also provides a reset pulse as output when timer T3 overflows.
XTAL1	35	32	I	Crystal Input 1: Input to the inverting amplifier that forms the oscillator, and input to the internal clock generator. Receives the external clock signal when an external oscillator is used.
XTAL2	34	31	O	Crystal Input 2: Output of the inverting amplifier that forms the oscillator. Left open-circuit when an external clock is used.

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PIN DESCRIPTION (Continued)

MNEMONIC	PIN NO.		TYPE	NAME AND FUNCTION
	PLCC	QFP		
V _{SS}	36, 37	34-36	I	Digital ground.
PSEN	47	48	O	Program Store Enable: Active-low read strobe to external program memory.
ALE/PROG	48	49	O	Address Latch Enable: Latches the low byte of the address during accesses to external memory. It is activated every six oscillator periods. During an external data memory access, one ALE pulse is skipped. ALE can drive up to eight LS TTL inputs and handles CMOS inputs without an external pull-up. This pin is also the program pulse input (PROG) during EPROM programming.
EA/V _{PP}	49	50	I	External Access: When EA is held at TTL level high, the CPU executes out of the internal program ROM provided the program counter is less than 8192. When EA is held at TTL low level, the CPU executes out of external program memory. EA is not allowed to float. This pin also receives the 12.75V programming supply voltage (V _{PP}) during EPROM programming.
AV _{REF-}	58	59	I	Analog to Digital Conversion Reference Resistor: Low-end.
AV _{REF+}	59	60	I	Analog to Digital Conversion Reference Resistor: High-end.
AV _{SS}	60	61	I	Analog Ground
AV _{DD}	61	63	I	Analog Power Supply

NOTE:

1. To avoid "latch-up" effect at power-on, the voltage on any pin at any time must not be higher or lower than V_{DD} + 0.5V or V_{SS} - 0.5V, respectively.

OSCILLATOR CHARACTERISTICS

XTAL1 and XTAL2 are the input and output, respectively, of an inverting amplifier. The pins can be configured for use as an on-chip oscillator, as shown in the logic symbol, page 1.

To drive the device from an external clock source, XTAL1 should be driven while XTAL2 is left unconnected. There are no requirements on the duty cycle of the external clock signal, because the input to the internal clock circuitry is through a divide-by-two flip-flop. However, minimum and maximum high and low times specified in the data sheet must be observed.

RESET

A reset is accomplished by holding the RST

pin high for at least two machine cycles (24 oscillator periods), while the oscillator is running. To insure a good power-on reset, the RST pin must be high long enough to allow the oscillator time to start up (normally a few milliseconds) plus two machine cycles. At power-on, the voltage on V_{DD} and RST must come up at the same time for a proper start-up.

IDLE MODE

In the idle mode, the CPU puts itself to sleep while all of the on-chip peripherals stay active. The instruction to invoke the idle mode is the last instruction executed in the normal operating mode before the idle mode is activated. The CPU contents, the on-chip RAM, and all of the special function registers remain intact during this mode. The idle mode

can be terminated either by any enabled interrupt (at which time the process is picked up at the interrupt service routine and continued), or by a hardware reset which starts the processor in the same manner as a power-on reset.

POWER-DOWN MODE

In the power-down mode, the oscillator is stopped and the instruction to invoke power-down is the last instruction executed. Only the contents of the on-chip RAM are preserved. A hardware reset is the only way to terminate the power-down mode. The control bits for the reduced power modes are in the special function register PCON. Table 1 shows the state of the I/O ports during low current operating modes.

Table 1. External Pin Status During Idle and Power-Down Modes

MODE	PROGRAM MEMORY	ALE	PSEN	PORT 0	PORT 1	PORT 2	PORT 3	PORT 4	PWM0/PWM1
Idle	Internal	1	1	Data	Data	Data	Data	Data	High
Idle	External	1	1	Float	Data	Address	Data	Data	High
Power-down	Internal	0	0	Data	Data	Data	Data	Data	High
Power-down	External	0	0	Float	Data	Data	Data	Data	High

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Serial Control Register (S1CON) – See Table 2

S1CON (DeH)	CR2	ENS1	STA	STO	SI	AA	CR1	CR0
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Bits CR0, CR1 and CR2 determine the serial clock frequency that is generated in the master mode of operation.

Table 2. Serial Clock Rates

CR2	CR1	CR0	BIT FREQUENCY (kHz) AT f_{osc}			f_{osc} DIVIDED BY
			6MHz	12MHz	16MHz	
0	0	0	23	47	62.5	256
0	0	1	27	54	71	224
0	1	0	31.25	62.5	83.3	192
0	1	1	37	75	100	160
1	0	0	6.25	12.5	17	960
1	0	1	50	100	133 ¹	120
1	1	0	100	200 ¹	267 ¹	60
1	1	1	0.25 < 31.25	0.5 < 62.5	0.67 < 83.3	96 x (256 – (reload value Timer 1)) (Reload value range: 0 – 254 in mode 2)

NOTE:

1. These frequencies exceed the upper limit of 100kHz of the I²C-bus specification and cannot be used in an I²C-bus application.

ABSOLUTE MAXIMUM RATINGS^{1, 2, 3}

PARAMETER	RATING	UNIT
Storage temperature range	–65 to +150	°C
Voltage on EA/V _{PP} to V _{SS} (87C552 only)	–0.5 to +13	V
Voltage on any other pin to V _{SS}	–0.5 to +6.5	V
Input, output DC current on any single I/O pin	5.0	mA
Power dissipation (based on package heat transfer limitations, not device power consumption)	1.0	W

NOTES:

- Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any conditions other than those described in the AC and DC Electrical Characteristics section of this specification is not implied.
- This product includes circuitry specifically designed for the protection of its internal devices from the damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying greater than the rated maxima.
- Parameters are valid over operating temperature range unless otherwise specified. All voltages are with respect to V_{SS} unless otherwise noted.

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DC ELECTRICAL CHARACTERISTICS

 $V_{SS}, AV_{SS} = 0V$

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS		UNIT
			MIN	MAX	
V_{DD}	Supply voltage PCB8XC552 PCF8XC552 PCA8XC552 87C552		4.0 4.0 4.5 4.5	6.0 6.0 5.5 5.5	V V V V
I_{DD}	Supply current operating: PCB8XC552 PCF8XC552 PCA8XC552 87C552	See notes 1 and 2 $f_{osc} = 16MHz$ $f_{osc} = 16MHz$ $f_{osc} = 16MHz$ $f_{osc} = 12MHz$		45 45 40 30	mA mA mA mA
I_{ID}	Idle mode: PCB8XC552 PCF8XC552 PCA8XC552 87C552	See notes 1 and 3 $f_{osc} = 16MHz$ $f_{osc} = 16MHz$ $f_{osc} = 16MHz$ $f_{osc} = 12MHz$		10 10 9 7	mA mA mA mA
I_{PD}	Power-down current: PCB8XC552 PCF8XC552 PCA8XC552 87C552	See notes 1 and 4; $2V < V_{PD} < V_{DD} \text{ max}$		50 50 150 50	μA μA μA μA
Inputs					
V_{IL}	Input low voltage, except $E\bar{A}$, P1.6, P1.7		-0.5	$0.2V_{DD}-0.1$	V
V_{IL1}	Input low voltage to $E\bar{A}$		-0.5	$0.2V_{DD}-0.3$	V
V_{IL2}	Input low voltage to P1.6/SCL, P1.7/SDA ⁵		-0.5	$0.3V_{DD}$	V
V_{IH}	Input high voltage, except XTAL1, RST		$0.2V_{DD}+0.9$	$V_{DD}+0.5$	V
V_{IH1}	Input high voltage, XTAL1, RST		$0.7V_{DD}$	$V_{DD}+0.5$	V
V_{IH2}	Input high voltage, P1.6/SCL, P1.7/SDA ⁵		$0.7V_{DD}$	6.0	V
$-I_{IL}$	Logical 0 input current, ports 1, 2, 3, 4, except P1.6, P1.7	$V_{IN} = 0.45V$		-50	μA
$-I_{TL}$	Logical 1-to-0 transition current, ports 1, 2, 3, 4, except P1.6, P1.7	See note 6		-650	μA
$\pm I_{IL1}$	Input leakage current, port 0, $E\bar{A}$, STADC, EW	$0.45V < V_i < V_{DD}$		10	μA
$\pm I_{IL2}$	Input leakage current, P1.6/SCL, P1.7/SDA	$0V < V_i < 6V$ $0V < V_{DD} < 5.5V$		10	μA
Outputs					
V_{OL}	Output low voltage, ports 1, 2, 3, 4, except P1.6, P1.7	$I_{OL} = 1.6mA^7$		0.45	V
V_{OL1}	Output low voltage, port 0, ALE, $PSEN$, $PWM0$, $PWM1$	$I_{OL} = 3.2mA^7$		0.45	V
V_{OL2}	Output low voltage, P1.6/SCL, P1.7/SDA	$I_{OL} = 3.0mA^7$		0.4	V
V_{OH}	Output high voltage, ports 1, 2, 3, 4, except P1.6/SCL, P1.7/SDA	$-I_{OH} = 60\mu A$ $-I_{OH} = 25\mu A$ $-I_{OH} = 10\mu A$	2.4 $0.75V_{DD}$ $0.9V_{DD}$		V V V V
V_{OH1}	Output high voltage (port 0 in external bus mode, ALE, $PSEN$, $PWM0$, $PWM1$) ⁸	$-I_{OH} = 400\mu A$ $-I_{OH} = 150\mu A$ $-I_{OH} = 40\mu A$	2.4 $0.75V_{DD}$ $0.9V_{DD}$		V V V V
V_{OH2}	High level output voltage (RST)	$-I_{OH} = 400\mu A$ $-I_{OH} = 120\mu A$	2.4 $0.8V_{DD}$		V V

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DC ELECTRICAL CHARACTERISTICS (Continued)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS		UNIT
			MIN	MAX	
Outputs (Continued)					
R _{RST}	Internal reset pull-down resistor		50	150	kohm
C _{IO}	Pin capacitance	Test freq = 1MHz, T _A = 25°C		10	pF
Analog Inputs					
AV _{DD}	Analog supply voltage: PCB8XC552 PCF8XC552 PCA8XC552 87C552 ⁹	AV _{DD} = V _{DD} ±0.2V AV _{DD} = V _{DD} ±0.2V AV _{DD} = V _{DD} ±0.2V AV _{DD} = V _{DD} ±0.2V	4.0 4.0 4.5 4.5	6.0 6.0 5.5 5.5	V V V V
AI _{DD}	Analog supply current: operating:	Port 5 = 0 to AV _{DD}		1.2	mA
AI _{ID}	Idle mode: PCB8XC552 PCF8XC552 PCA8XC552 87C552			50 50 100 50	μA μA μA μA
AI _{PD}	Power-down mode: PCB8XC552 PCF8XC552 PCA8XC552 87C552	2V < AV _{PD} < AV _{DD} max		50 50 100 50	μA μA μA μA
AV _{IN}	Analog input voltage		AV _{SS} -0.2	AV _{DD} +0.2	V
AV _{REF}	Reference voltage: AV _{REF-} AV _{REF+}		AV _{SS} -0.2	AV _{DD} +0.2	V V
R _{REF}	Resistance between AV _{REF+} and AV _{REF-}		10	50	kohms
C _{IA}	Analog input capacitance			15	pF
t _{ADS}	Sampling time			8t _{CY}	μs
t _{ADC}	Conversion time (including sampling time)			50t _{CY}	μs
DL _e	Differential non-linearity ^{10, 11, 12}			±1	LSB
IL _e	Integral non-linearity ^{10, 13}			±2	LSB
OS _e	Offset error ^{10, 14}			±2	LSB
G _e	Gain error ^{10, 15}			±0.4	%
A _e	Absolute voltage error ^{10, 16}			±3	LSB
M _{CTC}	Channel to channel matching			±1	LSB
C ₁	Crosstalk between inputs of port 5 ¹⁷	0-100kHz		-60	dB

NOTES: See Next Page.

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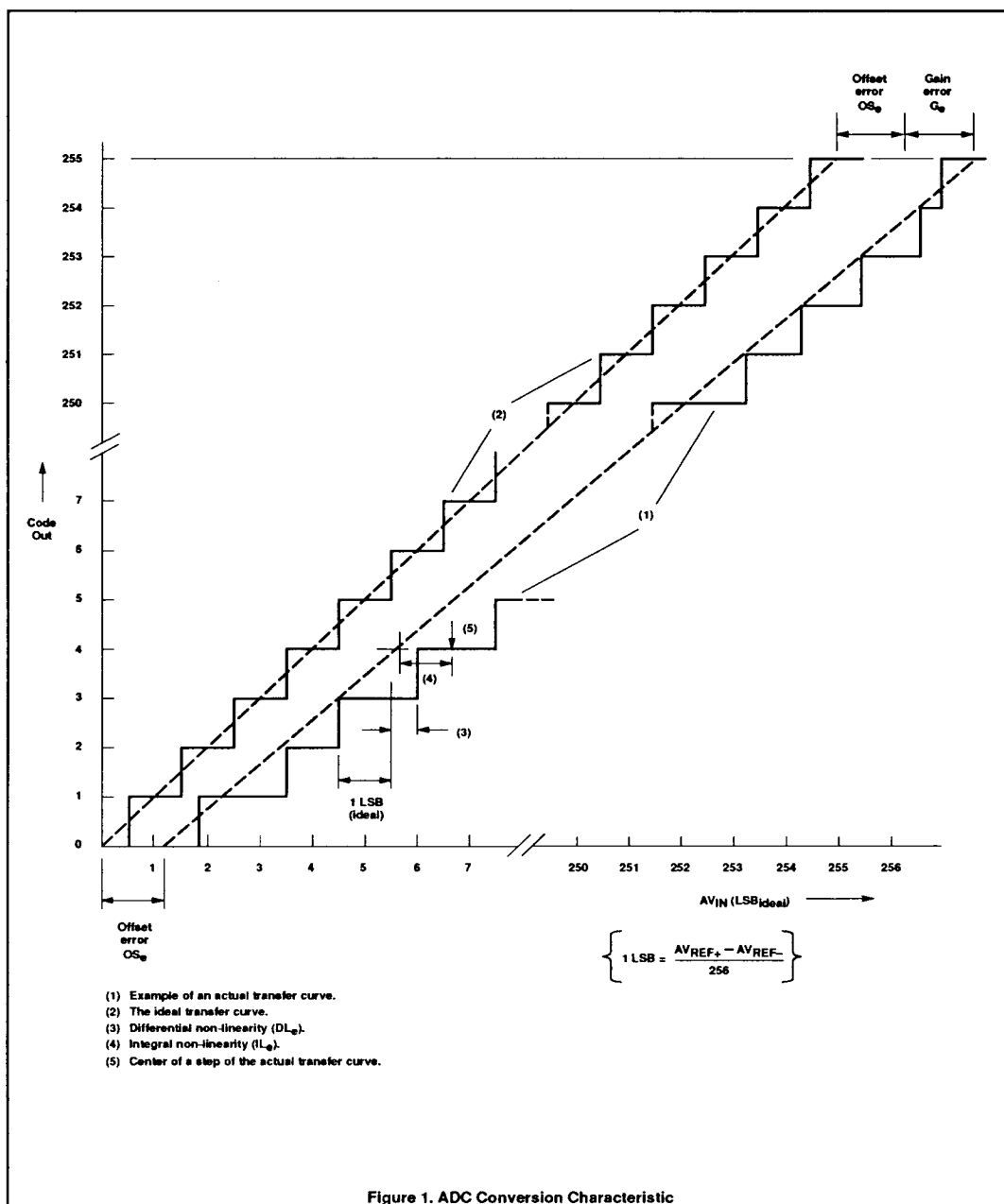
80C552/83C552/87C552

NOTES FOR DC ELECTRICAL CHARACTERISTICS:

1. See Figures 8 through 12 for I_{DD} test conditions.
2. The operating supply current is measured with all output pins disconnected; XTAL1 driven with $t_r = t_f = 10\text{ns}$; $V_{IL} = V_{SS} + 0.5\text{V}$; $V_{IH} = V_{DD} - 0.5\text{V}$; XTAL2 not connected; $\overline{EA} = \text{RST} = \text{Port } 0 = \overline{EW} = V_{DD}$; STADC = V_{SS} .
3. The idle mode supply current is measured with all output pins disconnected; XTAL1 driven with $t_r = t_f = 10\text{ns}$; $V_{IL} = V_{SS} + 0.5\text{V}$; $V_{IH} = V_{DD} - 0.5\text{V}$; XTAL2 not connected; $\overline{EA} = \text{Port } 0 = \overline{EW} = V_{DD}$; RST = STADC = V_{SS} .
4. The power-down current is measured with all output pins disconnected; XTAL2 not connected; $\overline{EA} = \text{Port } 0 = \overline{EW} = V_{DD}$; RST = STADC = XTAL1 = V_{SS} .
5. The input threshold voltage of P1.6 and P1.7 (SIO1) meets the I2C specification, so an input voltage below 1.5V will be recognized as a logic 0 while an input voltage above 3.0V will be recognized as a logic 1.
6. Pins of ports 1 (except P1.6, P1.7), 2, 3, and 4 source a transition current when they are being externally driven from 1 to 0. The transition current reaches its maximum value when V_{IN} is approximately 2V.
7. Capacitive loading on ports 0 and 2 may cause spurious noise to be superimposed on the V_{OL} s of ALE and ports 1 and 3. The noise is due to external bus capacitance discharging into the port 0 and port 2 pins when these pins make 1-to-0 transitions during bus operations. In the worst cases (capacitive loading > 100pF), the noise pulse on the ALE pin may exceed 0.8V. In such cases, it may be desirable to qualify ALE with a Schmitt Trigger, or use an address latch with a Schmitt Trigger STROBE input. I_{OL} can exceed these conditions provided that no single output sinks more than 5mA and no more than two outputs exceed the test conditions.
8. Capacitive loading on ports 0 and 2 may cause the V_{OH} on ALE and PSEN to momentarily fall below the $0.9V_{DD}$ specification when the address bits are stabilizing.
9. The following condition must not be exceeded: $V_{DD} - 0.2\text{V} < AV_{DD} < V_{DD} + 0.2\text{V}$.
10. Conditions: $AV_{REF-} = 0\text{V}$; $AV_{DD} = 5.0\text{V}$; $AV_{REF+} = 4.977\text{V}$. ADC is monotonic with no missing codes.
11. The differential non-linearity (DL_n) is the difference between the actual step width and the ideal step width. (See Figure 1.)
12. The ADC is monotonic; there are no missing codes.
13. The integral non-linearity (IL_n) is the peak difference between the center of the steps of the actual and the ideal transfer curve after appropriate adjustment of gain and offset error. (See Figure 1.)
14. The offset error (OS_n) is the absolute difference between the straight line which fits the actual transfer curve (after removing gain error), and a straight line which fits the ideal transfer curve. (See Figure 1.)
15. The gain error (G_n) is the relative difference in percent between the straight line fitting the actual transfer curve (after removing offset error), and the straight line which fits the ideal transfer curve. Gain error is constant at every point on the transfer curve. (See Figure 1.)
16. The absolute voltage error (A_n) is the maximum difference between the center of the steps of the actual transfer curve of the non-calibrated ADC and the ideal transfer curve.
17. This should be considered when both analog and digital signals are simultaneously input to port 5.

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AC ELECTRICAL CHARACTERISTICS^{1, 2}

SYMBOL	FIGURE	PARAMETER	12MHz CLOCK		VARIABLE CLOCK		UNIT
			MIN	MAX	MIN	MAX	
1/t _{CLCL}	2	Oscillator frequency ³			1.2	16	MHz
t _{LHLL}	2	ALE pulse width	127		2t _{CLCL} -40		ns
t _{AVLL}	2	Address valid to ALE low	28		t _{CLCL} -55		ns
t _{LLAX}	2	Address hold after ALE low	48		t _{CLCL} -35		ns
t _{LLIV}	2	ALE low to valid instruction in		234		4t _{CLCL} -100	ns
t _{LLPL}	2	ALE low to PSEN low	43		t _{CLCL} -40		ns
t _{PLPH}	2	PSEN pulse width	205		3t _{CLCL} -45		ns
t _{PLIV}	2	PSEN low to valid instruction in		145		3t _{CLCL} -105	ns
t _{PXIX}	2	Input instruction hold after PSEN	0		0		ns
t _{PXIZ}	2	Input instruction float after PSEN		59		t _{CLCL} -25	ns
t _{AVIV}	2	Address to valid instruction in		312		5t _{CLCL} -105	ns
t _{PLAZ}	2	PSEN low to address float		10		10	ns
Data Memory							
t _{AVLL}	3, 4	Address valid to ALE low	43		t _{CLCL} -40		ns
t _{RLRH}	3	RD pulse width	400		6t _{CLCL} -100		ns
t _{WLWH}	4	WR pulse width	400		6t _{CLCL} -100		ns
t _{RLDV}	3	RD low to valid data in		252		5t _{CLCL} -165	ns
t _{RHDX}	3	Data hold after RD	0		0		ns
t _{RHDZ}	3	Data float after RD		97		2t _{CLCL} -70	ns
t _{LLDV}	3	ALE low to valid data in		517		8t _{CLCL} -150	ns
t _{AVDV}	3	Address to valid data in		585		9t _{CLCL} -165	ns
t _{LLWL}	3, 4	ALE low to RD or WR low	200	300	3t _{CLCL} -50	3t _{CLCL} +50	ns
t _{AVWL}	3, 4	Address valid to WR low or RD low	203		4t _{CLCL} -130		ns
t _{QVWX}	4	Data valid to WR transition	23		t _{CLCL} -60		ns
t _{DW}	4	Data before WR	433		7t _{CLCL} -150		ns
t _{WHQX}	4	Data hold after WR	33		t _{CLCL} -50		ns
t _{RLAZ}	3	RD low to address float		0		0	ns
t _{WLHL}	3, 4	RD or WR high to ALE high	43	123	t _{CLCL} -40	t _{CLCL} +40	ns
External Clock							
t _{CHCX}	5	High time ⁴	20		20		ns
t _{CLCX}	5	Low time ⁴	20		20		ns
t _{CLCH}	5	Rise time ⁴		20		20	ns
t _{CHCL}	5	Fall time ⁴		20		20	ns

NOTES:

- Parameters are valid over operating temperature range unless otherwise specified.
- Load capacitance for port 0, ALE, and PSEN = 100pF, load capacitance for all other outputs = 80pF.
- 87C552: 1/t_{CLCL} = 3.5 to 16 MHz.
- These values are characterized but not 100% production tested.

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EXPLANATION OF THE AC SYMBOLS

Each timing symbol has five characters. The first character is always 't' (= time). The other characters, depending on their positions, indicate the name of a signal or the logical status of that signal. The designations are:

A – Address

C - Clock

D – Input data

H – Logic level high

I – Instruction (program memory contents)

L – Logic level low, or ALE

P - PSEN

Q – Output data

R – RD signal

t - Time

V – Valid

W – WR signal

X – No longer a valid logic level

Z - Float

Examples: t_{AVL} = Time for address valid to ALE low.

t_{LLPL} = Time for ALE low to **PSEN** low.

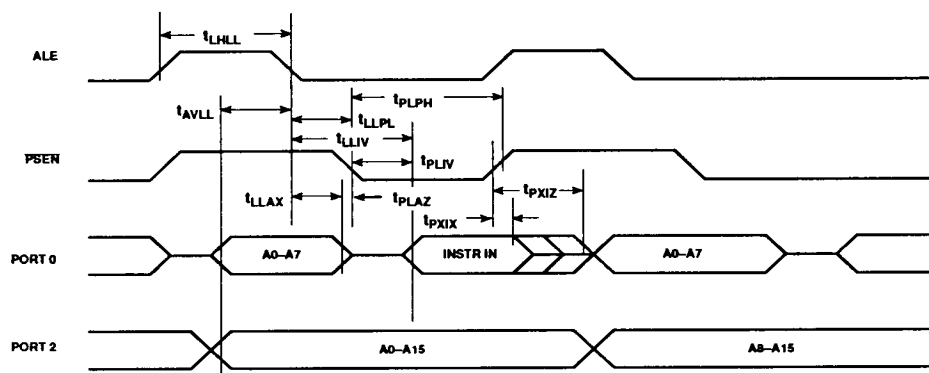


Figure 2. External Program Memory Read Cycle

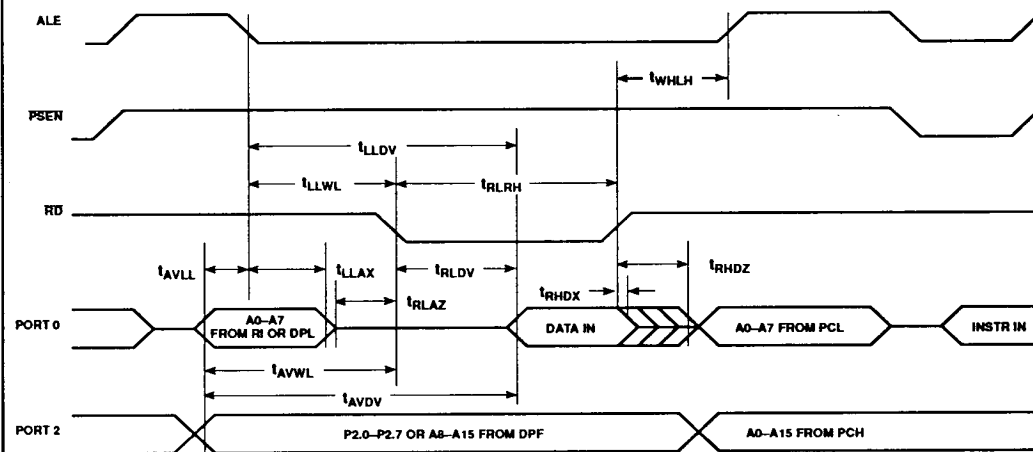
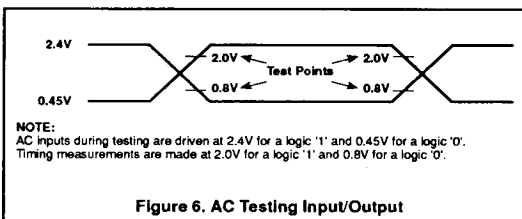
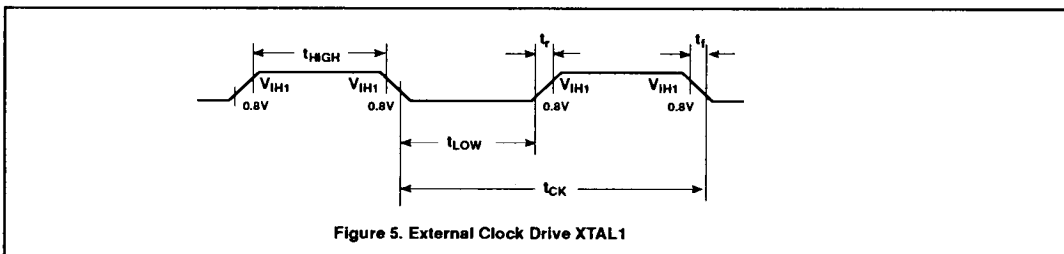
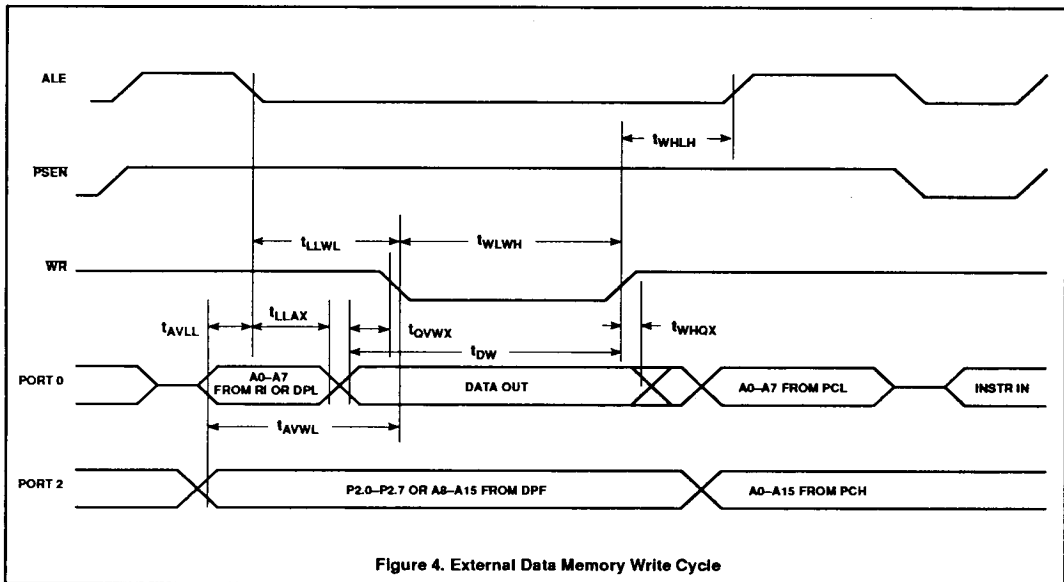


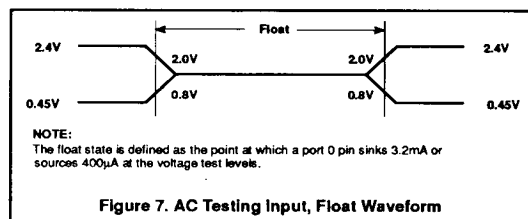
Figure 3. External Data Memory Read Cycle

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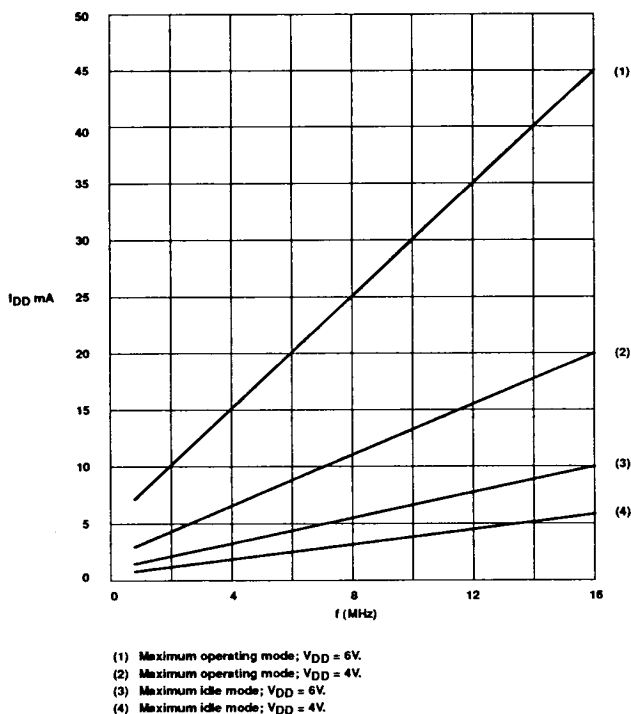
NOTE:
AC inputs during testing are driven at 2.4V for a logic '1' and 0.45V for a logic '0'.
Timing measurements are made at 2.0V for a logic '1' and 0.8V for a logic '0'.



NOTE:
The float state is defined as the point at which a port 0 pin sinks 3.2mA or sources 400μA at the voltage test levels.

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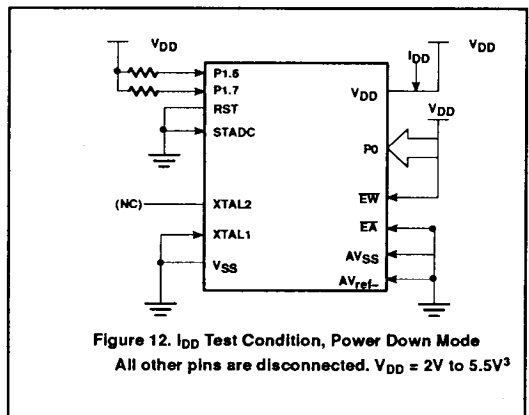
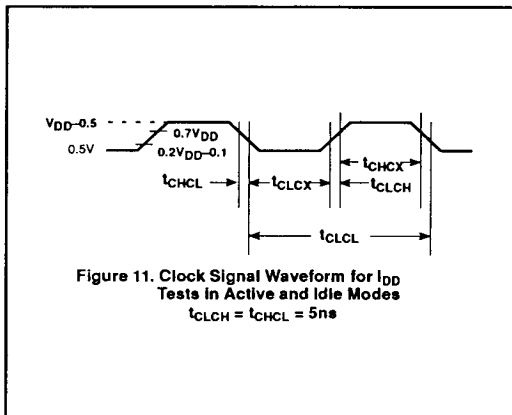
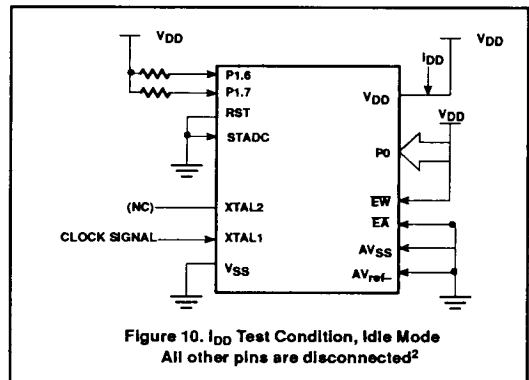
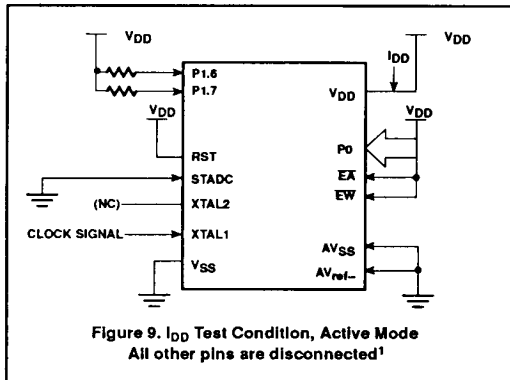
NOTE:

These values are valid only within the frequency specifications of the device under test.

Figure 8. Supply Current (I_{DD}) as a Function of Frequency at XTAL1 (f_{osc})

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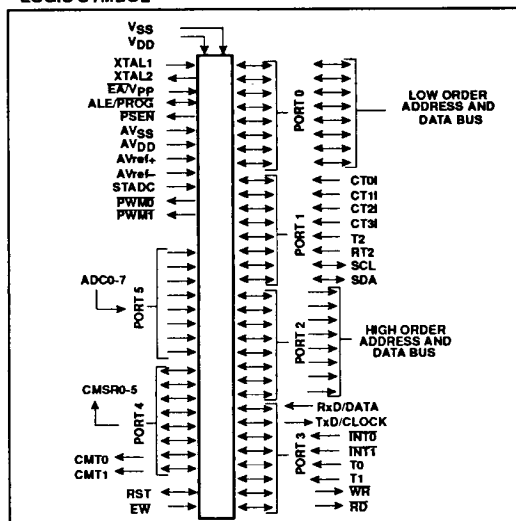
NOTES:

1. Active Mode:
 - a. The following pins must be forced to V_{DD} : $\overline{EA}$, RST, Port 0, and EW.
 - b. The following pins must be forced to V_{SS} : STADC, AV_{SS} , and AV_{ref-} .
 - c. Ports 1.6 and 1.7 should be connected to V_{DD} through resistors of sufficiently high value such that the sink current into these pins cannot exceed the I_{OL1} spec of these pins.
 - d. The following pins must be disconnected: XTAL2 and all pins not specified above.
2. Idle Mode:
 - a. The following pins must be forced to V_{DD} : Port 0 and EW.
 - b. The following pins must be forced to V_{SS} : RST, STADC, AV_{SS} , AV_{ref-} , and $\overline{EA}$.
 - c. Ports 1.6 and 1.7 should be connected to V_{DD} through resistors of sufficiently high value such that the sink current into these pins cannot exceed the I_{OL1} spec of these pins. These pins must not have logic 0 written to them prior to this measurement.
 - d. The following pins must be disconnected: XTAL2 and all pins not specified above.
3. Power Down Mode:
 - a. The following pins must be forced to V_{DD} : Port 0 and EW.
 - b. The following pins must be forced to V_{SS} : RST, STADC, XTAL1, AV_{SS} , AV_{ref-} , and $\overline{EA}$.
 - c. Ports 1.6 and 1.7 should be connected to V_{DD} through resistors of sufficiently high value such that the sink current into these pins cannot exceed the I_{OL1} spec of these pins. These pins must not have logic 0 written to them prior to this measurement.
 - d. The following pins must be disconnected: XTAL2 and all pins not specified above.

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LOGIC SYMBOL



EPROM CHARACTERISTICS

The 87C552 is programmed by using a modified Quick-Pulse Programming™ algorithm. It differs from older methods in the value used for V_{PP} (programming supply voltage) and in the width and number of the ALE/PROG pulses.

The 87C552 contains two signature bytes that can be read and used by an EPROM programming system to identify the device. The signature bytes identify the device as an 87C552 manufactured by Signetics.

Table 3 shows the logic levels for reading the signature byte, and for programming the program memory, the encryption table, and the lock bits. The circuit configuration and waveforms for quick-pulse programming are shown in Figures 13 and 14. Figure 15 shows the circuit configuration for normal program memory verification.

Quick-Pulse Programming

The setup for microcontroller quick-pulse programming is shown in Figure 13. Note that the 87C552 is running with a 4 to 6MHz oscillator. The reason the oscillator needs to be running is that the device is executing internal address and program data transfers.

The address of the EPROM location to be programmed is applied to ports 1 and 2, as

shown in Figure 13. The code byte to be programmed into that location is applied to port 0. RST, PSEN, and pins of ports 2 and 3 specified in Table 3 are held at the "Program Code Data" levels indicated in Table 3. The ALE/PROG is pulsed low 25 times as shown in Figure 14.

To program the encryption table, repeat the 25-pulse programming sequence for addresses 0 through 1FH, using the "Pgm Encryption Table" levels. Do not forget that after the encryption table is programmed, verification cycles will produce only encrypted data.

To program the lock bits, repeat the 25-pulse programming sequence using the "Pgm Lock Bit" levels. After one lock bit is programmed, further programming of the code memory and encryption table is disabled. However, the other lock bit can still be programmed.

Note that the EA/ V_{PP} pin must not be allowed to go above the maximum specified V_{PP} level for any amount of time. Even a narrow glitch above that voltage can cause permanent damage to the device. The V_{PP} source should be well regulated and free of glitches and overshoot.

Program Verification

If lock bit 2 has not been programmed, the on-chip program memory can be read out for

program verification. The address of the program memory locations to be read is applied to ports 1 and 2 as shown in Figure 15. The other pins are held at the "Verify Code Data" levels indicated in Table 3. The contents of the address location will be emitted on port 0. External pull-ups are required on port 0 for this operation.

If the encryption table has been programmed, the data presented at port 0 will be the exclusive NOR of the program byte with one of the encryption bytes. The user will have to know the encryption table contents in order to correctly decode the verification data. The encryption table itself cannot be read out.

Reading the Signature Bytes

The signature bytes are read by the same procedure as a normal verification of locations 030H and 031H, except that P3.6 and P3.7 need to be pulled to a logic low. The values are:

(030H) = 15H indicates manufactured by Philips Components

(031H) = 94H indicates 87C552

Program/Verify Algorithms

Any algorithm in agreement with the conditions listed in Table 3, and which satisfies the timing specifications, is suitable.

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Table 3. EPROM Programming Modes

MODE	RST	PSEN	ALE/PROG	EA/V _{PP}	P2.7	P2.6	P3.7	P3.6
Read signature	1	0	1	1	0	0	0	0
Program code data	1	0	0*	V _{PP}	1	0	1	1
Verify code data	1	0	1	1	0	0	1	1
Pgm encryption table	1	0	0*	V _{PP}	1	0	1	0
Pgm lock bit 1	1	0	0*	V _{PP}	1	1	1	1
Pgm lock bit 2	1	0	0*	V _{PP}	1	1	0	0

NOTES:

1. 0 = Valid low for that pin; 1 = valid high for that pin.

2. V_{PP} = 12.75V ±0.25V.3. V_{DD} = 5V ±10% during programming and verification.*ALE/PROG receives 25 programming pulses whilst V_{PP} is held at 12.75V. Each programming pulse is low for 100µs (±10µs) and high for a minimum of 10µs.

Erasure Characteristics

Erasure of the EPROM begins to occur when the chip is exposed to light with wavelengths shorter than approximately 4,000 angstroms. Since sunlight and fluorescent lighting have wavelengths in this range, exposure to the light sources over an extended time (about 1 week in sunlight, or 3 years in room level fluorescent lighting) could cause inadvertent

erasure. For this and secondary effects, it is recommended that an opaque label be placed over the window. For elevated temperature or environments where solvents are being used, apply Kapton tape Fluorglas part number 2345-5, or equivalent.

The recommended erasure procedure is ex-

posure to ultraviolet light (at 2537 angstroms) to an integrated dose of at least 15W-sec/cm². Exposing the EPROM to an ultraviolet lamp of 12,000µW/cm² rating for 20 to 39 minutes, at a distance of about 1 inch, should be sufficient. Erasure leaves the array in an all 1s state.

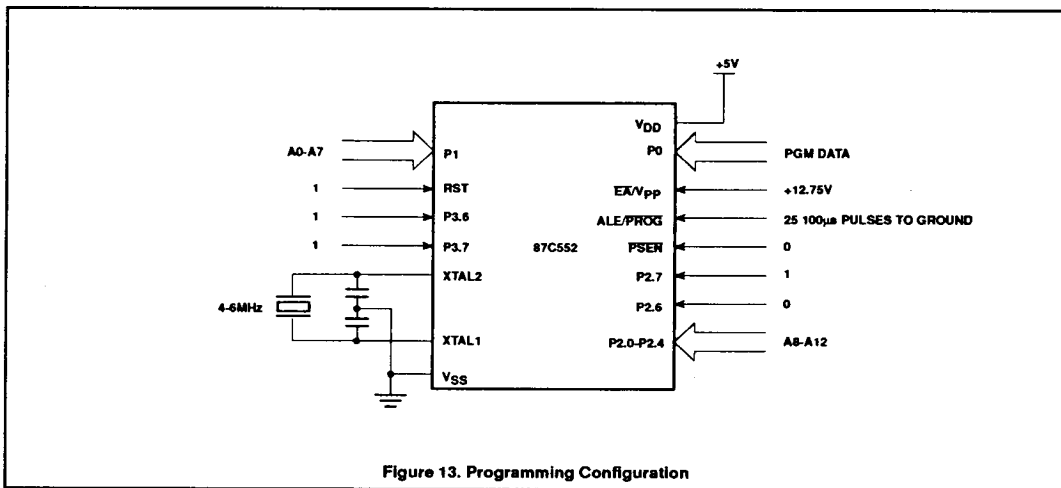
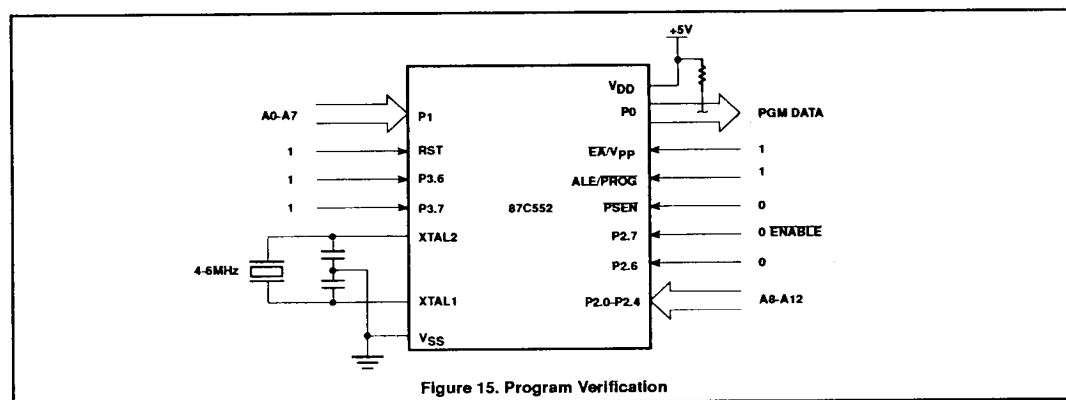
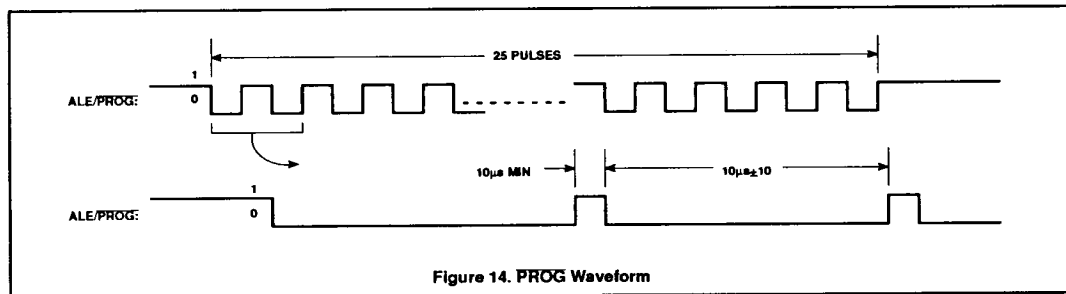


Figure 13. Programming Configuration

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EPROM PROGRAMMING AND VERIFICATION CHARACTERISTICS

 $T_A = 21^\circ\text{C to } +27^\circ\text{C}$, $V_{DD} = 5\text{V} \pm 10\%$, $V_{SS} = 0\text{V}$ (See Figure 16)

SYMBOL	PARAMETER	MIN	MAX	UNIT
V_{PP}	Programming supply voltage	12.5	13.0	V
I_{PP}	Programming supply current		50	mA
$1/t_{CLCL}$	Oscillator frequency	4	6	MHz
t_{AVGL}	Address setup to PROG low	$48t_{CLCL}$		
t_{GHAX}	Address hold after PROG	$48t_{CLCL}$		
t_{DVGL}	Data setup to PROG low	$48t_{CLCL}$		
t_{GHDX}	Data hold after PROG	$48t_{CLCL}$		
t_{EHSB}	P2.7 (ENABLE) high to V_{PP}	$48t_{CLCL}$		
t_{SHGL}	V_{PP} setup to PROG low	10		μs
t_{GHSL}	V_{PP} hold after PROG	10		μs
t_{GLGH}	PROG width	90	110	μs
t_{AVQV}	Address to data valid		$48t_{CLCL}$	
t_{ELOZ}	ENABLE low to data valid		$48t_{CLCL}$	
t_{EHQZ}	Data float after ENABLE	0	$48t_{CLCL}$	
t_{GHGL}	PROG high to PROG low	10		μs

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