

3 1/2 Digit A/D Converter

TSC7116 (LCD Drive) TSC7117 (LED Drive)

- Direct Display Drive
- Display Hold Function

Absolute Maximum Ratings

TSC7116

Supply Voltage (V^+ to V^-)	15 V
Analog Input Voltage (either input) (Note 1)	V^+ to V^-
Reference Input Voltage (either input)	V^+ to V^-
Clock Input	Test to V^+
Power Dissipation (Note 2)	
CerDIP Package	1000 mW
Plastic Package	800 mW
Operating Temperature	
"C" Devices	0°C to +70°C
"I" Devices	-25°C to +85°C
Storage Temperature	-65°C to +160°C
Lead Temperature (Soldering, 60 sec)	300°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated

TSC7117

Supply Voltage	
V^+	+6 V
V^-	-9 V
Analog Input Voltage (either input) (Note 1)	V^+ to V^-
Reference Input Voltage (either input)	V^+ to V^-
Clock Input	GND to V^+
Power Dissipation (Note 1)	
CerDIP Package	1000 mW
Plastic Package	800 mW
Operating Temperature	
"C" Devices	0°C to +70°C
"I" Devices	-25°C to +85°C
Storage Temperature	-65°C to +160°C
Lead Temperature (Soldering, 60 sec)	300°C

in the operational sections of the specifications is not implied. Exposure to Absolute Maximum Rating Conditions for extended periods may affect device reliability.

Electrical Characteristics (Note 3)

CHARACTERISTICS	CONDITIONS	MIN	TYP	MAX	UNIT
Zero Input Reading	$V_{IN} = 0.0$ V Full-Scale = 200.0 mV	-000.0	±000.0	+000.0	Digital Reading
Ratiometric Reading	$V_{IN} = V_{REF}$ $V_{REF} = 100$ mV	999	999/1000	1000	Digital Reading
Rollover Error (Difference in Reading for Equal Positive and Negative Reading Near Full-Scale)	$-V_{IN} = +V_{IN} = 200.0$ mV	-1	±0.2	+1	Counts
Linearity (Max. Deviation From Best Straight Line Fit)	Full-Scale = 200 mV or Full-Scale = 2.000 V	-1	±0.2	+1	Counts
Common-Mode Rejection Ratio (Note 4)	$V_{CM} = \pm 1$ V, $V_{IN} = 0$ V. Full-Scale = 200.0 mV	—	50	—	μV/V
Noise (Pk - Pk Value Not Exceeded 95% of Time)	$V_{IN} = 0$ V Full-Scale = 200.0 mV	—	15	—	μV
Leakage Current @ Input	$V_{IN} = 0$ V	—	1	10	pA
Zero Reading Drift	$V_{IN} = 0$ V "C" Device = 0°C to 70°C $V_{IN} = 0$ V "I" Device = -25°C to +85°C	—	0.2 1.0	1 2	μV/°C
Scale Factor Temperature Coefficient	$V_{IN} = 199.0$ mV, "C" Device = 0°C to 70°C (Ext. Ref = 0 ppm/°C) $V_{IN} = 199.0$ mV "I" Device: -25°C to +85°C	—	1	5 20	ppm/°C ppm/°C
Input Resistance, Pin 1 (Note 6)		30	70	—	kΩ
V_{IL} , Pin 1 (TSC7116 only)		—	—	Test +1.5	V
V_{IL} , Pin 1 (TSC7117 only)		—	—	GND +1.5	V
V_{IH} , Pin 1 (Both)		$V^+ - 1.5$	—	—	V
Supply Current (Does Not Include LED Current for 7107)	$V_{IN} = 0$	—	0.8	1.8	mA
Analog Common Voltage (With Respect to Pos. Supply)	25 kΩ Between Common and Pos. Supply	2.4	2.8	3.2	V
Temp. Coeff. of Analog common (With Respect to Pos. Supply)	25 kΩ Between Common and Pos. Supply	—	80	—	ppm/°C
TSC7116 ONLY Pk - Pk Segment Drive Voltage (Note 5)	V^+ to $V^- = 9$ V	4	5	6	V

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Electrical Characteristics (Cont.)

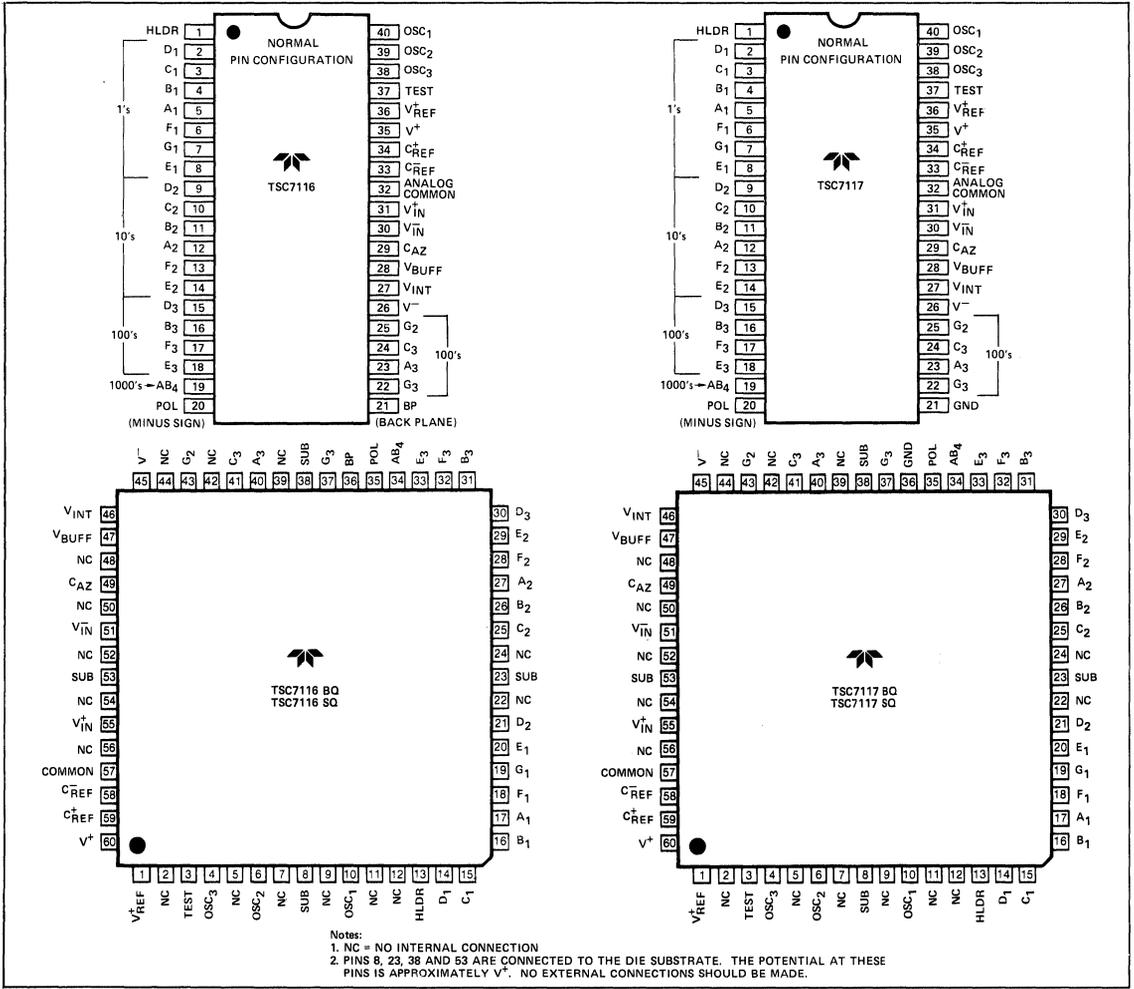
CHARACTERISTICS	CONDITIONS	MIN	TYP	MAX	UNIT
TSC7116 ONLY Pk - Pk Backplane Drive Voltage (Note 5)	V ⁺ to V ⁻ = 9 V	4	5	6	V
TSC7117 ONLY Segment Sinking Current (Except Pin 19)	V ⁺ = 5.0 V Segment Voltage = 3 V	5	8.0	—	mA
TSC7117 ONLY Segment Sinking Current (Pin 19 Only)	V ⁺ = 5.0 V Segment Voltage = 3 V	10	16	—	mA

NOTES:

- Input voltages may exceed the supply voltages provided the input current is limited to ± 100 µA.
- Dissipation rating assumes device is mounted with all leads soldered to printed circuit board.
- Unless otherwise noted, specifications apply to both the TSC7116 and TSC7117 at T_A = 25°C, f_{LOCK} = 48 kHz. TSC7116 is tested in the circuit of Figure 1. TSC7117 is tested in the circuit of Figure 2.
- Refer to "Differential Input" discussion.
- Backplane drive is in phase with segment drive for 'off' segment, 180° out of phase for 'on' segment. Frequency is 20 times conversion rate. Average dc component is less than 50 mV.
- The TSC7116 logic input has an internal pull-down resistor connected from HLDR, Pin 1, to TEST, Pin 37. The TSC7117 logic input has an internal pull-down resistor connected from HLDR, Pin 1 to GROUND, Pin 21.

Pin Configuration

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Ordering Information

Part No.	Package	Pin Layout	Temp. Range	Display Drive
TSC7116CPL	40-Pin Plastic Dip	Normal	0°C to +70°C	LCD
TSC7116IPL	40-Pin Plastic Dip	Normal	-25°C to +85°C	LCD
TSC7116CJL	40-Pin CerDIP	Normal	0°C to +70°C	LCD
TSC7116IJL	40-Pin CerDIP	Normal	-25°C to +85°C	LCD
TSC7116CBQ	60-Pin Plastic Flat Package	Formed Leads	0°C to +70°C	LCD
TSC7116CSQ	60-Pin Plastic Flat Package	Unformed Leads	0°C to +70°C	LCD
TSC7117CPL	40-Pin Plastic Dip	Normal	0°C to +70°C	LED
TSC7117IPL	40-Pin Plastic Dip	Normal	-25°C to +85°C	LED

Part No.	Package	Pin Layout	Temp. Range	Display Drive
TSC7117CJL	40-Pin CerDIP	Normal	0°C to +70°C	LED
TSC7117IJL	40-Pin CerDIP	Normal	-25°C to +85°C	LED
TSC7117CBQ	60-Pin Plastic Flat Package	Formed Leads	0°C to +70°C	LED
TSC7117CSQ	60-Pin Plastic Flat Package	Unformed Leads	0°C to +70°C	LED
Devices with Burn-In (160 Hours at +125°C)				
TSC7116CPL/BI	40-Pin Plastic Dip	Normal	0°C to +70°C	LCD
TSC7117CPL/BI	40-Pin Plastic Dip	Normal	0°C to +70°C	LED

Pin Description

40-Pin DIP Pin Number	60-Pin Flat Package Pin Number	Name	Description
1	13	HLDR	Hold Pin, Logic 1 holds present display reading.
2	14	D ₁	Activates the D section of the units display.
3	15	C ₁	Activates the C section of the units display.
4	16	B ₁	Activates the B section of the units display.
5	17	A ₁	Activates the A section of the units display.
6	18	F ₁	Activates the F section of the units display.
7	19	G ₁	Activates the G section of the units display.
8	20	E ₁	Activates the E section of the units display.
9	21	D ₂	Activates the D section of the tens display.
10	25	C ₂	Activates the C section of the tens display.
11	26	B ₂	Activates the B section of the tens display.
12	27	A ₂	Activates the A section of the tens display.
13	28	F ₂	Activates the F section of the tens display.
14	29	E ₂	Activates the E section of the tens display.
15	30	D ₃	Activates the D section of the hundreds display.
16	31	B ₃	Activates the B section of the hundreds display.
17	32	F ₃	Activates the F section of the hundreds display.
18	33	E ₃	Activates the E section of the hundreds display.
19	34	AB ₄	Activates both halves of the 1 in the thousands display.
20	35	POL	Activates the negative polarity display.
21	36	BP GND	TSC7116: LCD Backplane drive output. TSC7117: Digital Ground.
22	37	G ₃	Activates the G section of the hundreds display.
23	40	A ₃	Activates the A section of the hundreds display.
24	41	C ₃	Activates the C section of the hundreds display.
25	43	G ₂	Activates the G section of the tens display.
26	45	V ⁻	Negative power supply voltage.
27	46	V _{INT}	Integrator output. Connection point for integration capacitor. See INTEGRATING CAPACITOR section for additional details.

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Pin Description (Cont.)

40-Pin DIP Pin Number Normal	60-Pin Flat Package Pin Number	Name	Description
28	47	V _{BUFF}	Integration resistor connection. Use a 47 kΩ for a 200 mV full-scale range and a 470 kΩ for 2 V full-scale range.
29	49	C _{AZ}	The size of the auto-zero capacitor influences the system noise. Use a 0.47 μF capacitor for a 200 mV full-scale, and a 0.047 μF capacitor for a 2 volt full-scale. See paragraph on AUTO-ZERO CAPACITOR for more details.
30	51	V _{IN} ⁻	The analog low input is connected to this pin.
31	55	V _{IN} ⁺	The analog high input signal is connected to this pin.
32	57	Analog Common	This pin is primarily used to set the analog common-mode voltage for battery operation or in systems where the input signal is referenced to the power supply. See paragraph on ANALOG COMMON for more details. It also acts as a reference voltage source.
33	58	C _{REF} ⁻	See pin 34.
34	59	C _{REF} ⁺	A 0.1 μF capacitor is used in most applications. If a large common-mode voltage exists (for example the V _{IN} pin is not at analog common), and a 200 mV scale is used, a 1.0 μF is recommended and will hold the rollover error to 0.5 count.
35	60	V ⁺	Positive Power Supply Voltage.
36	1	V _{REF} ⁺	The analog input required to generate a full-scale output (1,999 counts). Place 100 mV between pins 32 and 36 for 199.9 mV full-scale. Place 1.00 volts between pins 32 and 36 for 2 volts full-scale. See paragraph on REFERENCE VOLTAGE.
37	3	Test	Lamp test. When pulled high (to V ⁺) all segments will be turned on and the display should read -1888. It may also be used as a negative supply for externally generated decimal points. See paragraph under TEST for additional information.
38	4	OSC ₃	See pin 40.
39	6	OSC ₂	See pin 40.
40	10	OSC ₁	Pins 40, 39, 38 make up the oscillator section. For a 48 kHz clock (3 readings per section) connect pin 40 to the junction of a 100 kΩ resistor and a 100 pF capacitor. The 100 kΩ resistor is tied to pin 39 and the 100 pF capacitor is tied to pin 38.

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Analog Section

Figure 3 shows the Block Diagram of the Analog Section for the TSC7116 and TSC7117. Each measurement cycle is divided into three phases. They are (1) auto-zero (A-Z), (2) signal integrate (INT) and (3) reference (REF).

Auto-Zero Phase

Input high and low are disconnected from the pins and internally shorted to analog common. The reference capacitor is charged to the reference voltage. A feedback loop is closed around the system to charge the auto-zero capacitor C_{AZ} to compensate for offset voltages in the buffer amplifier, integrator, and comparator. Since the comparator is included in the loop, the A-Z accuracy is limited only by the noise of the system. The offset referred to the input is less than 10 μV.

Signal Integrate Phase

The auto-zero loop is opened, the internal short is removed, and the internal input high and low are connected to the external pins. The converter then integrates the differential voltage between V_{IN}⁻ and V_{IN}⁺ for a fixed time. This differential voltage can be within a wide common-mode range; within one volt of either supply. If, on the other hand, the input signal has no return with respect to the converter power supply, V_{IN}⁻ can be tied to analog common to establish the correct common-mode voltage. At the end of this phase, the polarity of the integrated signal is determined.

Reference Integrate Phase

The final phase is reference integrate or de-integrate. Input low is internally connected to analog common and input high is connected across the previously charged reference capacitor. Circuitry within the chip ensures that the capacitor will be connected with the correct polarity to cause the integrator output to return to zero. The time required for the output to return to zero is proportional to the input signal. The digital reading displayed is:

$$1000 \times \frac{V_{IN}}{V_{REF}}$$

Reference

The positive reference voltage (V_{REF}⁺) is referenced to analog common.

Differential Input

The input can accept differential voltages anywhere within the common-mode range of the input amplifier; or specifically from 1.0 volts below the positive supply to 1.0 volt above the negative supply. In this range the system has a CMRR of 86 dB typical. However, since the integrator also swings with the common-mode voltage, care must be exercised to assure the integrator output does not saturate. A worse case condition would be a large positive common-mode voltage with a near full-scale negative differential input voltage. The negative input signal drives the integrator positive when most of

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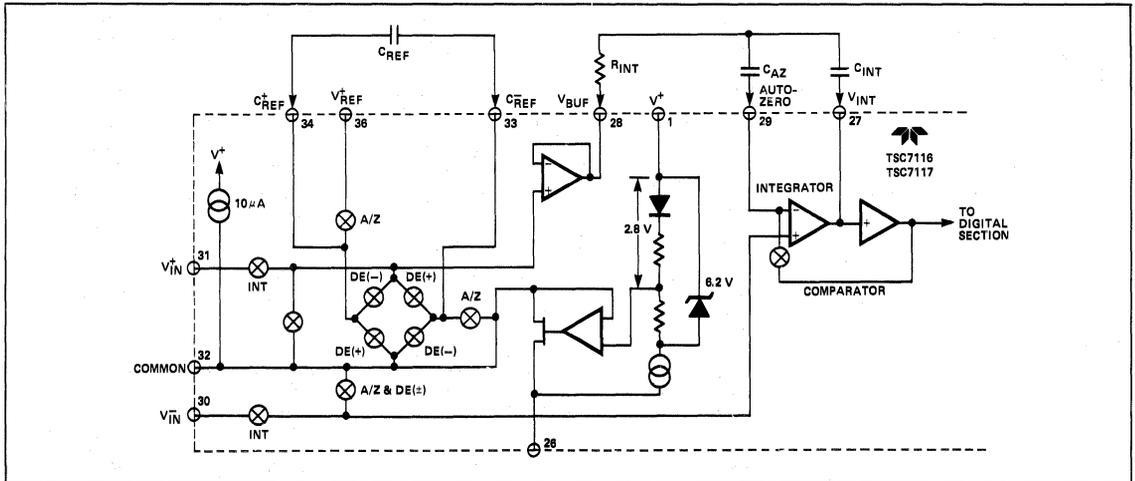


Figure 3: Analog Section of TSC7116/TSC7117

its swing has been used up by the positive common-mode voltage. For these critical applications the integrator swing can be reduced to less than the recommended 2 V full-scale swing with little loss of accuracy. The integrator output can swing within 0.3 volts of either supply without loss of linearity.

Analog Common

This pin is included primarily to set the common-mode voltage for battery operation (TSC7116) or for any system where the input signals are floating with respect to the power supply. The common pin sets a voltage that is approximately 2.8 volts more negative than the positive supply. This is selected to give a minimum end-of-life battery voltage of about 6 V. However, the analog common has some of the attributes of a reference voltage. When the total supply voltage is large enough to cause the zener to regulate (>7 V), the common voltage will have a low voltage coefficient (0.001%/%), low output impedance ($\approx 15 \Omega$), and a temperature coefficient of 80 ppm/ $^{\circ}\text{C}$ typically.

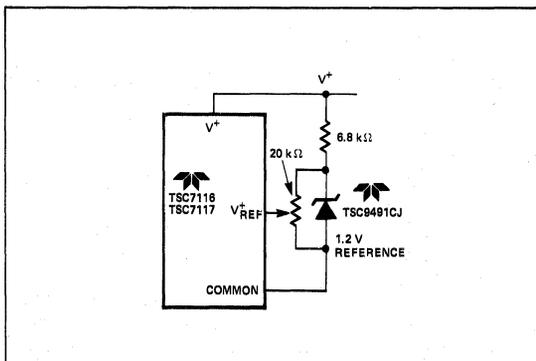


Figure 4: Using an External Reference

An external reference may be added to improve temperature stability or the TSC7116A/TSC7117A devices with lower analog common temperature drift may be used. The circuit is shown in Figure 4.

Analog common is also used as the V_{IN} return during auto-zero and deintegrate. If V_{IN} is different from analog common, a common-mode voltage exists in the system and is taken care of by the excellent CMRR of the converter. However, in some applications V_{IN} will be set at a fixed known voltage (power supply common for instance). In this application, analog common should be tied to the same point, thus removing the common-mode voltage from the converter. The same holds true for the reference voltage. If reference can be conveniently referenced to analog common, it should be since this removes the common-mode voltage from the reference system.

Within the IC, analog common is tied to an N-channel FET that can sink 30 mA or more of current to hold the voltage 2.8 volts below the positive supply (when a load is trying to pull the common line positive). However, there is only 10 μA of source current, so common may easily be tied to a more negative voltage thus over-riding the internal reference.

Test

The TEST pin serves two functions. On the TSC7117 it is coupled to the internally generated digital supply through a 500 Ω resistor. Thus it can be used as the negative supply for externally generated segment drivers such as decimal points or any other presentation the user may want to include on the LCD display. Figures 5 and 6 show such an application. No more than a 1 mA load should be applied.

The second function is a "lamp test." When TEST is pulled high (to V^+) all segments will be turned on and the display should read -1888. The TEST pin will sink about 10 mA under these conditions.

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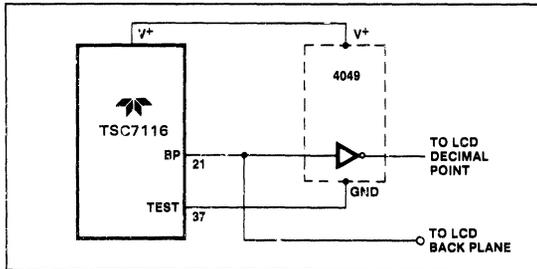


Figure 5: Simple Inverter for Fixed Decimal Point

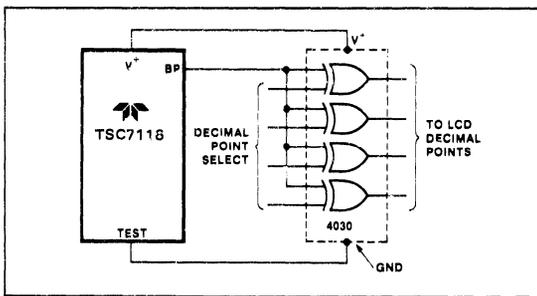


Figure 6: Exclusive "OR" Gate for Decimal Point Drive

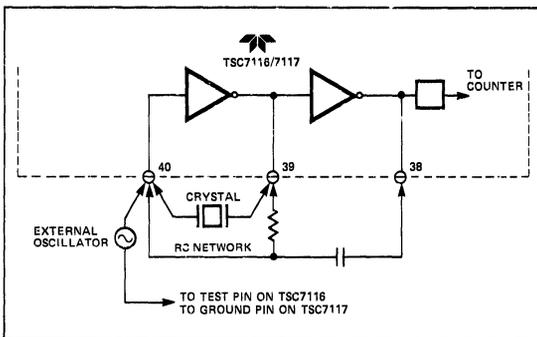


Figure 7: Clock Circuits

Digital Section

Figures 8 and 9 show the digital section for the TSC7116 and TSC7117, respectively. In the TSC7116 (Figure 8), an internal digital ground is generated from a 6 volt Zener diode and a large P channel source follower. This supply is made stiff to absorb the large capacitive currents when the back plane (BP) voltage is switched. The BP frequency is the clock frequency divided by 800. For three readings/second this is a 60 Hz square wave with a nominal amplitude of 5 volts. The segments are driven at the same frequency and amplitude and are in phase with BP when OFF, but out of phase when ON. In all cases, negligible dc voltage exists across the segments.

Figure 9 is the Digital Section of the TSC7117. It is identical to the TSC7116 except that the regulated supply and back plane drive have been eliminated and the segment drive is typically 8 mA. The 1000 output (pin 19) sinks current from two LED segments, and has a 16 mA drive capability. The TSC7117 is designed to drive common anode LEDs.

In both devices, the polarity indication is "on" for negative analog inputs. If V_{IN} and V_{IN} are reversed, this indication can be reversed also, if desired.

System Timing

Figure 9 shows the clocking method used in the TSC7116 and TSC7117. Three clocking methods may be used:

1. An external oscillator connected to pin 40.
2. A crystal between pins 39 and 40.
3. An RC oscillator using all three pins.

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The oscillator frequency is divided by four before it clocks the decade counters. It is then further divided to form the three convert-cycle phases. These are signal integrate (1000 counts), reference de-integrate (0 to 2000 counts) and auto-zero (1000 to 3000 counts). For signals less than full-scale auto-zero gets the unused portion of reference de-integrate. This makes a complete measure cycle of 4,000 (16,000 clock pulses) independent of input voltage. For three readings/second, an oscillator frequency of 48 kHz would be used.

To achieve maximum rejection of 60 Hz pickup, the signal integrate cycle should be a multiple of 60 Hz. Oscillator frequencies of 240 kHz, 120 kHz, 80 kHz, 60 kHz, 43 kHz, 40 kHz, 33-1/3 kHz, etc. should be selected. For 50 Hz rejection, oscillator frequencies of 200 kHz, 100 kHz, 66-2/3 kHz, 50 kHz, 40 kHz, etc. would be suitable. Note that 40 kHz (2.5 readings/second) will reject both 50 and 60 Hz (also 400 and 440 Hz).

HOLD Reading Input

When HLDR is at a logic "HI" the latch will not be updated. A/D conversions will continue but will not be updated until the HLDR is returned to "LOW". To continuously update the display connect to TEST (TSC7116) or GROUND (TSC7117) or disconnect. This input is CMOS compatible with 70K typical resistance to TEST (TSC7116) or GROUND (TSC7117).

Component Value Selection

Auto-Zero Capacitor

The size of the auto-zero capacitor has some influence on the noise of the system. For 200 mV full-scale where noise is very important, a 0.47 μ F capacitor is recommended. On the 2 volt scale, a 0.047 μ F capacitor increase the speed of recovery from overload and is adequate for noise on this scale.

Reference Capacitor

A 0.1 μ F capacitor is acceptable in most applications. However, where a large common-mode voltage exists (i.e. the V_{IN} pin is not at analog common) and a 200 mV scale is used, a large value is required to prevent to roll-over error. Generally 1.0 μ F will hold the roll-over error to 0.5 count in this instance.

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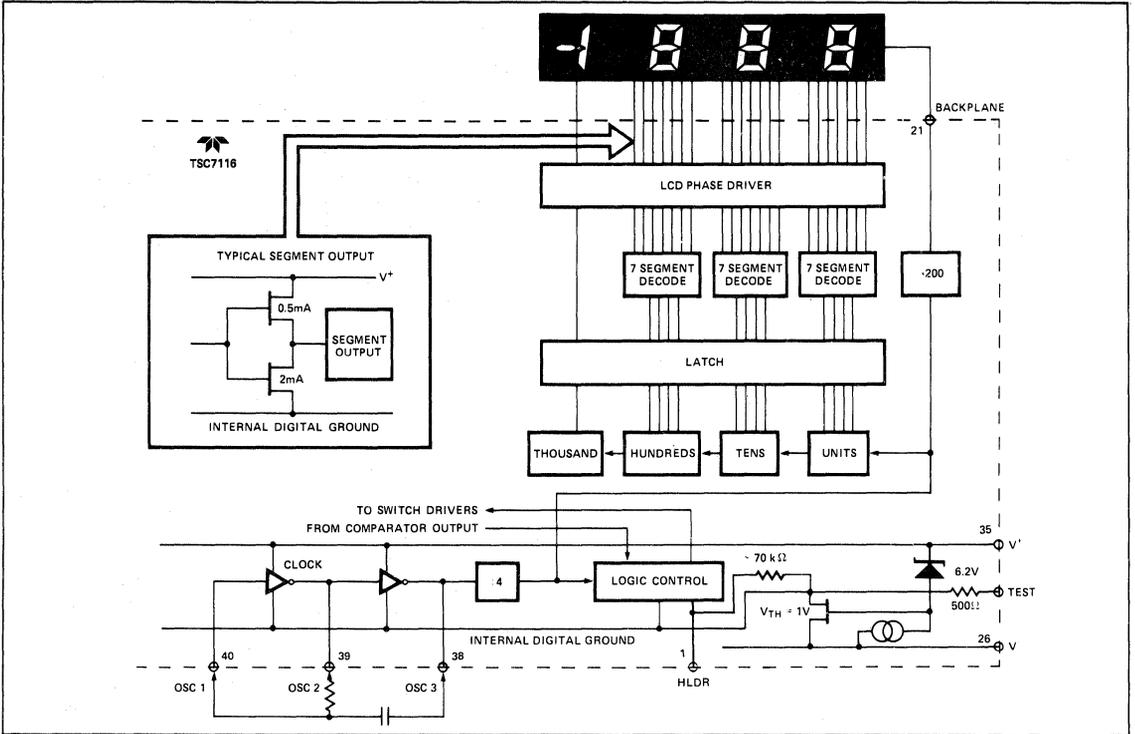


Figure 8: TSC7116 Digital Section

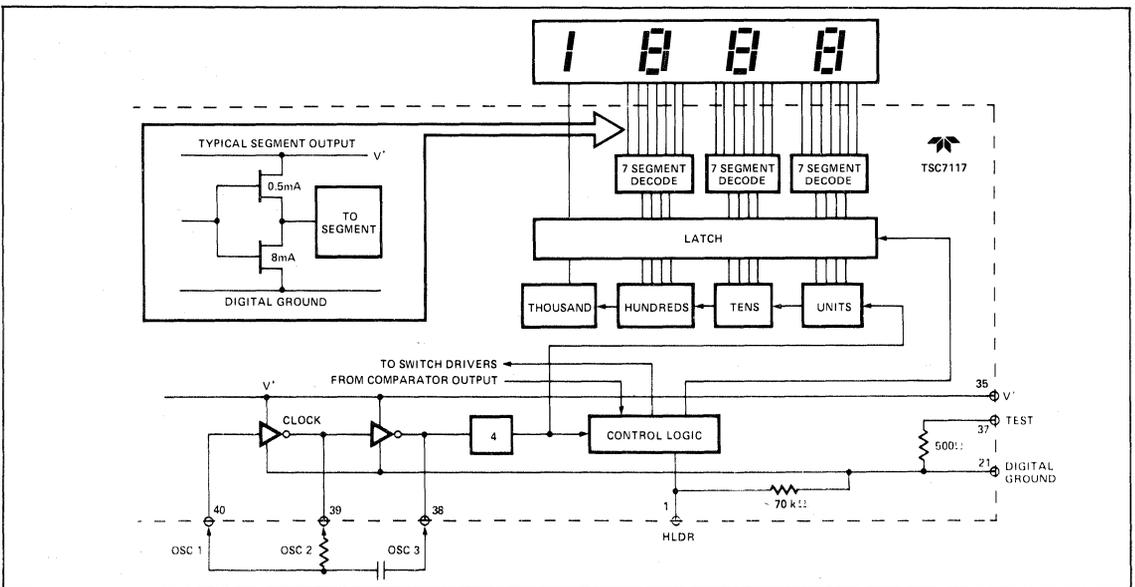


Figure 9: TSC7117 Digital Section

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Integrating Capacitor

The integrating capacitor should be selected to give the maximum voltage swing that ensures tolerance build-up will not saturate the integrator swing (approx. 0.3 volt from either supply). In the TSC7116 or the TSC7117, when the analog common is used as a reference, a nominal ± 2 volt full-scale integrator swing is acceptable. For the TSC7117 with ± 5 volt supplies and analog common tied to supply ground, a ± 3.5 to ± 4 volt swing is nominal. For three readings/second (48 kHz clock) nominal values for C_{INT} are 0.22 μF and 0.10 μF , respectively. If different oscillator frequencies are used, these values should be changed in inverse proportion to maintain the output swing.

The integrating capacitor must have low dielectric absorption to prevent roll-over errors. Polypropylene capacitors are recommended for this application.

Integrating Resistor

Both the buffer amplifier and the integrator have a class A output stage with 100 μA of quiescent current. They can supply 20 μA of drive current with negligible non-linearity. The integrating resistor should be large enough to remain in this very linear region over the input voltage range, but small enough that undue leakage requirements are not placed on the PC board. For 2 volt full-scale, 470 k Ω is near optimum and similarly a 47 k Ω for a 200.0 mV scale.

Oscillator Components

For all ranges of frequency a 100 k Ω resistor is recommended and the capacitor is selected from the equation $f = \frac{45}{RC}$. For 48 kHz clock (3 readings/second), $C = 100 \text{ pF}$.

Reference Voltage

To generate full-scale output (2000 counts) the analog input required is: $V_{IN} = 2 V_{REF}$. Thus, for the 200.0 mV and 2.000 volt scale, V_{REF} should equal 100.0 mV and 1.00 volt respectively. In many applications where the A/D is connected to a transducer, there will exist a scale factor between the input voltage and the digital reading. For instance, in a measuring system, the designer might like to have a full-scale reading when the voltage from the transducer is 700 mV. Instead of dividing the input down to 200.0 mV, the designer should use the input voltage directly and select $V_{REF} = 350 \text{ mV}$. Suitable values for integrating resistor and capacitor would be 120 k Ω and 0.22 μF . This makes the system slightly quieter and also avoids a divider network on the input. The TSC7117 with ± 5 V supplies can accept input signals up to ± 4 V. Another advantage of this system occurs when a digital reading of zero is desired for $V_{IN} \neq 0$. Temperature and weighing systems with a variable tare are examples. This offset reading can be conveniently generated by connecting the voltage transducer between V_{IN} and common and the variable (or fixed) offset voltage between common and V_{IN} .

TSC7117 Power Supplies

The TSC7117 is designed to work from ± 5 V supplies. However, if a negative supply is not available, it can be generated from the clock output with two diodes, two capacitors and an inexpensive IC. Figure 10 shows this application.

In selected applications no negative supply is required. The conditions to use a single +5 V supply are:

- The input signal can be referenced to the center of the common-mode range of the converter.
- The signal is less than ± 1.5 volts.
- An external reference is used.

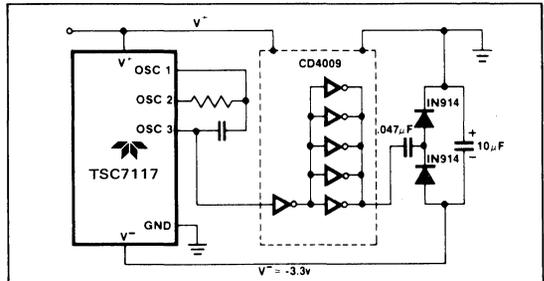


Figure 10: Generating Negative Supply From +5V

Typical Applications

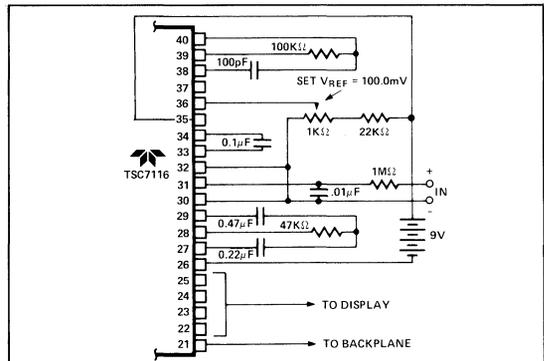


Figure 11: TSC7116 Using the Internal Reference (200 mV Full-Scale, 3 RPS)

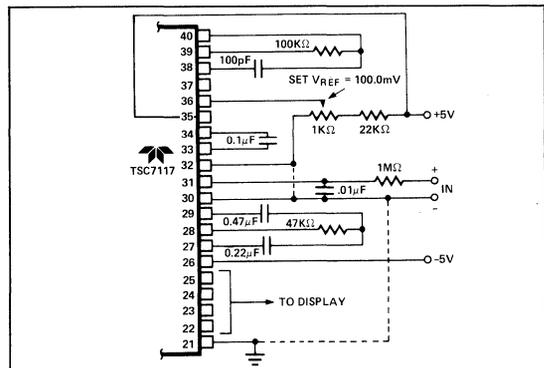


Figure 12: TSC7117 Internal Reference (200 mV Full-Scale, 3 RPS, V_{IN} Tied to GND for Single Ended Inputs).

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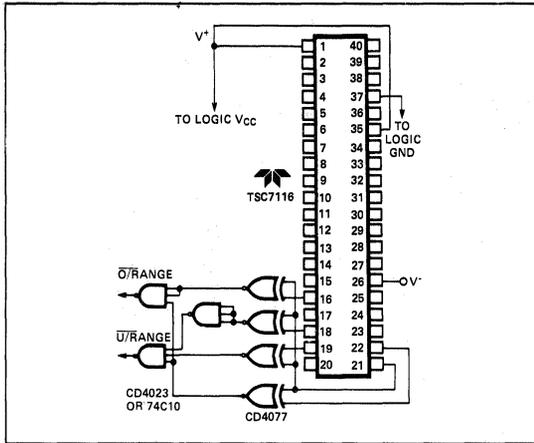


Figure 13: Circuit for Developing Underrange and Overrange Signals from TSC7116 Outputs.

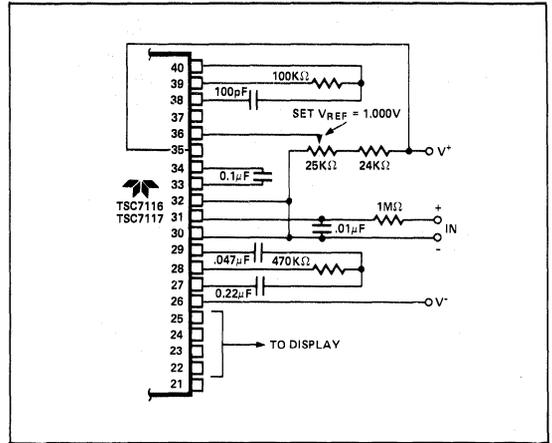


Figure 15: TSC7116/TSC7117: Recommended Component Values for 2.00 V Full-Scale.

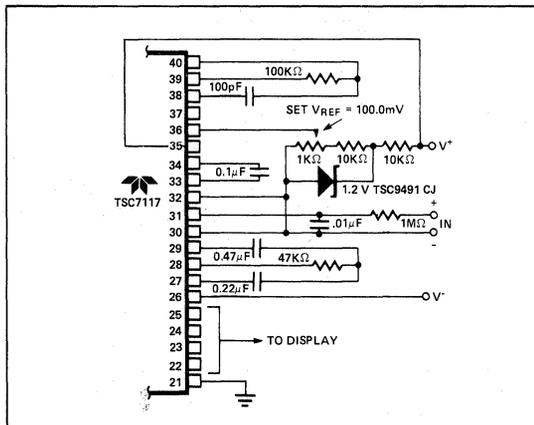


Figure 14: TSC7117 With a 1.2 V External Band-Gap Reference. V_{IN} Tied to Common).

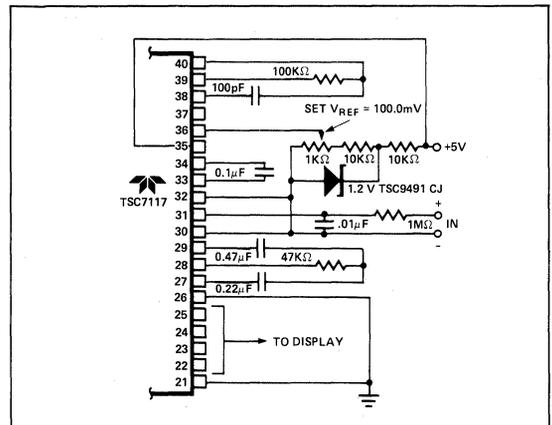


Figure 16: TSC7117 Operated from Single +5 V Supply. An External Reference Must Be Used in This Application.

Applications Information

The TSC7117 sinks the LED display current and this causes heat to build up in the IC package. If the internal voltage reference is used, the changing chip temperature can cause the display to change reading. By reducing package power dissipation such variations can be reduced. By reducing the LED common anode voltage the TSC7117 package power dissipation is reduced.

Figure 17 is a photograph of a curve-tracer display showing the relationship between output current and output voltage for a typical TSC7117CPL. Since a typical LED has 1.8 volts across it at 8 mA, and its common anode is connected to +5 V, the TSC7117 output is at 3.2 V (point A on Fig. 17). Maximum power dissipation is $8.1 \text{ mA} \times 3.2 \text{ V} \times 24 \text{ segments} = 622 \text{ mW}$.

Notice, however, that once the TSC7117 output voltage is above two volts, the LED current is essentially constant as output voltage increases. Reducing the output voltage by 0.7 V (point B of Figure 17) results in 7.7 mA of LED current, only a 5 percent reduction. Maximum power dissipation is now only $7.7 \text{ mA} \times 2.5 \text{ V} \times 24 = 462 \text{ mW}$, a reduction of 26%. An output voltage reduction of 1 volt (point C) reduces LED current by 10% (7.3 mA) but power dissipation by 38%! ($7.3 \text{ mA} \times 2.2 \text{ V} \times 24 = 385 \text{ mW}$).

Reduced power dissipation is very easy to obtain. Fig. 18 shows two ways: either a 5.1 ohm, 1/4 watt resistor or a 1 Amp diode placed in series with the display (but not in series with the TSC7117). The resistor will reduce the TSC7117 output voltage, when all 24 segments are "ON," to point "C" of Fig.

3 1/2 Digit A/D Converter

- Direct Display Drive
- Display Hold Function

TSC7116 (LCD Drive)
TSC7117 (LED Drive)

17. When segments turn off, the output voltage will increase. The diode, on the other hand, will result in a relatively steady output voltage, around point "B."

In addition to limiting maximum power dissipation, the resistor reduces the change in power dissipation as the display changes. This effect is caused by the fact that, as fewer segments are "ON," each "ON" output drops more voltage and current. For the best case of six segments (a "111" display) to worst case (a "1888" display) the resistor circuit will

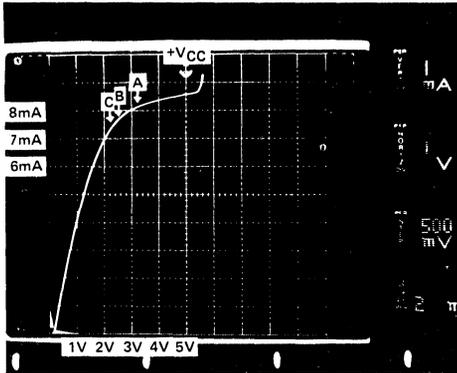


Figure 17: TSC7117 Output Current vs Output Voltage

change about 230 mW, while a circuit without the resistor will change about 470 mW. Therefore, the resistor will reduce the effect of display dissipation on reference voltage drift by about 50%.

The change in LED brightness caused by the resistor is almost unnoticeable as more segments turn off. If display brightness remaining steady is very important to the designer, diode may be used instead of the resistor.

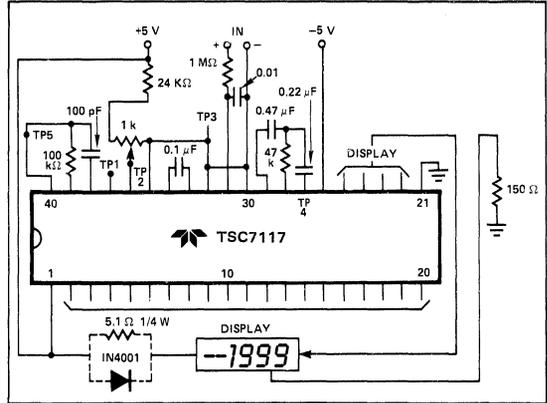


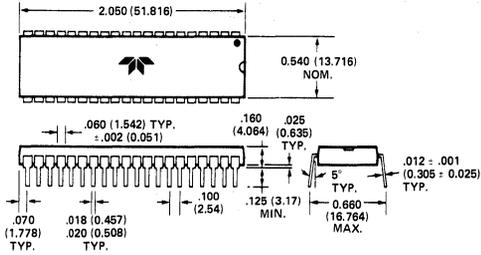
Figure 18: Diode or Resistor Limits Package Power Dissipation

TSC7116 (LCD Drive)
TSC7117 (LED Drive)

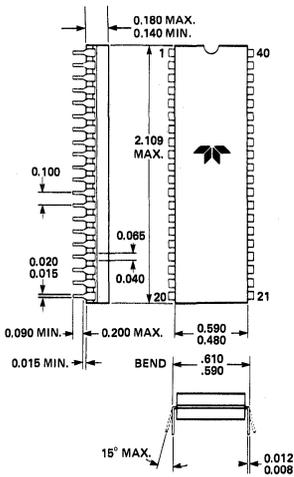
3 1/2 Digit A/D Converter
 • Direct Display Drive
 • Display Hold Function

Package Information

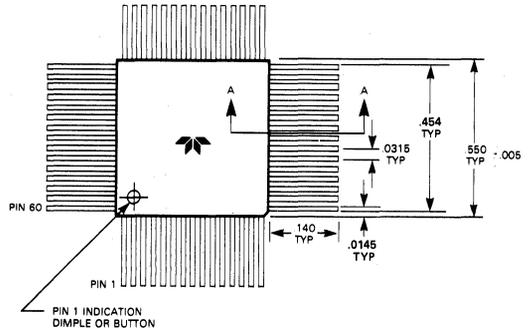
**40-Pin Plastic Dual-In-Line Package
 (Package #17)**



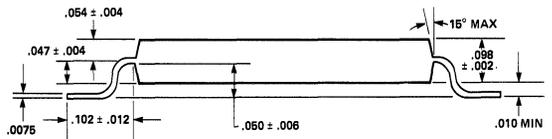
**40-Pin CerDIP
 (Package #20)**



60-Pin Plastic Flat Package



**"SQ" Package — Unformed Leads
 (Package #22)**



**"BQ" Package — Formed Leads
 (Package #21)**