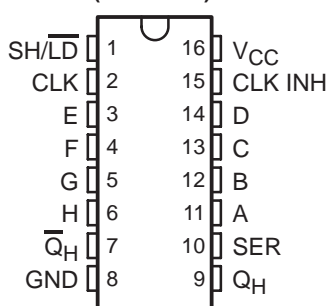


# SN54LV165A, SN74LV165A PARALLEL-LOAD 8-BIT SHIFT REGISTERS

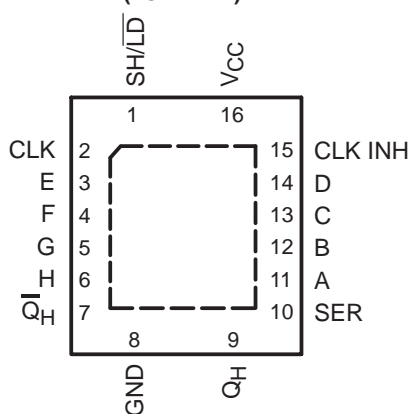
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- 2-V to 5.5-V  $V_{CC}$  Operation
- Max  $t_{pd}$  of 10.5 ns at 5 V
- Support Mixed-Mode Voltage Operation on All Ports
- $I_{off}$  Supports Partial-Power-Down Mode Operation
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)
  - 1000-V Charged-Device Model (C101)

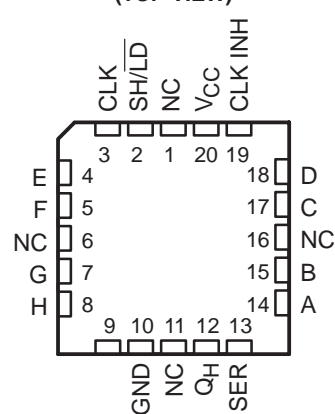
SN54LV165A . . . J OR W PACKAGE  
SN74LV165A . . . D, DB, DGV, NS,  
OR PW PACKAGE  
(TOP VIEW)



SN74LV165A . . . RGY PACKAGE  
(TOP VIEW)



SN54LV165A . . . FK PACKAGE  
(TOP VIEW)



NC – No internal connection

## description/ordering information

The 'LV165A devices are parallel-load, 8-bit shift registers designed for 2-V to 5.5-V  $V_{CC}$  operation.

When the devices are clocked, data is shifted toward the serial output  $Q_H$ . Parallel-in access to each stage is provided by eight individual direct data inputs that are enabled by a low level at the shift/load ( $SH/\overline{LD}$ ) input. The 'LV165A devices feature a clock-inhibit function and a complemented serial output,  $\overline{Q}_H$ .

## ORDERING INFORMATION

$T_A$	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	QFN – RGY	Reel of 1000	SN74LV165ARGYR	LV165A
	SOIC – D	Tube of 40	SN74LV165AD	LV165A
		Reel of 2500	SN74LV165ADR	
	SOP – NS	Reel of 2000	SN74LV165ANSR	74LV165A
	SSOP – DB	Reel of 2000	SN74LV165ADBR	LV165A
	TSSOP – PW	Tube of 90	SN74LV165APW	LV165A
		Reel of 2000	SN74LV165APWR	
Reel of 250		SN74LV165APWT		
TVSOP – DGV	Reel of 2000	SN74LV165ADGVR	LV165A	
–55°C to 125°C	CDIP – J	Tube of 25	SNJ54LV165AJ	SNJ54LV165AJ
	CFP – W	Tube of 150	SNJ54LV165AW	SNJ54LV165AW
	LCCC – FK	Tube of 55	SNJ54LV165AFK	SNJ54LV165AFK

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).



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UNLESS OTHERWISE NOTED this document contains PRODUCTION DATA information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS  
INSTRUMENTS**

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# SN54LV165A, SN74LV165A PARALLEL-LOAD 8-BIT SHIFT REGISTERS

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## description/ordering information (continued)

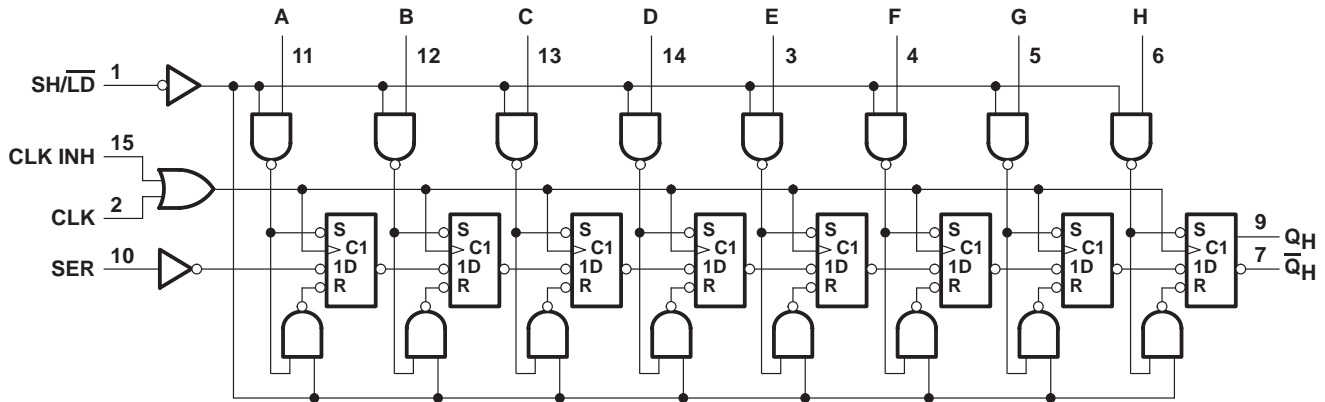
Clocking is accomplished by a low-to-high transition of the clock (CLK) input while  $\overline{SH/LD}$  is held high and clock inhibit (CLK INH) is held low. The functions of CLK and CLK INH are interchangeable. Since a low CLK and a low-to-high transition of CLK INH accomplishes clocking, CLK INH should be changed to the high level only while CLK is high. Parallel loading is inhibited when  $\overline{SH/LD}$  is held high. The parallel inputs to the register are enabled while  $\overline{SH/LD}$  is held low, independently of the levels of CLK, CLK INH, or SER.

These devices are fully specified for partial-power-down applications using  $I_{off}$ . The  $I_{off}$  circuitry disables the outputs, preventing damaging current backflow through the devices when they are powered down.

FUNCTION TABLE

INPUTS			OPERATION
$\overline{SH/LD}$	CLK	CLK INH	
L	X	X	Parallel load
H	H	X	$Q_0$
H	X	H	$Q_0$
H	L	↑	Shift
H	↑	L	Shift

## logic diagram (positive logic)

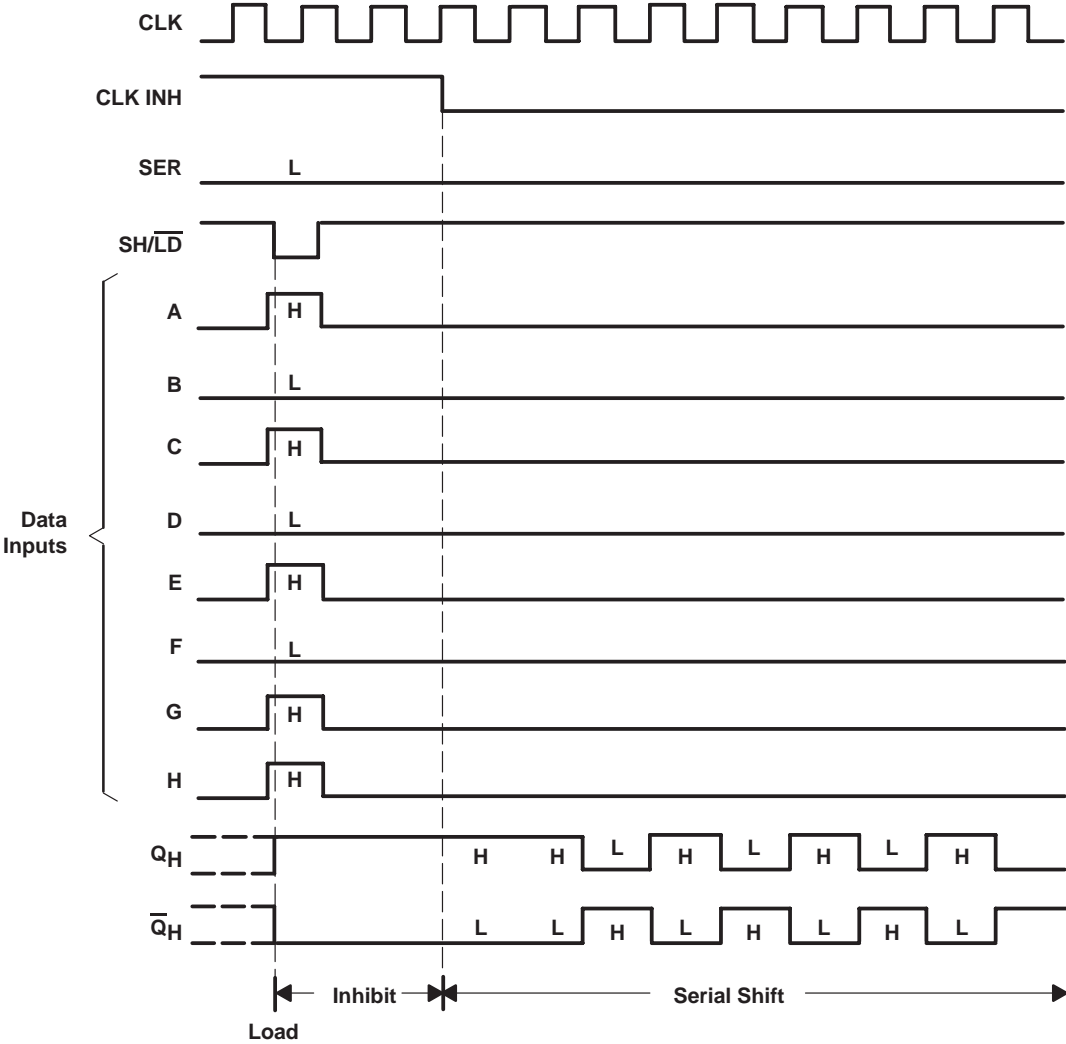


Pin numbers shown are for the D, DB, DGV, J, NS, PW, RGY, and W packages.

# SN54LV165A, SN74LV165A PARALLEL-LOAD 8-BIT SHIFT REGISTERS

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## typical shift, load, and inhibit sequences



# SN54LV165A, SN74LV165A PARALLEL-LOAD 8-BIT SHIFT REGISTERS

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## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$ .....	-0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1) .....	-0.5 V to 7 V
Voltage range applied to any output in the high-impedance or power-off state, $V_O$ (see Note 1) .....	-0.5 V to 7 V
Output voltage range, $V_O$ (see Notes 1 and 2) .....	-0.5 V to $V_{CC} + 0.5$ V
Input clamp current, $I_{IK}$ ( $V_I < 0$ ) .....	-20 mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ ) .....	-50 mA
Continuous output current, $I_O$ ( $V_O = 0$ to $V_{CC}$ ) .....	$\pm 25$ mA
Continuous current through $V_{CC}$ or GND .....	$\pm 50$ mA
Package thermal impedance, $\theta_{JA}$ (see Note 3): D package .....	73°C/W
(see Note 3): DB package .....	82°C/W
(see Note 3): DGV package .....	120°C/W
(see Note 3): NS package .....	67°C/W
(see Note 3): PW package .....	108°C/W
(see Note 4): RGY package .....	39°C/W
Storage temperature range, $T_{stg}$ .....	-65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES:
1. The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
  2. This value is limited to 5.5 V maximum.
  3. The package thermal impedance is calculated in accordance with JESD 51-7.
  4. The package thermal impedance is calculated in accordance with JESD 51-5.



# SN54LV165A, SN74LV165A PARALLEL-LOAD 8-BIT SHIFT REGISTERS

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## recommended operating conditions (see Note 5)

		SN54LV165A		SN74LV165A		UNIT
		MIN	MAX	MIN	MAX	
V <sub>CC</sub>	Supply voltage	2	5.5	2	5.5	V
V <sub>IH</sub>	High-level input voltage	V <sub>CC</sub> = 2 V	1.5	1.5		V
		V <sub>CC</sub> = 2.3 V to 2.7 V	V <sub>CC</sub> × 0.7	V <sub>CC</sub> × 0.7		
		V <sub>CC</sub> = 3 V to 3.6 V	V <sub>CC</sub> × 0.7	V <sub>CC</sub> × 0.7		
		V <sub>CC</sub> = 4.5 V to 5.5 V	V <sub>CC</sub> × 0.7	V <sub>CC</sub> × 0.7		
V <sub>IL</sub>	Low-level input voltage	V <sub>CC</sub> = 2 V		0.5	0.5	V
		V <sub>CC</sub> = 2.3 V to 2.7 V	V <sub>CC</sub> × 0.3	V <sub>CC</sub> × 0.3	V <sub>CC</sub> × 0.3	
		V <sub>CC</sub> = 3 V to 3.6 V	V <sub>CC</sub> × 0.3	V <sub>CC</sub> × 0.3	V <sub>CC</sub> × 0.3	
		V <sub>CC</sub> = 4.5 V to 5.5 V	V <sub>CC</sub> × 0.3	V <sub>CC</sub> × 0.3	V <sub>CC</sub> × 0.3	
V <sub>I</sub>	Input voltage	0	5.5	0	5.5	V
V <sub>O</sub>	Output voltage	0	V <sub>CC</sub>	0	V <sub>CC</sub>	V
I <sub>OH</sub>	High-level output current	V <sub>CC</sub> = 2 V		-50	-50	μA
		V <sub>CC</sub> = 2.3 V to 2.7 V		-2	-2	mA
		V <sub>CC</sub> = 3 V to 3.6 V		-6	-6	
		V <sub>CC</sub> = 4.5 V to 5.5 V		-12	-12	
I <sub>OL</sub>	Low-level output current	V <sub>CC</sub> = 2 V		50	50	μA
		V <sub>CC</sub> = 2.3 V to 2.7 V		2	2	mA
		V <sub>CC</sub> = 3 V to 3.6 V		6	6	
		V <sub>CC</sub> = 4.5 V to 5.5 V		12	12	
Δt/Δv	Input transition rise or fall rate	V <sub>CC</sub> = 2.3 V to 2.7 V		200	200	ns/V
		V <sub>CC</sub> = 3 V to 3.6 V		100	100	
		V <sub>CC</sub> = 4.5 V to 5.5 V		20	20	
T <sub>A</sub>	Operating free-air temperature	-55	125	-40	85	°C

NOTE 5: All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V <sub>CC</sub>	SN54LV165A			SN74LV165A			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V <sub>OH</sub>	I <sub>OH</sub> = -50 μA	2 V to 5.5 V	V <sub>CC</sub> -0.1			V <sub>CC</sub> -0.1			V
	I <sub>OH</sub> = -2 mA	2.3 V	2			2			
	I <sub>OH</sub> = -6 mA	3 V	2.48			2.48			
	I <sub>OH</sub> = -12 mA	4.5 V	3.8			3.8			
V <sub>OL</sub>	I <sub>OL</sub> = 50 μA	2 V to 5.5 V			0.1			0.1	V
	I <sub>OL</sub> = 2 mA	2.3 V			0.4			0.4	
	I <sub>OL</sub> = 6 mA	3 V			0.44			0.44	
	I <sub>OL</sub> = 12 mA	4.5 V			0.55			0.55	
I <sub>I</sub>	V <sub>I</sub> = 5.5 V or GND	0 to 5.5 V			±1			±1	μA
I <sub>CC</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0	5.5 V			20			20	μA
I <sub>off</sub>	V <sub>I</sub> or V <sub>O</sub> = 0 to 5.5 V	0			5			5	μA
C <sub>i</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND	3.3 V		1.7			1.7		pF

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# SN54LV165A, SN74LV165A PARALLEL-LOAD 8-BIT SHIFT REGISTERS

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timing requirements over recommended operating free-air temperature range,  $V_{CC} = 2.5 V \pm 0.2 V$  (unless otherwise noted) (see Figure 1)

		$T_A = 25^\circ C$		SN54LV165A		SN74LV165A		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
$t_w$	Pulse duration	CLK high or low	8.5		9		9	ns
		SH/LD low	11		13		13	
$t_{su}$	Setup time	SH/LD high before CLK $\uparrow$	7		8.5		8.5	ns
		SER before CLK $\uparrow$	8.5		9.5		9.5	
		CLK INH before CLK $\uparrow$	7		7		7	
		Data before SH/LD $\uparrow$	11.5		12		12	
$t_h$	Hold time	SER data after CLK $\uparrow$	-1		0		0	ns
		Parallel data after SH/LD $\uparrow$	0		0.5		0.5	
		SH/LD high after CLK $\uparrow$	0		0		0	

timing requirements over recommended operating free-air temperature range,  $V_{CC} = 3.3 V \pm 0.3 V$  (unless otherwise noted) (see Figure 1)

		$T_A = 25^\circ C$		SN54LV165A		SN74LV165A		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
$t_w$	Pulse duration	CLK high or low	6		7		7	ns
		SH/LD low	7.5		9		9	
$t_{su}$	Setup time	SH/LD high before CLK $\uparrow$	5		6		6	ns
		SER before CLK $\uparrow$	5		6		6	
		CLK INH before CLK $\uparrow$	5		5		5	
		Data before SH/LD $\uparrow$	7.5		8.5		8.5	
$t_h$	Hold time	SER data after CLK $\uparrow$	0		0		0	ns
		Parallel data after SH/LD $\uparrow$	0.5		0.5		0.5	
		SH/LD high after CLK $\uparrow$	0		0		0	

timing requirements over recommended operating free-air temperature range,  $V_{CC} = 5 V \pm 0.5 V$  (unless otherwise noted) (see Figure 1)

		$T_A = 25^\circ C$		SN54LV165A		SN74LV165A		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
$t_w$	Pulse duration	CLK high or low	4		4		4	ns
		SH/LD low	5		6		6	
$t_{su}$	Setup time	SH/LD high before CLK $\uparrow$	4		4		4	ns
		SER before CLK $\uparrow$	4		4		4	
		CLK INH before CLK $\uparrow$	3.5		3.5		3.5	
		Data before SH/LD $\uparrow$	5		5		5	
$t_h$	Hold time	SER data after CLK $\uparrow$	0.5		0.5		0.5	ns
		Parallel data after SH/LD $\uparrow$	1		1		1	
		SH/LD high after CLK $\uparrow$	0.5		0.5		0.5	

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# SN54LV165A, SN74LV165A PARALLEL-LOAD 8-BIT SHIFT REGISTERS

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**switching characteristics over recommended operating free-air temperature range,  $V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$  (unless otherwise noted) (see Figure 1)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			SN54LV165A		SN74LV165A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
$f_{\text{max}}$			$C_L = 15\text{ pF}$	50*	80*		45*		45		MHz
			$C_L = 50\text{ pF}$	40	65		35		35		
$t_{\text{pd}}$	CLK	$Q_H$ or $\bar{Q}_H$	$C_L = 15\text{ pF}$		12.2*	19.8*	1*	22*	1	22	ns
	SH/ $\bar{\text{LD}}$				13.1*	21.5*	1*	23.5*	1	23.5	
	H				12.9*	21.7*	1*	24*	1	24	
$t_{\text{pd}}$	CLK	$Q_H$ or $\bar{Q}_H$	$C_L = 50\text{ pF}$		15.3	23.3	1	26	1	26	ns
	SH/ $\bar{\text{LD}}$				16.1	25.1	1	28	1	28	
	H				15.9	25.3	1	28	1	28	

\* On products compliant to MIL-PRF-38535, this parameter is not production tested.

**switching characteristics over recommended operating free-air temperature range,  $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$  (unless otherwise noted) (see Figure 1)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			SN54LV165A		SN74LV165A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
$f_{\text{max}}$			$C_L = 15\text{ pF}$	65*	115*		55*		55		MHz
			$C_L = 50\text{ pF}$	60	90		50		50		
$t_{\text{pd}}$	CLK	$Q_H$ or $\bar{Q}_H$	$C_L = 15\text{ pF}$		8.6*	15.4*	1*	18*	1	18	ns
	SH/ $\bar{\text{LD}}$				9.1*	15.8*	1*	18.5*	1	18.5	
	H				8.9*	14.1*	1*	16.5*	1	16.5	
$t_{\text{pd}}$	CLK	$Q_H$ or $\bar{Q}_H$	$C_L = 50\text{ pF}$		10.9	14.9	1	16.9	1	16.9	ns
	SH/ $\bar{\text{LD}}$				11.3	19.3	1	22	1	22	
	H				11.1	17.6	1	20	1	20	

\* On products compliant to MIL-PRF-38535, this parameter is not production tested.

**switching characteristics over recommended operating free-air temperature range,  $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$  (unless otherwise noted) (see Figure 1)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			SN54LV165A		SN74LV165A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
$f_{\text{max}}$			$C_L = 15\text{ pF}$	110*	165*		90*		90		MHz
			$C_L = 50\text{ pF}$	95	125		85		85		
$t_{\text{pd}}$	CLK	$Q_H$ or $\bar{Q}_H$	$C_L = 15\text{ pF}$		6*	9.9*	1*	11.5*	1	11.5	ns
	SH/ $\bar{\text{LD}}$				6*	9.9*	1*	11.5*	1	11.5	
	H				6*	9*	1*	10.5*	1	10.5	
$t_{\text{pd}}$	CLK	$Q_H$ or $\bar{Q}_H$	$C_L = 50\text{ pF}$		7.7	11.9	1	13.5	1	13.5	ns
	SH/ $\bar{\text{LD}}$				7.7	11.9	1	13.5	1	13.5	
	H				7.6	11	1	12.5	1	12.5	

\* On products compliant to MIL-PRF-38535, this parameter is not production tested.

**operating characteristics,  $T_A = 25^\circ\text{C}$**

PARAMETER	TEST CONDITIONS	$V_{CC}$	TYP	UNIT
$C_{\text{pd}}$ Power dissipation capacitance	$C_L = 50\text{ pF}$ , $f = 10\text{ MHz}$	3.3 V	36.1	pF
		5 V	37.5	

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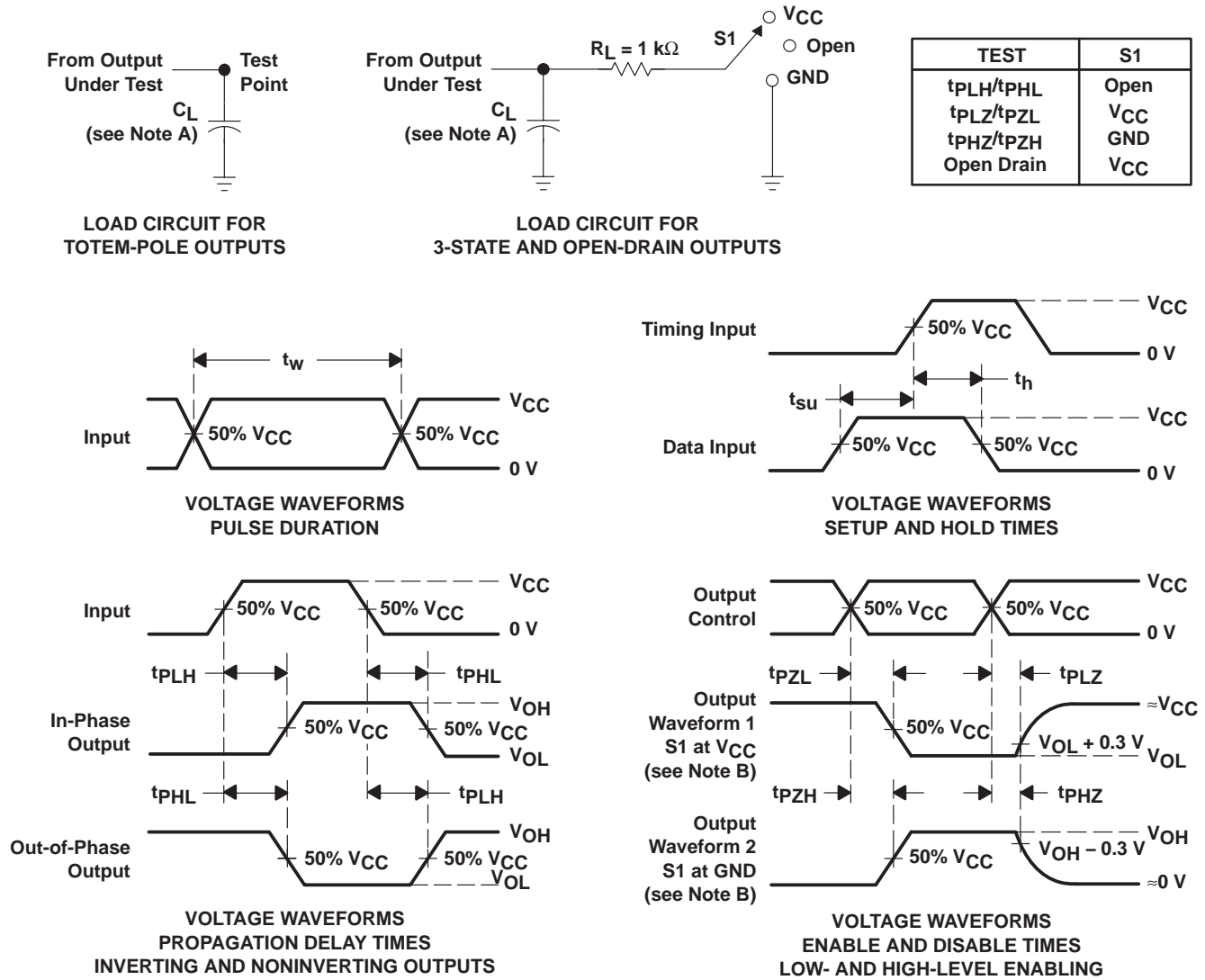


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## PARAMETER MEASUREMENT INFORMATION



- NOTES:
- A.  $C_L$  includes probe and jig capacitance.
  - B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
  - C. All input pulses are supplied by generators having the following characteristics: PRR  $\leq 1\text{ MHz}$ ,  $Z_O = 50\ \Omega$ ,  $t_r \leq 3\text{ ns}$ ,  $t_f \leq 3\text{ ns}$ .
  - D. The outputs are measured one at a time, with one input transition per measurement.
  - E.  $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
  - F.  $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .
  - G.  $t_{PHL}$  and  $t_{PLH}$  are the same as  $t_{pd}$ .
  - H. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
SN74LV165AD	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV165ADBR	ACTIVE	SSOP	DB	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV165ADBRE4	ACTIVE	SSOP	DB	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV165ADE4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV165ADGVR	ACTIVE	TVSOP	DGV	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV165ADGVRE4	ACTIVE	TVSOP	DGV	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV165ADR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV165ADRE4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV165ANSR	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV165ANSRE4	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV165APW	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV165APWE4	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV165APWG4	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV165APWR	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV165APWRE4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV165APWRG4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV165APWT	ACTIVE	TSSOP	PW	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV165APWTE4	ACTIVE	TSSOP	PW	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV165ARGYR	ACTIVE	QFN	RGY	16	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1YEAR
SN74LV165ARGYRG4	ACTIVE	QFN	RGY	16	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1YEAR

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBsolete:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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DGV (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE

24 PINS SHOWN

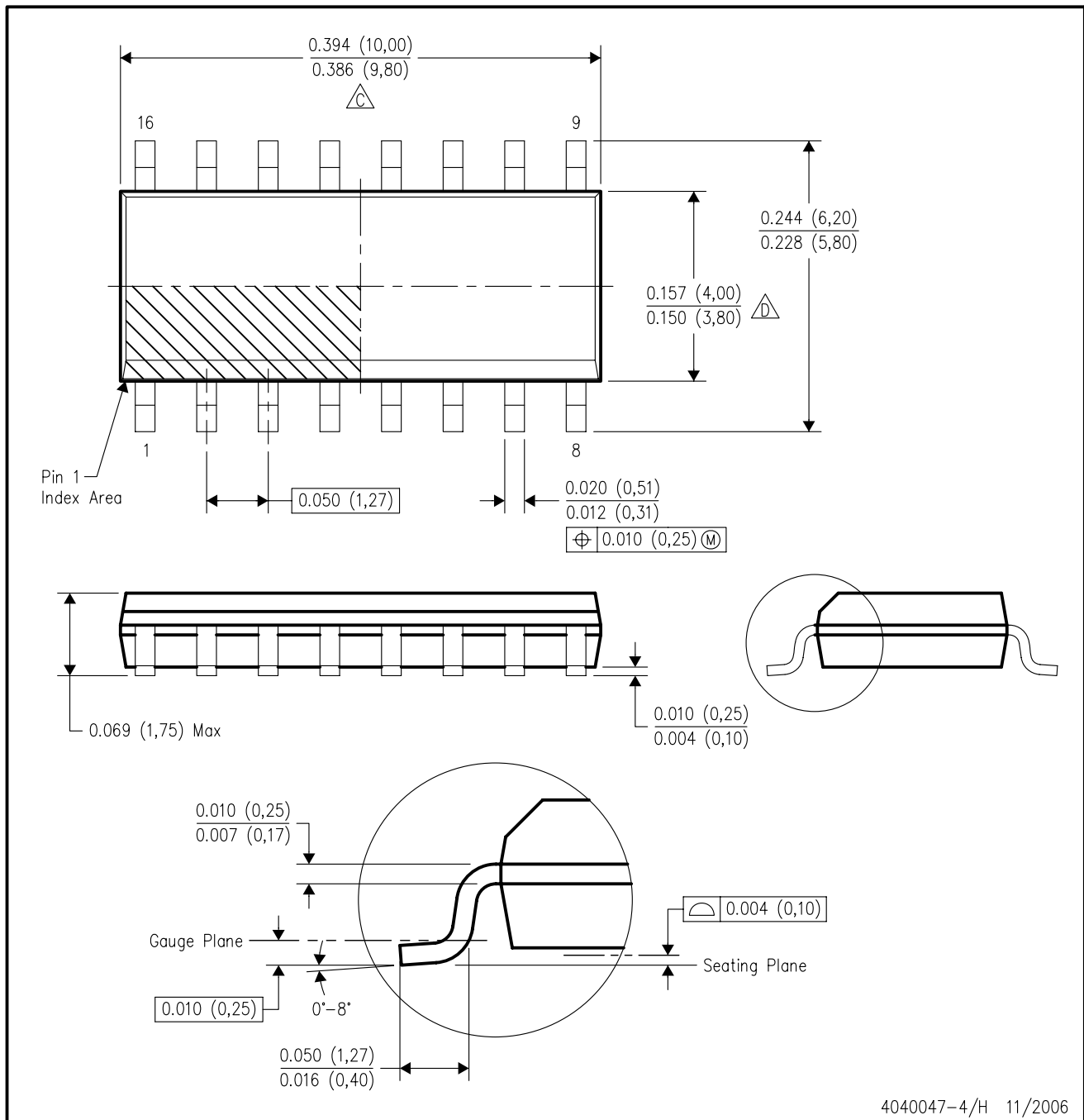


4073251/E 08/00

- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.  
 D. Falls within JEDEC: 24/48 Pins – MO-153  
 14/16/20/56 Pins – MO-194

D (R-PDSO-G16)

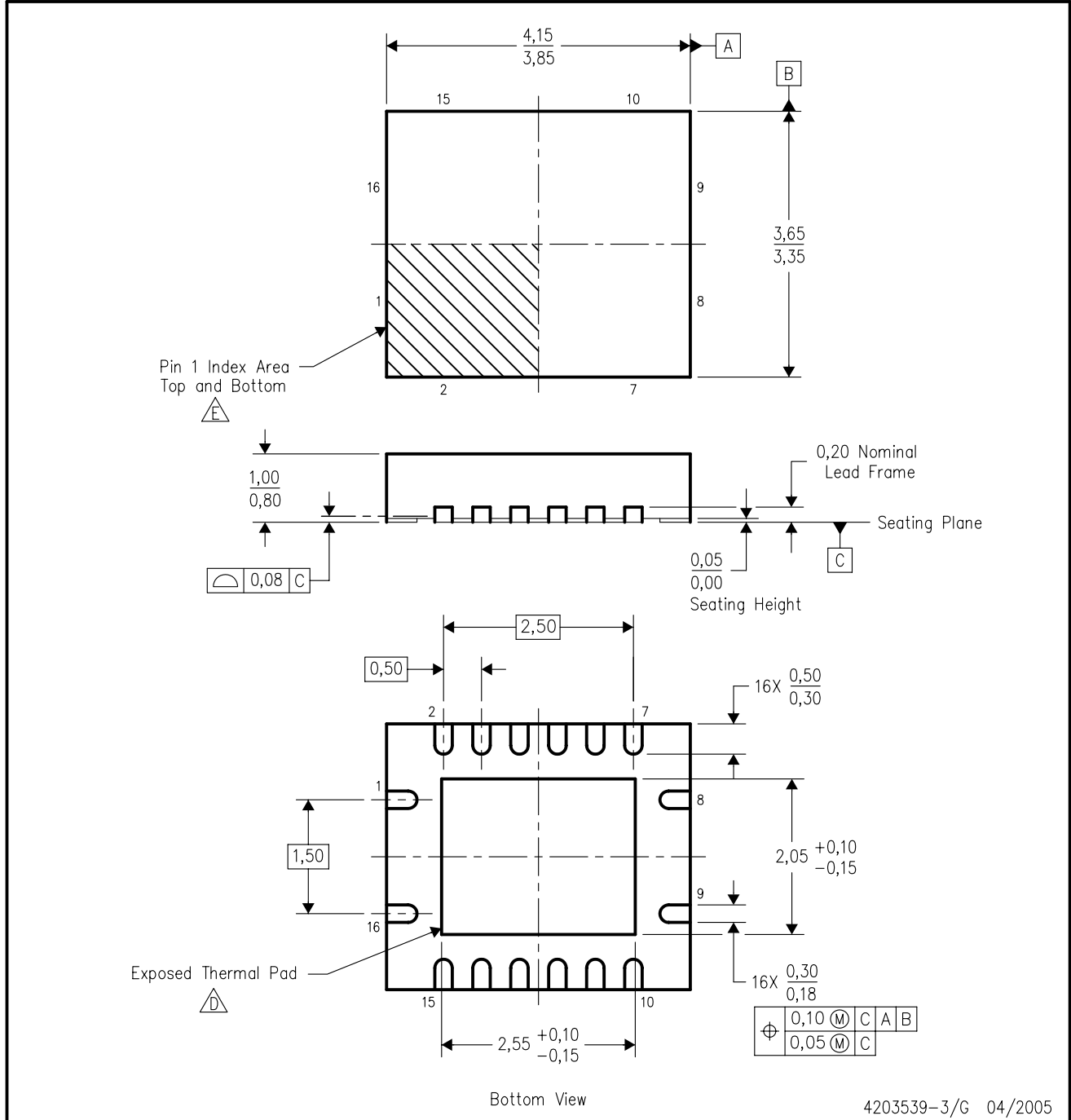
PLASTIC SMALL-OUTLINE PACKAGE





- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.
  - D. Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.
  - E. Reference JEDEC MS-012 variation AC.

RGY (R-PQFP-N16)

PLASTIC QUAD FLATPACK



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. QFN (Quad Flatpack No-Lead) package configuration.
  -  The package thermal pad must be soldered to the board for thermal and mechanical performance.
  -  Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated. The Pin 1 identifiers are either a molded, marked, or metal feature.
  - F. Package complies to JEDEC MO-241 variation BB.

# MECHANICAL DATA

NS (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

DB (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE

28 PINS SHOWN



4040065 /E 12/01

- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-150

PW (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN



4040064/F 01/97

- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-153

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DSP	<a href="http://dsp.ti.com">dsp.ti.com</a>	Broadband	<a href="http://www.ti.com/broadband">www.ti.com/broadband</a>
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