COUNTER 54/74LS293

4-Bit Binary Ripple Counter

DESCRIPTION

The '293 is a 4-bit ripple type binary counter. The device consists of four master-slave flip-flops internally connected to provide a divide-by-two section and a divide-by-eight section. Each section has a separate Clock input to initiate state changes of the counter on the HIGH-to-LOW clock transition. State changes of the Q outputs do not occur simultaneously because of internal ripple delays. Therefore, decoded output signals are subject to decoding spikes and should not be used for clocks or strobes.

A gated AND asynchronous Master Reset (MR_1 MR_2) is provided which overrides both clocks and resets (clears) all the flip-flops.

Since the output from the divide-by-two section is not internally connected to the succeeding stages, the device may be operated in various counting modes. In a 4-bit ripple counter the output Q_0 must be connected externally to input $\overline{CP}_1$. The input count pulses are applied to input $\overline{CP}_0$. Simultaneous divisions of 2, 4, 8 and 16 are performed at the Q_0, Q_1, Q_2 and Q_3 outputs as shown in the function table. As a 3-bit ripple counter the input count pulses are applied to input $\overline{CP}_1$. Simultaneous frequency divisions of 2, 4 and 8 are available at the Q_1, Q_2 and Q_3 outputs. Independent use of the first flip-flop is available if the reset function coincides with reset of the 3-bit ripple-through counter.

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (Total)
74LS293	42MHz	9mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGES V_{CC} = 5V ± 5%; T_A = 0°C to + 70°C	MILITARY RANGES V_{CC} = 5V ± 10%; T_A = −55°C to + 125°C
Plastic DIP	N74LS293N	
Plastic SO	N74LS293D	
Ceramic DIP		S54LS293F
Flatpack		S54LS293W

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	54/74LS
MR	Inputs	1LSul
$\overline{CP}_0$	Input	6LSul
$\overline{CP}_1$	Input	4LSul
All	Outputs	10LSul

NOTE
A 54/74LS unit load (LSul) is 20μA I_{IH} and − 0.4mA I_{IL}.

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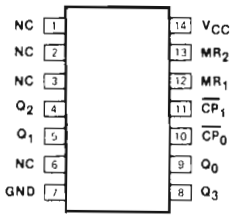
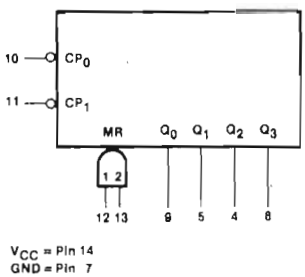
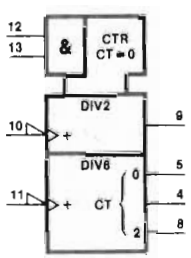
PIN CONFIGURATION



LOGIC SYMBOL

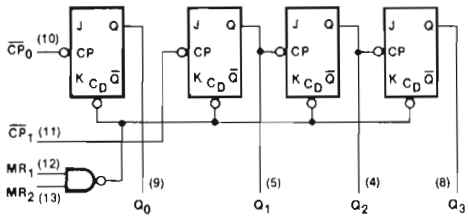


LOGIC SYMBOL (IEEE/IEC)



COUNTER 54/74LS293

LOGIC DIAGRAM



( ) = Pin numbers
V_{CC} = Pin 14
GND = Pin 7

MODE SELECTION

RESET INPUTS		OUTPUTS			
MR_1	MR_2	Q_0	Q_1	Q_2	Q_3
H	H	L	L	L	L
L	H	Count			
H	L	Count			
L	L	Count			

H = HIGH voltage level
L = LOW voltage level
X = Don t care

FUNCTION TABLE

COUNT	OUTPUTS			
	Q_0	Q_1	Q_2	Q_3
0	L	L	L	L
1	H	L	L	L
2	L	H	L	L
3	H	H	L	L
4	L	L	H	L
5	H	L	H	L
6	L	H	H	L
7	H	H	H	L
8	L	L	L	H
9	H	L	L	H
10	L	H	L	H
11	H	H	L	H
12	L	L	H	H
13	H	L	H	H
14	L	H	H	H
15	H	H	H	H

NOTE
Output Q_0 connected to input $\overline{CP}_1$.

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

	PARAMETER	54LS	74LS	UNIT
V_{CC}	Supply voltage	7.0	7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +1	−30 to +1	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +V_{CC}	−0.5 to +V_{CC}	V
T_A	Operating free-air temperature range	−55 to +125	0 to 70	°C

NOTE
V_{IN} limited to 5.5V on $\overline{CP}_0$ and $\overline{CP}_1$ inputs.

COUNTER 54/74LS293

RECOMMENDED OPERATING CONDITIONS

PARAMETER			54/74LS			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage	Mil	4.5	5.0	5.5	V
		Com'l	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage		2.0			V
V_{IL}	LOW-level input voltage	Mil			+0.7	V
		Com'l			+0.8	V
I_{IK}	Input clamp current				−18	mA
I_{OH}	HIGH-level output current				−400	μA
I_{OL}	LOW-level output current	Mil			4	mA
		Com'l			8	mA
T_A	Operating free-air temperature	Mil	−55		+125	°C
		Com'l	0		70	°C

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DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER		TEST CONDITIONS[1]			54/74LS293			UNIT
					Min	Typ[2]	Max	
V_{OH}	HIGH-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX, I_{OH} = MAX		Mil	2.5	3.4		V
				Com'l	2.7	3.4		V
V_{OL}	LOW-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX	I_{OL} = MAX	Mil		0.25	0.4	V
				Com'l		0.35	0.5	V
			I_{OL} = 4mA	74LS		0.25	0.4	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}					−1.5	V
I_I	Input current at maximum input voltage	V_{CC} = MAX	V_I = 7.0V	MR inputs			0.1	mA
			V_I = 5.5V	$\overline{CP}$ inputs			0.2	mA
I_{IH}	HIGH-level input current	V_{CC} = MAX, V_I = 2.7V		MR inputs			20	μA
				$\overline{CP}$ inputs[5]			40	μA
I_{IL}	LOW-level input current	V_{CC} = MAX, V_I = 0.4V		MR inputs			−0.4	mA
				$\overline{CP}_0$ input			−2.4	mA
				$\overline{CP}_1$ input			−1.6	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX			−20		−100	mA
I_{CC}	Supply current[4] (total)	V_{CC} = MAX				9	15	mA

NOTES
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. I_{OS} is tested with V_{OUT} = +0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
4. Measure I_{CC} with Clock inputs grounded, all outputs open, both MR inputs grounded following momentary connection to 4.5V
5. The maximum limit for the 54LS293 is 80μA for $\overline{CP}_0$ and $\overline{CP}_1$ inputs.

AC CHARACTERISTICS $T_A = 25°C$, $V_{CC} = 5.0V$

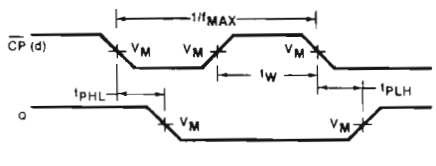
PARAMETER		TEST CONDITIONS	54LS/74LS $C_L = 15pF$, $R_L = 2k\Omega$		UNIT
			Min	Max	
f_{MAX}	$\overline{CP}_0$ input count frequency	Waveform 1	32		MHz
f_{MAX}	$\overline{CP}_1$ input count frequency	Waveform 1	16		MHz
t_{PLH} t_{PHL}	Propagation delay $\overline{CP}_0$ input to Q_0 output	Waveform 1		16 18	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{CP}_1$ input to Q_1 output	Waveform 1		16 21	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{CP}_1$ input to Q_2 output	Waveform 1		32 35	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{CP}_1$ input to Q_3 output	Waveform 1		51 51	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{CP}_0$ input to Q_3 output	Waveform 1		70 70	ns
t_{PHL}	MR input to any output	Waveform 2		40	ns

NOTE
Per industry convention, f_{MAX} is the worst case value of the maximum device operating frequency with no constraints on t_r, t_f, pulse width or duty cycle.

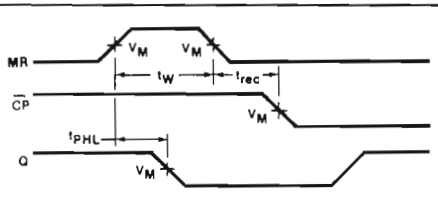
AC SETUP REQUIREMENTS $T_A = 25°C$, $V_{CC} = 5.0V$

PARAMETER		TEST CONDITIONS	54LS/74LS		UNIT
			Min	Max	
t_W	$\overline{CP}_0$ pulse width	Waveform 1	15		ns
t_W	$\overline{CP}_1$ pulse width	Waveform 1	30		ns
t_W	MR pulse width	Waveform 2	15		ns
t_{rec}	Recovery time, MR to $\overline{CP}$	Waveform 2	25		ns

AC WAVEFORMS



Waveform 1



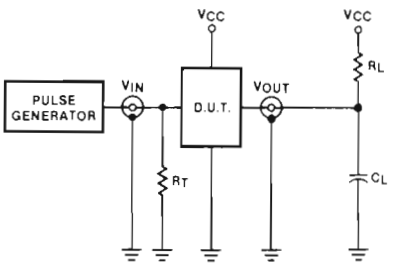
Waveform 2

V_M = 1.5V for 54/74 and 54S/74S, V_M = 1.3V for 54LS/74LS.

The number of Clock Pulses required between the t_{PLH} and t_{PHL} measurements can be determined from the appropriate Truth Table

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUIT FOR 54/74 OPEN COLLECTOR OUTPUTS



DEFINITIONS

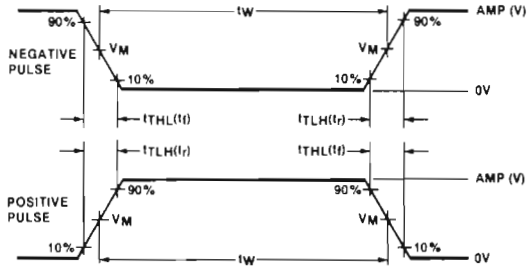
R_L = Load resistor to V_{CC}, see AC CHARACTERISTICS for value

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.

t_{TLH}, t_{THL} Values should be less than or equal to the table entries.

INPUT PULSE DEFINITIONS



V_M = 1.3V for 54LS/74LS; V_M = 1.5V for all other TTL families.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54/74	3.0V	1MHz	500ns	7ns	7ns
54LS/74LS	3.0V	1MHz	500ns	15ns	6ns
54S/74S	3.0V	1MHz	500ns	2.5ns	2.5ns