FLIP-FLOPS

54/74174, LS174, S174

Hex D Flip-Flops

- **Six edge-triggered D-type flip-flops**
- **Three speed-power ranges available**
- **Buffered common clock**
- **Buffered, asynchronous Master Reset**

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (Total)
74174	35MHz	45mA
74LS174	40MHz	16mA
74S174	110MHz	90mA

DESCRIPTION

The '174 has six edge-triggered D-type flip-flops with individual D inputs and Q outputs. The common buffered Clock (CP) and Master Reset ($\overline{MR}$) inputs load and reset (clear) all flip-flops simultaneously.

The register is fully edge triggered. The state of each D input, one setup time before the LOW-to-HIGH clock transition, is transferred to the corresponding flip-flop's Q output.

All outputs will be forced LOW independently of Clock or Data inputs by a LOW voltage level on the $\overline{MR}$ input. The device is useful for applications where the true output only is required and the Clock and Master Reset are common to all storage elements.

ORDERING CODE

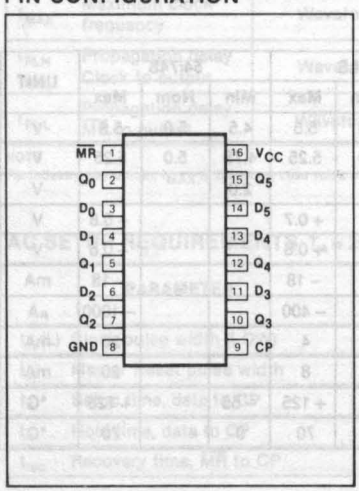
PACKAGES	COMMERCIAL RANGES V_{CC} = 5V ± 5%; T_A = 0°C to +70°C	MILITARY RANGES V_{CC} = 5V ± 10%; T_A = −55°C to +125°C
Plastic DIP	N74174N • N74LS174N N74S174N	
Plastic SO	N74LS174D N74S174D	
Ceramic DIP		S54174F • S54LS174F S54S174F
Flatpack		S54174W • S54LS174W S54S174W
LLCC		S54S174G • S54LS174G

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

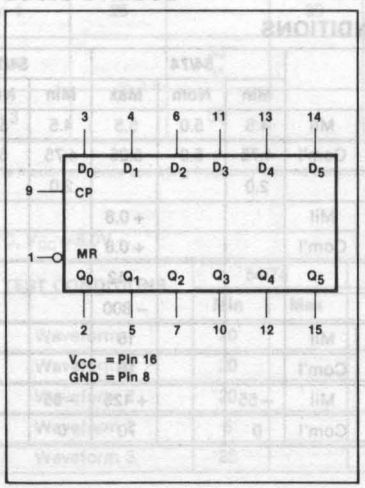
PINS	DESCRIPTION	54/74	54/74S	54/74LS
All	Inputs	1ul	1Sul	1LSul
Q_0–Q_5	Outputs	10ul	10Sul	10LSul

NOTE
Where a 54/74 unit load (ul) is understood to be 40μA I_{IH} and −1.6mA I_{IL}, a 54/74S unit load (Sul) is 50μA I_{IH} and −2.0mA I_{IL}, and 54/74LS unit load (LSul) is 20μA I_{IH} and −0.4mA I_{IL}.

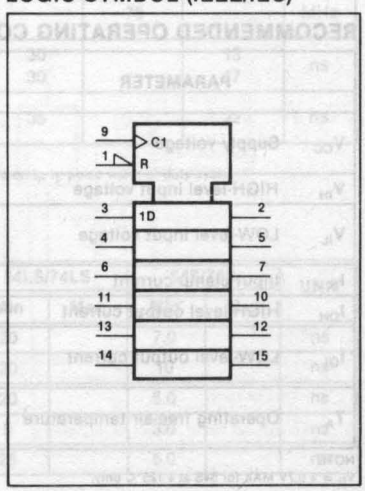
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



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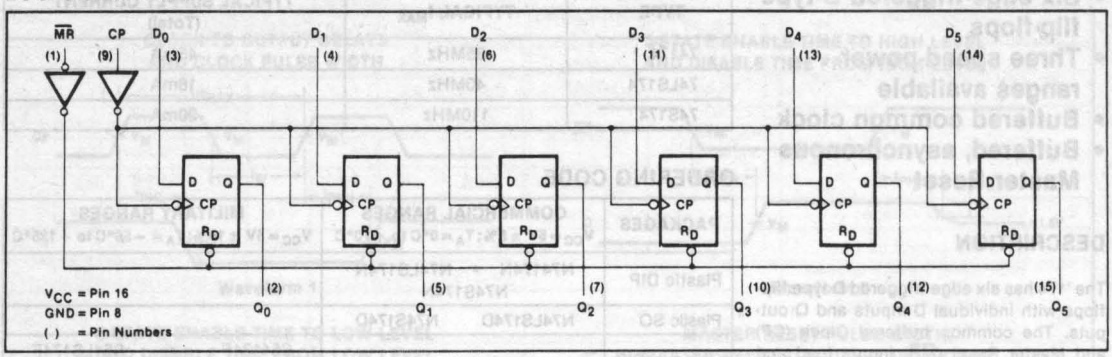
LOGIC DIAGRAM



FUNCTION TABLE

OPERATING MODE	INPUTS			OUTPUTS
	$\overline{MR}$	CP	D_n	Q_n
Reset (clear)	L	X	X	L
Load "1"	H	↑	h	H
Load "0"	H	↑	l	L

H = HIGH voltage level steady state
h = HIGH voltage level one setup time prior to the LOW-to-HIGH clock transition.
L = LOW voltage level steady state.
l = LOW voltage level one setup time prior to the LOW-to-HIGH clock transition.
X = Don't care.
↑ = LOW-to-HIGH clock transition.

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER		54	54LS	54S	74	74LS	74S	UNIT
V_{CC}	Supply voltage	7.0	7.0	7.0	7.0	7.0	7.0	V
V_{IN}	Input voltage	−0.5 to +5.5	−0.5 to +7.0	−0.5 to +5.5	−0.5 to +5.5	−0.5 to +7.0	−0.5 to +5.5	V
I_{IN}	Input current	−30 to +5	−30 to +1	−30 to +5	−30 to +5	−30 to +1	−30 to +5	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +V_{CC}	−0.5 to +V_{CC}	−0.5 to +V_{CC}	−0.5 to +V_{CC}	−0.5 to +V_{CC}	−0.5 to +V_{CC}	V
T_A	Operating free-air temperature range	−55 to +125			0 to 70			°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER			54/74			54/74LS			54/74S			UNIT
			Min	Nom	Max	Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply voltage	Mil	4.5	5.0	5.5	4.5	5.0	5.5	4.5	5.0	5.5	V
		Com'l	4.75	5.0	5.25	4.75	5.0	5.25	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage		2.0			2.0			2.0			V
V_{IL}	LOW-level input voltage	Mil			+0.8			+0.7			+0.8	V
		Com'l			+0.8			+0.8			+0.8	V
I_{IK}	Input clamp current				−12			−18			−18	mA
I_{OH}	HIGH-level output current				−800			−400			−1000	μA
I_{OL}	LOW-level output current	Mil			16			4			20	mA
		Com'l			16			8			20	mA
T_A	Operating free-air temperature	Mil	−55		+125	−55		+125	−55		+125	°C
		Com'l	0		70	0		70	0		70	°C

NOTE
V_{IL} = +0.7V MAX for 54S at +125°C only.

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER		TEST CONDITIONS[1]			54/74174			54/74LS174			54/74S174			UNIT
					Min	Typ[2]	Max	Min	Typ[2]	Max	Min	Typ[2]	Max	
V_{OH}	HIGH-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX, I_{OH} = MAX		Mil	2.4	3.4		2.5	3.4		2.5	3.4		V
				Com'l	2.4	3.4		2.7	3.4		2.7	3.4		V
V_{OL}	LOW-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX	I_{OL} = MAX	Mil		0.2	0.4		0.25	0.4			0.5[5]	V
				Com'l		0.2	0.4		0.35	0.5			0.5	V
			I_{OL} = 4mA	74LS					0.25	0.4				V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}					– 1.5			– 1.5			– 1.2	V
I_I	Input current at maximum input voltage	V_{CC} = MAX	V_I = 5.5V				1.0						1.0	mA
			V_I = 7.0V							0.1				mA
I_{IH}	HIGH-level input current	V_{CC} = MAX	V_I = 2.4V				40							μA
			V_I = 2.7V							20			50	μA
I_{IL}	LOW-level input current	V_{CC} = MAX	V_I = 0.4V				– 1.6			– 0.4				mA
			V_I = 0.5V										– 2.0	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX		Mil	– 20		– 57	– 20		– 100	– 40		– 100	mA
				Com'l	– 18		– 57	– 20		– 100	– 40		– 100	mA
I_{CC}	Supply current[4] (total)	V_{CC} = MAX				45	65		16	26		90	144	mA

NOTES
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. I_{OS} is tested with V_{OUT} = + 0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
4. I_{CC} is measured after a momentary ground, then 4.5V is applied to Clock, with 4.5V applied to all Data and $\overline{MR}$ inputs and all outputs open.
5. V_{OL} = + 0.45V MAX for 54S at + 125°C only.

AC CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

PARAMETER		TEST CONDITIONS	54/74		54LS/74LS		54S/74S		UNIT
			C_L = 15pF, R_L = 400Ω		C_L = 15pF, R_L = 2kΩ		C_L = 15pF, R_L = 280Ω		
			Min	Max	Min	Max	Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1	25		30		75		MHz
t_{PLH} t_{PHL}	Propagation delay Clock to output	Waveform 1		30 35		30 30		13 17	ns
t_{PHL}	Propagation delay $\overline{MR}$ to output	Waveform 3		35		35		22	ns

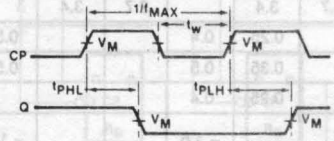
NOTE
Per industry convention, f_{MAX} is the worst case value of the maximum device operating frequency with no constraints on t_r, t_f, pulse width or duty cycle.

AC SETUP REQUIREMENTS T_A = 25°C, V_{CC} = 5.0V

PARAMETER		TEST CONDITIONS	54/74		54LS/74LS		54S/74S		UNIT
			Min	Max	Min	Max	Min	Max	
t_W(L)	Clock pulse width (LOW)	Waveform 1	20		20		7.0		ns
t_W	Master Reset pulse width	Waveform 3	20		20		10		ns
t_s	Setup time, data to CP	Waveform 2	20		20		5.0		ns
t_h	Hold time, data to CP	Waveform 2	5		5		3.0		ns
t_{rec}	Recovery time, $\overline{MR}$ to CP	Waveform 3	25		25		5.0		ns

AC WAVEFORMS

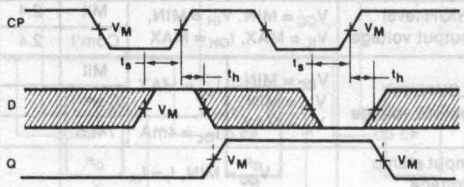
CLOCK TO OUTPUT DELAYS AND CLOCK PULSE WIDTH



V_M = 1.5V for 54/74 and 54S/74S, V_M = 1.3V for 54LS/74LS.

Waveform 1

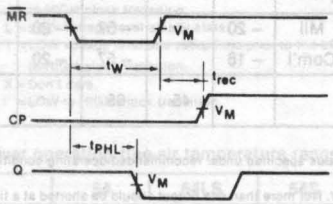
DATA SET-UP AND HOLD TIMES



V_M = 1.5V for 54/74 and 54S/74S, V_M = 1.3V for 54LS/74LS.
The shaded areas indicate when the input is permitted to change for predictable output performance

Waveform 2

MASTER RESET TO OUTPUT DELAY, MASTER RESET PULSE WIDTH, AND MASTER RESET RECOVERY TIME

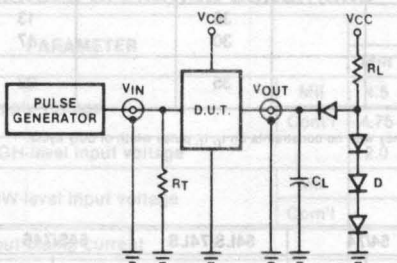


V_M = 1.5V for 54/74 and 54S/74S, V_M = 1.3V for 54LS/74LS.

Waveform 3

TEST CIRCUITS AND WAVEFORMS

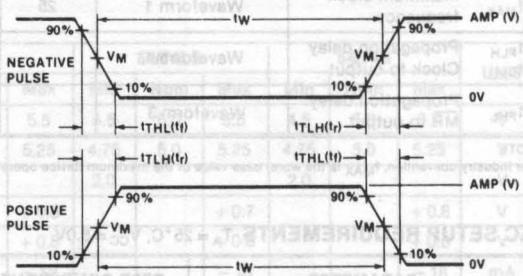
TEST CIRCUIT FOR 54/74 TOTEM-POLE OUTPUTS



DEFINITIONS

R_L = Load resistor to V_{CC}; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
D = Diodes are 1N916, 1N3064, or equivalent.
t_{TLH}, t_{THL} Values should be less than or equal to the table entries.

INPUT PULSE DEFINITIONS



V_M = 1.3V for 54LS/74LS; V_M = 1.5V for all other TTL families.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54/74	3.0V	1MHz	500ns	7ns	7ns
54LS/74LS	3.0V	1MHz	500ns	15ns	6ns
54S/74S	3.0V	1MHz	500ns	2.5ns	2.5ns