

# CS51411, CS51412, CS51413, CS51414

## 1.5 A, 260 kHz and 520 kHz, Low Voltage Buck Regulators with External Bias or Synchronization Capability

The CS5141X products are 1.5 A buck regulator ICs. These devices are fixed-frequency operating at 260 kHz and 520 kHz. The regulators use the  $V^2$ ™ control architecture to provide unmatched transient response, the best overall regulation and the simplest loop compensation for today's high-speed logic. These products accommodate input voltages from 4.5 V to 40 V.

The CS51411 and CS51413 contain synchronization circuitry. The CS51412 and CS51414 have the option of powering the controller from an external 3.3 V to 6.0 V supply in order to improve efficiency, especially in high input voltage, light load conditions.

The on-chip NPN transistor is capable of providing a minimum of 1.5 A of output current, and is biased by an external "boost" capacitor to ensure saturation, thus minimizing on-chip power dissipation. Protection circuitry includes thermal shutdown, cycle-by-cycle current limiting and frequency foldback. The CS51411 and CS51413 are functionally pin-compatible with the LT1375. The CS51412 and CS51414 are functionally pin-compatible with the LT1376.

### Features

- $V^2$  Architecture Provides Ultrafast Transient Response, Improved Regulation and Simplified Design
- 2.0% Error Amp Reference Voltage Tolerance
- Switch Frequency Decrease of 4:1 in Short Circuit Conditions Reduces Short Circuit Power Dissipation
- BOOST Lead Allows "Bootstrapped" Operation to Maximize Efficiency
- Sync Function for Parallel Supply Operation or Noise Minimization
- Shutdown Lead Provides Power-Down Option
- 85  $\mu$ A Quiescent Current During Power-Down
- Thermal Shutdown
- Soft-Start
- Pin-Compatible with LT1375 and LT1376
- Pb-Free Packages are Available



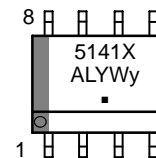
ON Semiconductor®

<http://onsemi.com>



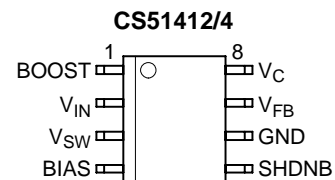
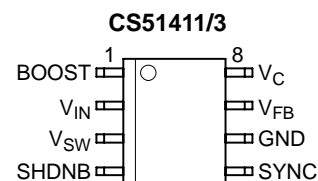
SOIC-8  
D SUFFIX  
CASE 751

### MARKING DIAGRAM



5141x = Device Code  
x = 1, 2, 3 or 4  
A = Assembly Location  
L = Wafer Lot  
Y = Year  
W = Work Week  
y = E or G  
▪ = Pb-Free Package

### PIN CONNECTIONS



### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 15 of this data sheet.

# CS51411, CS51412, CS51413, CS51414

## PRODUCT SELECTION GUIDE+

Part Number	Frequency	Temperature Range	Bias/Sync
CS51411E	260 kHz	-40°C to 85°C	Sync
CS51411G	260 kHz	0°C to 70°C	Sync
CS51412E	260 kHz	-40°C to 85°C	Bias
CS51412G	260 kHz	0°C to 70°C	Bias
CS51413E	520 kHz	-40°C to 85°C	Sync
CS51413G	520 kHz	0°C to 70°C	Sync
CS51414E	520 kHz	-40°C to 85°C	Bias
CS51414G	520 kHz	0°C to 70°C	Bias

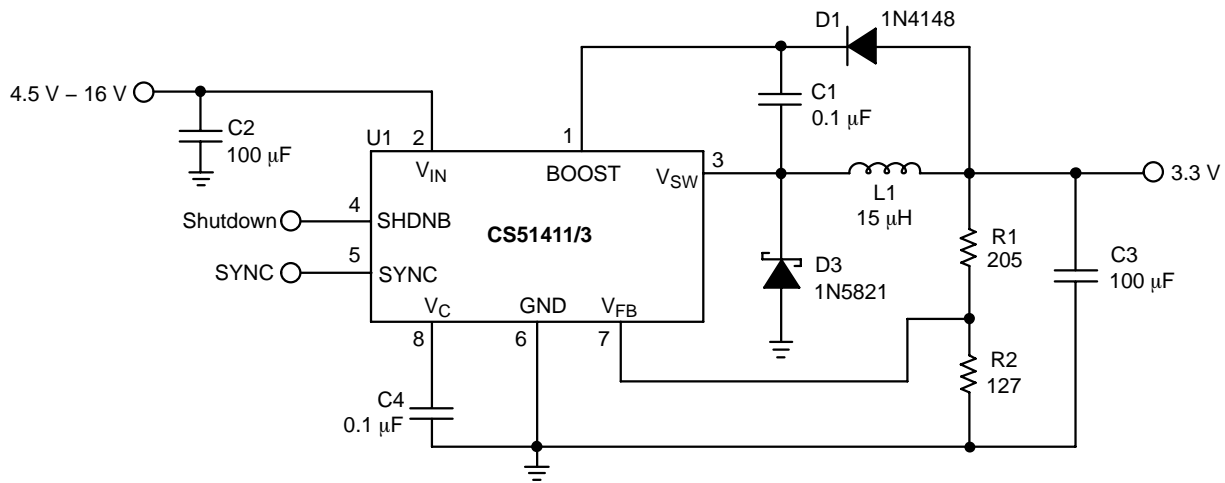


Figure 1. Application Diagram, 4.5 V – 16 V to 3.3 V @ 1.0 A Converter

## MAXIMUM RATINGS

Rating	Value	Unit
Operating Junction Temperature Range, $T_J$	-40 to 150	°C
Lead Temperature Soldering: Reflow: (SMD styles only) (Note 1)	230 peak	°C
Storage Temperature Range, $T_S$	-65 to +150	°C
ESD Damage Threshold (Human Body Model)	2.0	kV

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

1. 60 second maximum above 183°C.

# CS51411, CS51412, CS51413, CS51414

## MAXIMUM RATINGS

Pin Name	V <sub>Max</sub>	V <sub>MIN</sub>	I <sub>SOURCE</sub>	I <sub>SINK</sub>
V <sub>IN</sub>	40 V	-0.3 V	N/A	4.0 A
BOOST	40 V	-0.3 V	N/A	100 mA
V <sub>SW</sub>	40 V	-0.6 V/-1.0 V, t < 50 ns	4.0 A	10 mA
V <sub>C</sub>	7.0 V	-0.3 V	1.0 mA	1.0 mA
SHDNB	7.0 V	-0.3 V	1.0 mA	1.0 mA
SYNC	7.0 V	-0.3 V	1.0 mA	1.0 mA
BIAS	7.0 V	-0.3 V	1.0 mA	50 mA
V <sub>FB</sub>	7.0 V	-0.3 V	1.0 mA	1.0 mA
GND	7.0 V	-0.3 V	50 mA	1.0 mA

**ELECTRICAL CHARACTERISTICS** (-40°C < T<sub>J</sub> < 125°C (CS51411E/2E/3E/4E); -40°C < T<sub>A</sub> < 85°C (CS51411E/2E/3E/4E); 0°C < T<sub>A</sub> < 70°C (CS51411G/2G/3G/4G), 4.5 V < V<sub>IN</sub> < 40 V; unless otherwise specified.)

Characteristic	Test Conditions	Min	Typ	Max	Unit
----------------	-----------------	-----	-----	-----	------

### Oscillator

Operating Frequency	CS51411/CS51412	224	260	296	kHz
Operating Frequency	CS51413/CS51414	446	520	594	kHz
Frequency Line Regulation	-	-	0.05	0.15	%/V
Maximum Duty Cycle	-	85	90	95	%
V <sub>FB</sub> Frequency Foldback Threshold	-	0.29	0.32	0.36	V

### PWM Comparator

Slope Compensation Voltage	CS51411/CS51412, Fix V <sub>FB</sub> , ΔV <sub>C</sub> /ΔT <sub>ON</sub> CS51413/CS51414	8.0 25	17 50	26 75	mV/μs mV/μs
Minimum Output Pulse Width	CS51411/CS51412, V <sub>FB</sub> to V <sub>SW</sub> CS51413/CS51414, V <sub>FB</sub> to V <sub>SW</sub>	- -	150 -	300 230	ns ns

### Power Switch

Current Limit	V <sub>FB</sub> > 0.36 V	1.6	2.3	3.0	A
Foldback Current	V <sub>FB</sub> < 0.29 V	0.9	1.5	2.1	A
Saturation Voltage	I <sub>OUT</sub> = 1.5 A, V <sub>BOOST</sub> = V <sub>IN</sub> + 2.5 V	0.4	0.7	1.0	V
Current Limit Delay	(Note 2)	-	120	160	ns

### Error Amplifier

Internal Reference Voltage	-	1.244	1.270	1.296	V
Reference PSRR	(Note 2)	-	40	-	dB
FB Input Bias Current	-	-	0.02	0.1	μA
Output Source Current	V <sub>C</sub> = 1.270 V, V <sub>FB</sub> = 1.0 V	15	25	35	μA
Output Sink Current	V <sub>C</sub> = 1.270 V, V <sub>FB</sub> = 2.0 V	15	25	35	μA
Output High Voltage	V <sub>FB</sub> = 1.0 V	1.39	1.46	1.53	V
Output Low Voltage	V <sub>FB</sub> = 2.0 V	5.0	20	60	mV
Unity Gain Bandwidth	(Note 2)	-	500	-	kHz
Open Loop Amplifier Gain	(Note 2)	-	70	-	dB
Amplifier Transconductance	(Note 2)	-	6.4	-	mA/V

2. Guaranteed by design, not 100% tested in production.

# CS51411, CS51412, CS51413, CS51414

**ELECTRICAL CHARACTERISTICS** ( $-40^{\circ}\text{C} < T_J < 125^{\circ}\text{C}$  (CS51411E/2E/3E/4E);  $-40^{\circ}\text{C} < T_A < 85^{\circ}\text{C}$  (CS51411E/2E/3E/4E);  $0^{\circ}\text{C} < T_A < 70^{\circ}\text{C}$  (CS51411G/2G/3G/4G),  $4.5\text{ V} < V_{IN} < 40\text{ V}$ ; unless otherwise specified.)

Characteristic	Test Conditions	Min	Typ	Max	Unit
<b>Sync</b>					
Sync Frequency Range	CS51411/CS51412	305	–	470	kHz
Sync Frequency Range	CS51413/CS51414	575	–	880	kHz
Sync Pin Bias Current	$V_{SYNC} = 0\text{ V}$ $V_{SYNC} = 5.0\text{ V}$	– 250	0.1 360	0.2 460	$\mu\text{A}$ $\mu\text{A}$
Sync Threshold Voltage	–	1.0	1.5	1.9	V

## Shutdown

Shutdown Threshold Voltage	–	1.0	1.3	1.6	V
Shutdown Pin Bias Current	$V_{SHDNB} = 0\text{ V}$	0.14	5.00	35	$\mu\text{A}$

## Thermal Shutdown

Overtemperature Trip Point	(Note 3)	175	185	195	$^{\circ}\text{C}$
Thermal Shutdown Hysteresis	(Note 3)	–	42	–	$^{\circ}\text{C}$

## General

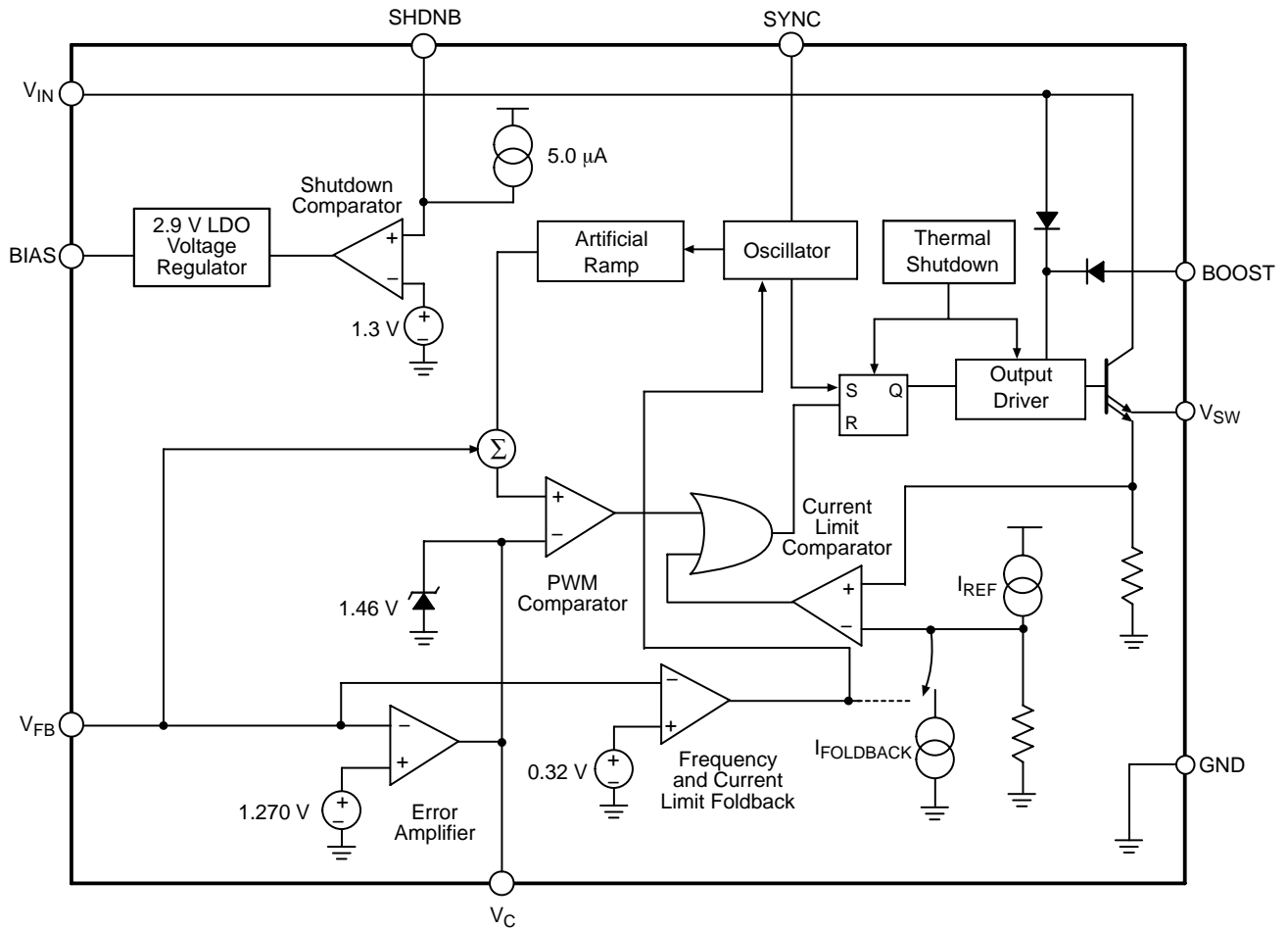
Quiescent Current	$I_{SW} = 0\text{ A}$	3.0	4.0	6.25	mA
Shutdown Quiescent Current	$V_{SHDNB} = 0\text{ V}$	8.0	20	85	$\mu\text{A}$
Boost Operating Current	$V_{BOOST} - V_{SW} = 2.5\text{ V}$	6.0	15	40	mA/A
Minimum Boost Voltage	(Note 3)	–	–	2.5	V
Startup Voltage	–	2.2	3.3	4.4	V
Minimum Output Current	–	–	7.0	12	mA

3. Guaranteed by design, not 100% tested in production.

## PACKAGE PIN DESCRIPTION

Package Pin #	Pin Symbol	Function
1	BOOST	The BOOST pin provides additional drive voltage to the on-chip NPN power transistor. The resulting decrease in switch on voltage increases efficiency.
2	$V_{IN}$	This pin is the main power input to the IC.
3	$V_{SW}$	This is the connection to the emitter of the on-chip NPN power transistor and serves as the switch output to the inductor. This pin may be subjected to negative voltages during switch off-time. A catch diode is required to clamp the pin voltage in normal operation. This node can stand $-1.0\text{ V}$ for less than 50 ns during switch node flyback.
4 (CS51412/CS51414)	BIAS	The BIAS pin connects to the on-chip power rail and allows the IC to run most of its internal circuitry from the regulated output or another low voltage supply to improve efficiency. The BIAS pin is left floating if this feature is not used.
5 (CS51411/CS51413)	SYNC	This pin provides the synchronization input.
5 (CS51412/CS51414) 4 (CS51411/CS51413)	SHDNB	The shutdown pin is active low and TTL compatible. The IC goes into sleep mode, drawing less than $85\text{ }\mu\text{A}$ when the pin voltage is pulled below 1.0 V. This pin should be left floating in normal position.
6	GND	Power return connection for the IC.
7	$V_{FB}$	The FB pin provides input to the inverting input of the error amplifier. If $V_{FB}$ is lower than 0.29 V, the oscillator frequency is divided by four, and current limit folds back to about 1 A. These features protect the IC under severe overcurrent or short circuit conditions.
8	$V_C$	The $V_C$ pin provides a connection point to the output of the error amplifier and input to the PWM comparator. Driving of this pin should be avoided because on-chip test circuitry becomes active whenever current exceeding 0.5 mA is forced into the IC.

**CS51411, CS51412, CS51413, CS51414**



**Figure 2. Block Diagram**

APPLICATIONS INFORMATION

THEORY OF OPERATION

V<sup>2</sup> Control

The CS5141X family of buck regulators provides leading edge technology, a high level of integration and high operating frequencies allowing the layout of a switchmode power supply in a very small board area. These devices are based on the proprietary V<sup>2</sup> control architecture. V<sup>2</sup> control uses the output voltage and its ripple as the ramp signal, providing an ease of use not generally associated with voltage or current mode control. Improved line regulation, load regulation and very fast transient response are also major advantages.

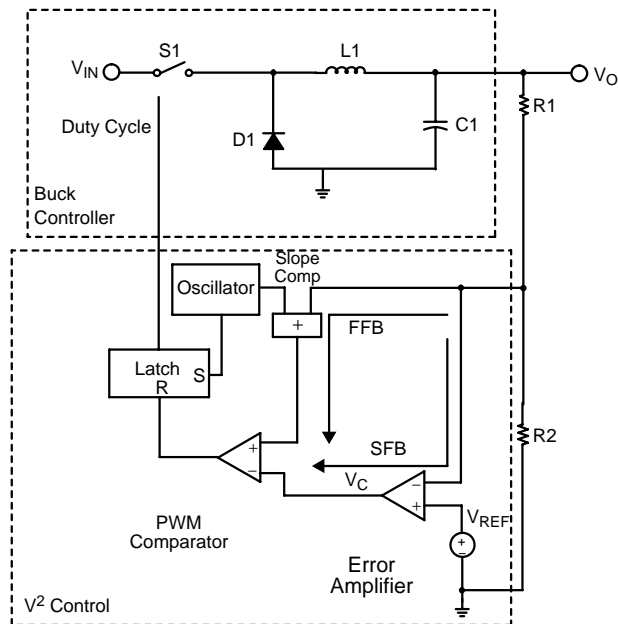


Figure 3. Buck Converter with V<sup>2</sup> Control

As shown in Figure 3, there are two voltage feedback paths in V<sup>2</sup> control, namely Fast Feedback (FFB) and Slow Feedback (SFB). In FFB path, the feedback voltage connects directly to the PWM comparator. This feedback path carries the ramp signal as well as the output DC voltage. Artificial ramp derived from oscillator is added to the feedback signal to improve stability. The other feedback path SFB connects the feedback voltage to the error amplifier whose output V<sub>C</sub> feeds to the other input of the PWM comparator. In a constant frequency mode, the oscillator signal sets the output latch and turns on the switch S1. This starts a new switch cycle. The ramp signal, composed of both artificial ramp and output ripple, eventually comes across the V<sub>C</sub> voltage, and consequently resets the latch to turn off the switch. The switch S1 will turn on again at the beginning of the next switch cycle. In a buck converter, the output ripple is determined by the ripple current of the inductor L1 and the ESR (equivalent series resistor) of the output capacitor C1.

The slope compensation signal is a fixed voltage ramp provided by the oscillator. Adding this signal eliminates subharmonic oscillation associated with the operation at duty cycle greater than 50%. The artificial ramp also ensures the proper PWM function when the output ripple voltage is inadequate. The slope compensation signal is properly sized to serve its purposes without sacrificing the transient response speed.

Underload and line transient, not only the ramp signal changes, but more significantly the DC component of the feedback voltage varies proportionally to the output voltage. FFB path connects both signals directly to the PWM comparator. This allows instant modulation of the duty cycle to counteract any output voltage deviations. The transient response time is independent of the error amplifier bandwidth. This eliminates the delay associated with error amplifier and greatly improves the transient response time. The error amplifier is used here to ensure excellent DC accuracy.

Error Amplifier

The CS5141X has a transconductance error amplifier, whose noninverting input is connected to an Internal Reference Voltage generated from the on-chip regulator. The inverting input connects to the V<sub>FB</sub> pin. The output of the error amplifier is made available at the V<sub>C</sub> pin. A typical frequency compensation requires only a 0.1 μF capacitor connected between the V<sub>C</sub> pin and ground, as shown in Figure 1. This capacitor and error amplifier's output resistance (approximately 8.0 MΩ) create a low frequency pole to limit the bandwidth. Since V<sup>2</sup> control does not require a high bandwidth error amplifier, the frequency compensation is greatly simplified.

The V<sub>C</sub> pin is clamped below Output High Voltage. This allows the regulator to recover quickly from overcurrent or short circuit conditions.

Oscillator and Sync Feature (CS51411 and CS51413 only)

The on-chip oscillator is trimmed at the factory and requires no external components for frequency control. The high switching frequency allows smaller external components to be used, resulting in a board area and cost savings. The tight frequency tolerance simplifies magnetic components selection. The switching frequency is reduced to 25% of the nominal value when the V<sub>FB</sub> pin voltage is below Frequency Foldback Threshold. In short circuit or overload conditions, this reduces the power dissipation of the IC and external components.

An external clock signal can sync CS51411/CS51414 to a higher frequency. The rising edge of the sync pulse turns on the power switch to start a new switching cycle, as shown in Figure 4. There is approximately 0.5 μs delay between the rising edge of the sync pulse and rising edge of the V<sub>SW</sub> pin voltage. The sync threshold is TTL logic compatible, and duty cycle of the

sync pulses can vary from 10% to 90%. The frequency foldback feature is disabled during the sync mode.

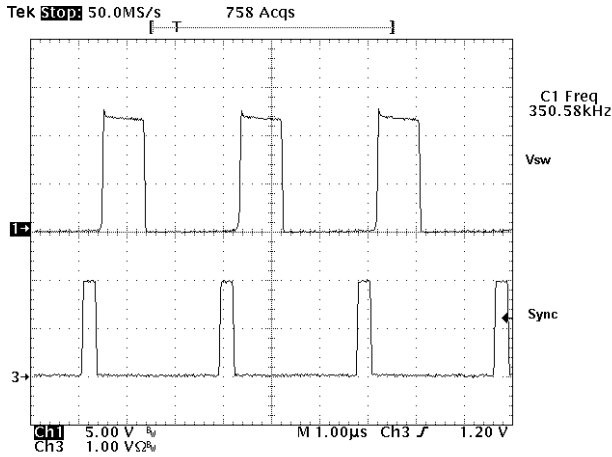


Figure 4. A CS51411 Buck Regulator is Synced by an External 350 kHz Pulse Signal

**Power Switch and Current Limit**

The collector of the built-in NPN power switch is connected to the  $V_{IN}$  pin, and the emitter to the  $V_{SW}$  pin. When the switch turns on, the  $V_{SW}$  voltage is equal to the  $V_{IN}$  minus switch Saturation Voltage. In the buck regulator, the  $V_{SW}$  voltage swings to one diode drop below ground when the power switch turns off, and the inductor current is commutated to the catch diode. Due to the presence of high pulsed current, the traces connecting the  $V_{SW}$  pin, inductor and diode should be kept as short as possible to minimize the noise and radiation. For the same reason, the input capacitor should be placed close to the  $V_{IN}$  pin and the anode of the diode.

The saturation voltage of the power switch is dependent on the switching current, as shown in Figure 5.

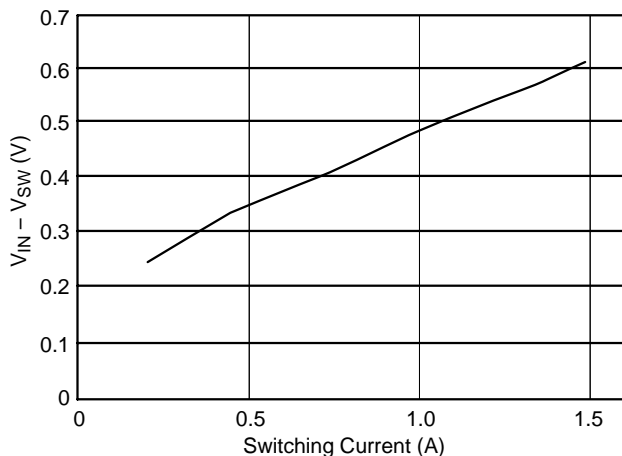


Figure 5. The Saturation Voltage of the Power Switch Increases with the Conducting Current

Members of the CS5141X family contain pulse-by-pulse current limiting to protect the power switch and external components. When the peak of the switching current reaches the Current Limit, the power switch turns off after the

Current Limit Delay. The switch will not turn on until the next switching cycle. The current limit threshold is independent of switching duty cycle. The maximum load current, given by the following formula under continuous conduction mode, is less than the Current Limit due to the ripple current.

$$I_{O(MAX)} = I_{LIM} - \frac{V_O(V_{IN} - V_O)}{2(L)(V_{IN})(f_s)}$$

where:

- $f_s$  = switching frequency,
- $I_{LIM}$  = current limit threshold,
- $V_O$  = output voltage,
- $V_{IN}$  = input voltage,
- $L$  = inductor value.

When the regulator runs undercurrent limit, the subharmonic oscillation may cause low frequency oscillation, as shown in Figure 6. Similar to current mode control, this oscillation occurs at the duty cycle greater than 50% and can be alleviated by using a larger inductor value. The current limit threshold is reduced to Foldback Current when the FB pin falls below Foldback Threshold. This feature protects the IC and external components under the power up or overload conditions.

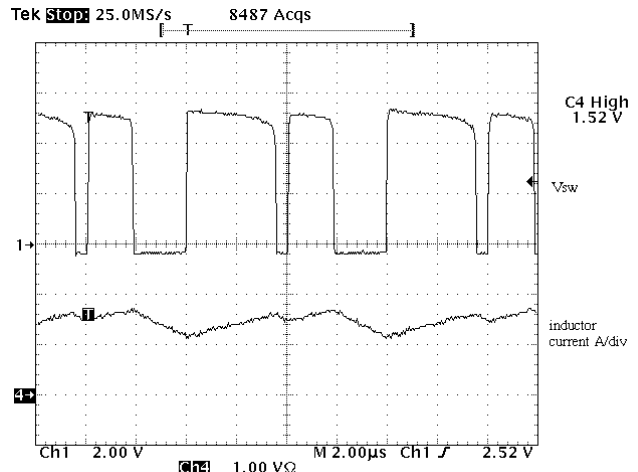


Figure 6. The Regulator in Current Limit

**BOOST Pin**

The BOOST pin provides base driving current for the power switch. A voltage higher than  $V_{IN}$  provides required headroom to turn on the power switch. This in turn reduces IC power dissipation and improves overall system efficiency. The BOOST pin can be connected to an external boost-strapping circuit which typically uses a 0.1  $\mu$ F capacitor and a 1N914 or 1N4148 diode, as shown in Figure 1. When the power switch is turned on, the voltage on the BOOST pin is equal to

$$V_{BOOST} = V_{IN} + V_O - V_F$$

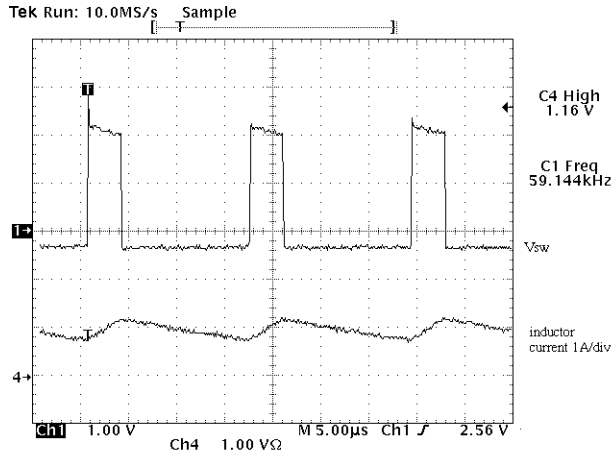
where:

- $V_F$  = diode forward voltage.





can result in an equal percentage drop of the inductor and diode current. The short circuit waveforms are captured in Figure 9, and the benefit of the foldback frequency and current limit is self-evident.



**Figure 9. In Short Circuit, the Foldback Current and Foldback Frequency Limit the Switching Current to Protect the IC, Inductor and Catch Diode**

**Thermal Considerations**

A calculation of the power dissipation of the IC is always necessary prior to the adoption of the regulator. The current drawn by the IC includes quiescent current, predriver current, and power switch base current. The quiescent current drives the low power circuits in the IC, which include comparators, error amplifier and other logic blocks. Therefore, this current is independent of the switching current and generates power equal to

$$W_Q = V_{IN} \times I_Q$$

where:

$I_Q$  = quiescent current.

The predriver current is used to turn on/off the power switch and is approximately equal to 12 mA in worst case. During steady state operation, the IC draws this current from the Boost pin when the power switch is on and then receives it from the  $V_{IN}$  pin when the switch is off. The predriver current always returns to the  $V_{SW}$  pin. Since the predriver current goes out to the regulator’s output even when the power switch is turned off, a minimum load is required to prevent overvoltage in light load conditions. If the Boost pin voltage is equal to  $V_{IN} + V_O$  when the switch is on, the power dissipation due to predriver current can be calculated by

$$W_{DRV} = 12 \text{ mA} \times (V_{IN} - V_O + \frac{V_O^2}{V_{IN}})$$

The base current of a bipolar transistor is equal to collector current divided by beta of the device. Beta of 60 is used here to estimate the base current. The Boost pin provides the base current when the transistor needs to be on. The power dissipated by the IC due to this current is

$$W_{BASE} = \frac{V_O^2}{V_{IN}} \times \frac{I_S}{60}$$

where:

$I_S$  = DC switching current.

When the power switch turns on, the saturation voltage and conduction current contribute to the power loss of a non-ideal switch. The power loss can be quantified as

$$W_{SAT} = \frac{V_O}{V_{IN}} \times I_S \times V_{SAT}$$

where:

$V_{SAT}$  = saturation voltage of the power switch which is shown in Figure 5.

The switching loss occurs when the switch experiences both high current and voltage during each switch transition. This regulator has a 30 ns turn-off time and associated power loss is equal to

$$W_S = \frac{I_S \times V_{IN}}{2} \times 30 \text{ ns} \times f_S$$

The turn-on time is much shorter and thus turn-on loss is not considered here.

The total power dissipated by the IC is sum of all the above

$$W_{IC} = W_Q + W_{DRV} + W_{BASE} + W_{SAT} + W_S$$

The IC junction temperature can be calculated from the ambient temperature, IC power dissipation and thermal resistance of the package. The equation is shown as follows,

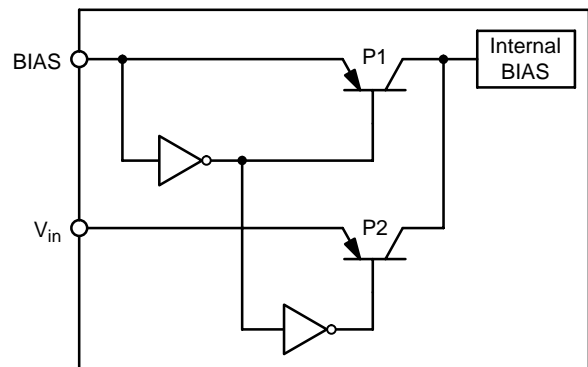
$$T_J = W_{IC} \times R_{\theta JA} + T_A$$

The maximum IC junction temperature shall not exceed 125°C to guarantee proper operation and avoid any damages to the IC.

**Using the BIAS Pin**

The efficiency savings in using the BIAS pin is most notable at low load and high input voltage as will be explained below.

Figure 10 will help to understand the increase in efficiency when the BIAS pin is used. The circuitry shown is not the actual implementation, but is useful in the explanation.



**Figure 10.**

Internal bias to the IC can be supplied via the  $V_{in}$  pin or the BIAS pin. When the BIAS pin is low, the logic turns P2 on and current is routed to the internal bias circuitry from the  $V_{in}$  pin. Conversely, when the BIAS pin is high, the logic turns P1 on and current is routed to the internal bias circuitry from the BIAS pin.

Here is an example of the power savings:

The input voltage range for  $V_{in}$  is 4.5 V to 40 V. The input voltage range for BIAS is 3.3 V to 6 V. The quiescent current specification is 3 mA (min), 4 mA (typ), and 6.25 mA (max).

Using a typical battery voltage of 14 V and the typical quiescent current number of 4 mA, the power would be:

$$P = V \times I = 14 \times 4e-3 = 56 \text{ mW}$$

We'll assume the BIAS pin is connected to an external regulator at 5 V instead of the output voltage. The BIAS pin would normally be connected to the output voltage, but adding an added switching regulator efficiency number here would cloud this example. Now the internal BIAS circuitry is being powered via 5 V. The resulting on chip power being dissipated is:

$$P = V \times I = 5 \times 4e-3 = 21 \text{ mW}$$

The power savings is 35 mW.

Now, to demonstrate more notable savings using the maximum battery input voltage of 40 V, the maximum quiescent current of 6.25 mA, and the lowest allowed BIAS voltage for proper operation of 3.3 V;

Powered from  $V_{in}$ :

$$P = 40 \times 6.25e-3 = 250 \text{ mW}$$

Powered from the BIAS pin:

$$P = 3.3 \times 6.25e-3 = 21 \text{ mW}$$

The power savings is 229 mW.

**Minimum Load Requirement**

As pointed out in the previous section, a minimum load is required for this regulator due to the predriver current feeding the output. Placing a resistor equal to  $V_O$  divided by 12 mA should prevent any voltage overshoot at light load conditions. Alternatively, the feedback resistors can be valued properly to consume 12 mA current.

**COMPONENT SELECTION**

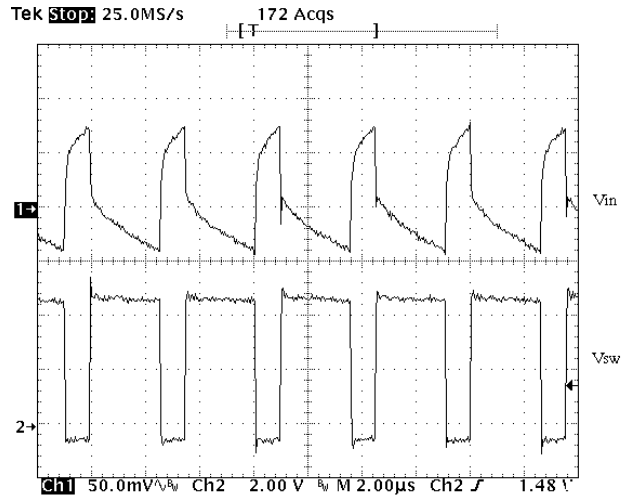
**Input Capacitor**

In a buck converter, the input capacitor witnesses pulsed current with an amplitude equal to the load current. This pulsed current and the ESR of the input capacitors determine the  $V_{IN}$  ripple voltage, which is shown in Figure 11. For  $V_{IN}$  ripple, low ESR is a critical requirement for the input capacitor selection. The pulsed input current possesses a significant AC component, which is absorbed by the input capacitors. The RMS current of the input capacitor can be calculated using:

$$I_{RMS} = I_O \sqrt{D(1 - D)}$$

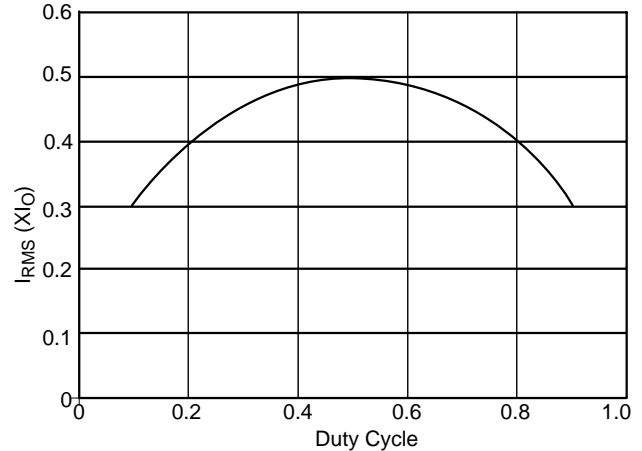
where:

$D$  = switching duty cycle which is equal to  $V_O/V_{IN}$ .  
 $I_O$  = load current.



**Figure 11. Input Voltage Ripple in a Buck Converter**

To calculate the RMS current, multiply the load current with the constant given by Figure 12 at each duty cycle. It is a common practice to select the input capacitor with an RMS current rating more than half the maximum load current. If multiple capacitors are paralleled, the RMS current for each capacitor should be the total current divided by the number of capacitors.



**Figure 12. Input Capacitor RMS Current can be Calculated by Multiplying Y Value with Maximum Load Current at any Duty Cycle**

Selecting the capacitor type is determined by each design's constraint and emphasis. The aluminum electrolytic capacitors are widely available at lowest cost. Their ESR and Equivalent Series Inductor (ESL) are relatively high. Multiple capacitors are usually paralleled to achieve lower ESR. In addition, electrolytic capacitors usually need to be paralleled with a ceramic capacitor for filtering high frequency noises. The OS-CON are solid aluminum electrolytic capacitors, and therefore has a much lower ESR. Recently, the price of the OS-CON capacitors

has dropped significantly so that it is now feasible to use them for some low cost designs. Electrolytic capacitors are physically large, and not used in applications where the size, and especially height is the major concern.

Ceramic capacitors are now available in values over 10  $\mu\text{F}$ . Since the ceramic capacitor has low ESR and ESL, a single ceramic capacitor can be adequate for both low frequency and high frequency noises. The disadvantage of ceramic capacitors are their high cost. Solid tantalum capacitors can have low ESR and small size. However, the reliability of the tantalum capacitor is always a concern in the application where the capacitor may experience surge current.

**Output Capacitor**

In a buck converter, the requirements on the output capacitor are not as critical as those on the input capacitor. The current to the output capacitor comes from the inductor and thus is triangular. In most applications, this makes the RMS ripple current not an issue in selecting output capacitors.

The output ripple voltage is the sum of a triangular wave caused by ripple current flowing through ESR, and a square wave due to ESL. Capacitive reactance is assumed to be small compared to ESR and ESL. The peak-to-peak ripple current of the inductor is:

$$I_{P-P} = \frac{V_O(V_{IN} - V_O)}{(V_{IN})(L)(f_S)}$$

$V_{\text{RIPPLE(ESR)}}$ , the output ripple due to the ESR, is equal to the product of  $I_{P-P}$  and ESR. The voltage developed across the ESL is proportional to the  $di/dt$  of the output capacitor. It is realized that the  $di/dt$  of the output capacitor is the same as the  $di/dt$  of the inductor current. Therefore, when the switch turns on, the  $di/dt$  is equal to  $(V_{IN} - V_O)/L$ , and it becomes  $V_O/L$  when the switch turns off. The total ripple voltage induced by ESL can then be derived from

$$V_{\text{RIPPLE(ESL)}} = \text{ESL} \left( \frac{V_{IN}}{L} \right) + \text{ESL} \left( \frac{V_{IN} - V_O}{L} \right) = \text{ESL} \left( \frac{V_{IN}}{L} \right)$$

The total output ripple is the sum of the  $V_{\text{RIPPLE(ESR)}}$  and  $V_{\text{RIPPLE(ESL)}}$ .

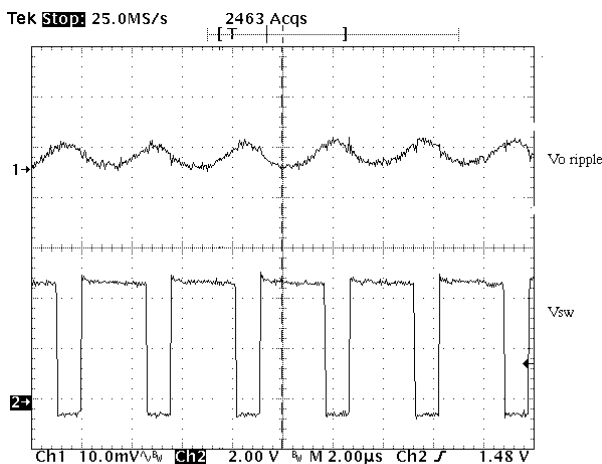


Figure 13. The Output Voltage Ripple Using Two 10  $\mu\text{F}$  Ceramic Capacitors in Parallel

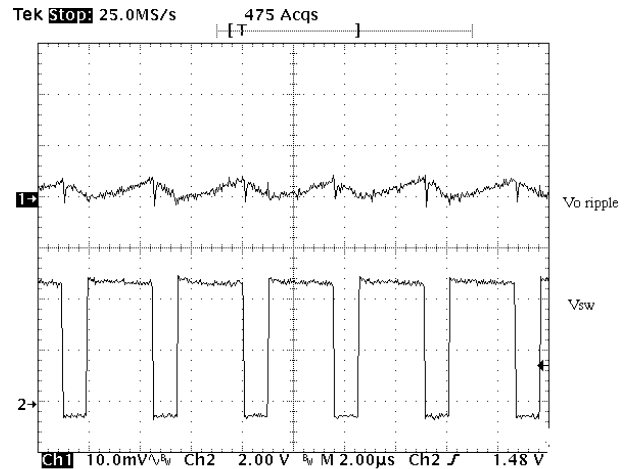


Figure 14. The Output Voltage Ripple Using One 100  $\mu\text{F}$  POSCAP Capacitor

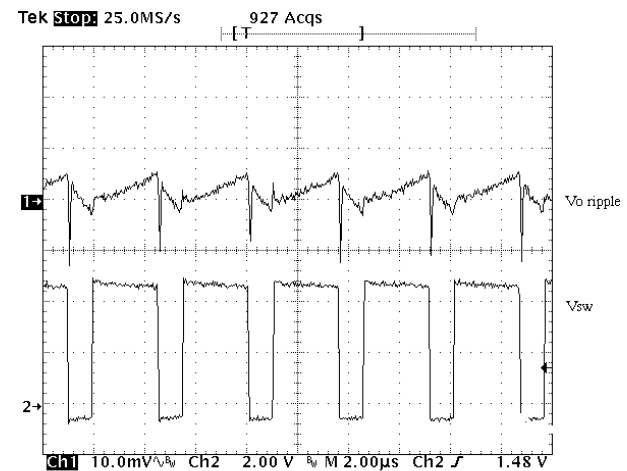


Figure 15. The Output Voltage Ripple Using One 100  $\mu\text{F}$  OS-CON

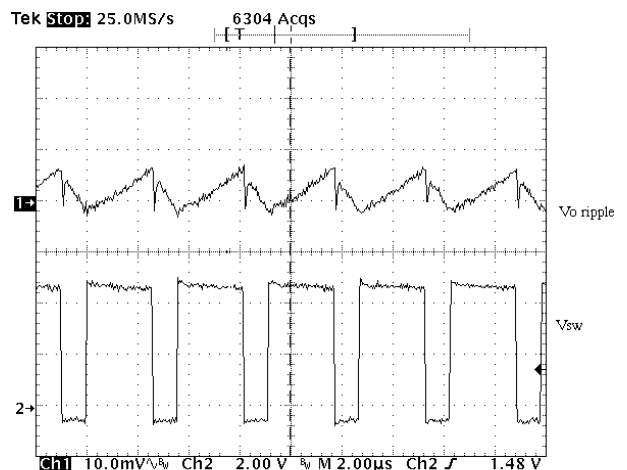


Figure 16. The Output Voltage Ripple Using One 100  $\mu\text{F}$  Tantalum Capacitor

Figure 13 to Figure 16 show the output ripple of a 5.0 V to 3.3 V/500 mA regulator using 22 μH inductor and various capacitor types. At the switching frequency, the low ESR and ESL make the ceramic capacitors behave capacitively as shown in Figure 13. Additional paralleled ceramic capacitors will further reduce the ripple voltage, but inevitably increase the cost. “POSCAP”, manufactured by SANYO, is a solid electrolytic capacitor. The anode is sintered tantalum and the cathode is a highly conductive polymerized organic semiconductor. TPC series, featuring low ESR and low profile, is used in the measurement of Figure 14. It is shown that POSCAP presents a good balance of capacitance and ESR, compared with a ceramic capacitor. In this application, the low ESR generates less than 5.0 mV of ripple and the ESL is almost unnoticeable. The ESL of the through-hole OS-CON capacitor give rise to the inductive impedance. It is evident from Figure 15 which shows the step rise of the output ripple on the switch turn-on and large spike on the switch turn-off. The ESL prevents the output capacitor from quickly charging up the parasitic capacitor of the inductor when the switch node is pulled below ground through the catch diode conduction. This results in the spike associated with the falling edge of the switch node. The D package tantalum capacitor used in Figure 16 has the same footprint as the POSCAP, but doubles the height. The ESR of the tantalum capacitor is apparently higher than the POSCAP. The electrolytic and tantalum capacitors provide a low-cost solution with compromised performance. The reliability of the tantalum capacitor is not a serious concern for output filtering because the output capacitor is usually free of surge current and voltage.

#### Diode Selection

The diode in the buck converter provides the inductor current path when the power switch turns off. The peak reverse voltage is equal to the maximum input voltage. The peak conducting current is clamped by the current limit of the IC. The average current can be calculated from:

$$I_{D(AVG)} = \frac{I_O(V_{IN} - V_O)}{V_{IN}}$$

The worse case of the diode average current occurs during maximum load current and maximum input voltage. For the diode to survive the short circuit condition, the current rating of the diode should be equal to the Foldback Current Limit. See Table 1 for Schottky diodes from ON Semiconductor which are suggested for CS5141X regulator.

#### Inductor Selection

When choosing inductors, one might have to consider maximum load current, core and copper losses, component height, output ripple, EMI, saturation and cost. Lower inductor values are chosen to reduce the physical size of the inductor. Higher value cuts down the ripple current, core losses and allows more output current. For most applications, the inductor value falls in the range between 2.2 μH and 22 μH. The saturation current ratings of the inductor shall not exceed the  $I_{L(PK)}$ , calculated according to

$$I_{L(PK)} = I_O + \frac{V_O(V_{IN} - V_O)}{2(f_S)L(V_{IN})}$$

The DC current through the inductor is equal to the load current. The worse case occurs during maximum load current. Check the vendor’s spec to adjust the inductor value undercurrent loading. Inductors can lose over 50% of inductance when it nears saturation.

The core materials have a significant effect on inductor performance. The ferrite core has benefits of small physical size, and very low power dissipation. But be careful not to operate these inductors too far beyond their maximum ratings for peak current, as this will saturate the core. Powered Iron cores are low cost and have a more gradual saturation curve. The cores with an open magnetic path, such as rod or barrel, tend to generate high magnetic field radiation. However, they are usually cheap and small. The cores providing a close magnetic loop, such as pot-core and toroid, generate low electro-magnetic interference (EMI).

There are many magnetic component vendors providing standard product lines suitable for CS5141X. Table 2 lists three vendors, their products and contact information.

## CS51411, CS51412, CS51413, CS51414

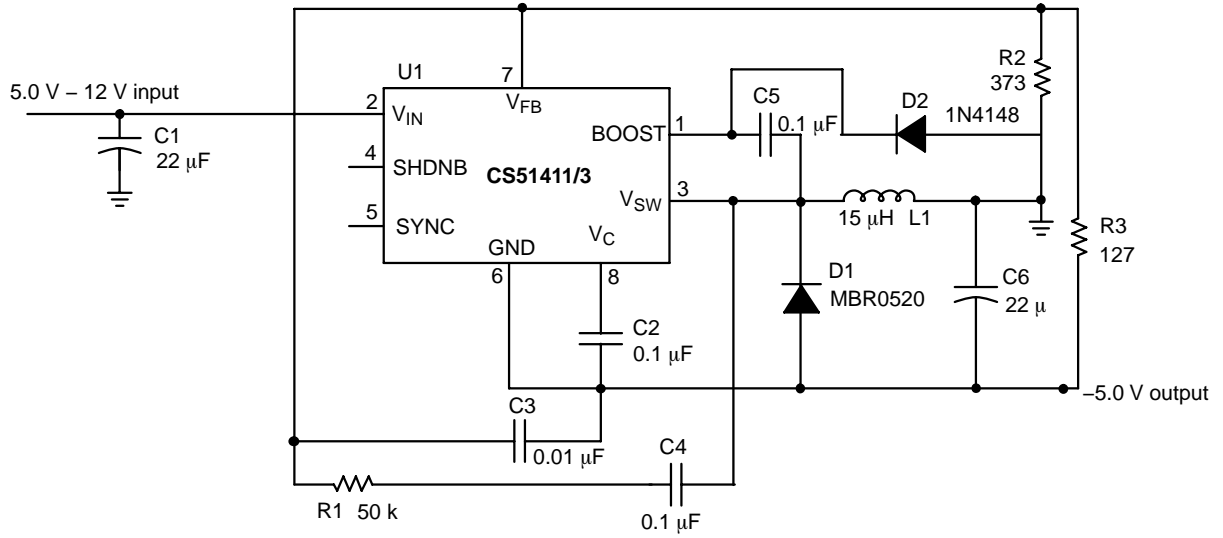
**Table 1.**

Part Number	V <sub>BREAKDOWN</sub> (V)	I <sub>AVERAGE</sub> (A)	V <sub>(F)</sub> (V) @ I <sub>AVERAGE</sub>	Package
1N5817	20	1.0	0.45	Axial Lead
1N5818	30	1.0	0.55	Axial Lead
1N5819	40	1.0	0.6	Axial Lead
MBR0520	20	0.5	0.385	SOD-123
MBR0530	30	0.5	0.43	SOD-123
MBR0540	40	0.5	0.53	SOD-123
MBRS120	20	1.0	0.55	SMB
MBRS130	30	1.0	0.395	SMB
MBRS140	40	1.0	0.6	SMB

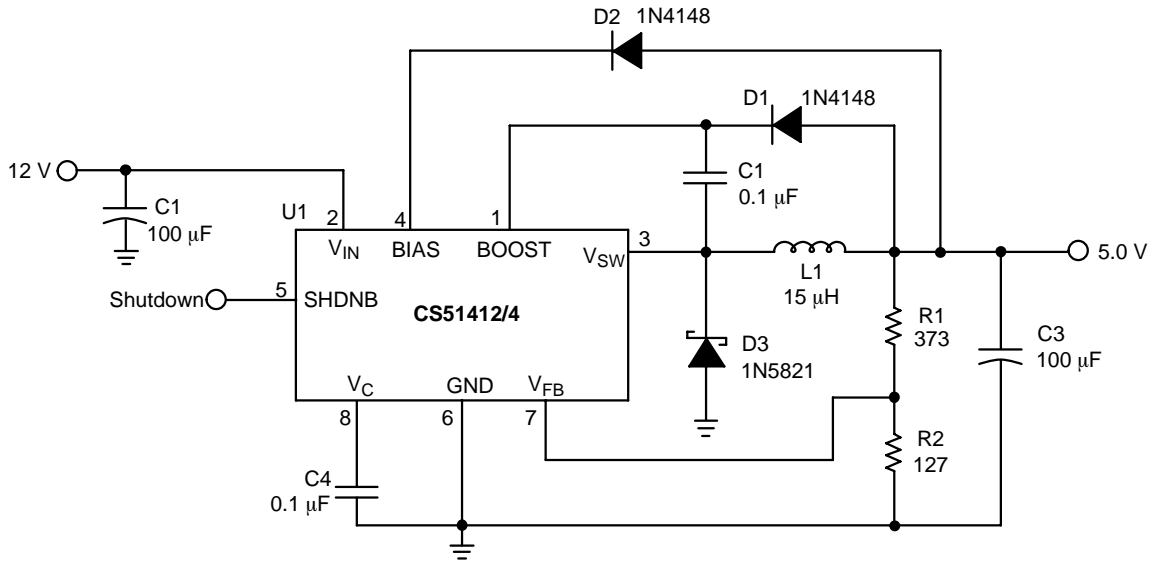
**Table 2.**

Vendor	Product Family	Web Site	Telephone
Coiltronics	UNI-Pac1/2: SMT, barrel THIN-PAC: SMT, toroid, low profile CTX: Leaded, toroid	www.coiltronics.com	(516) 241-7876
Coilcraft	DO1608: SMT, barrel DS/DT 1608: SMT, barrel, magnetically shielded DO3316: SMT, barrel DS/DT 3316: SMT, barrel, magnetically shielded DO3308: SMT, barrel, low profile	www.coilcraft.com	(800) 322-2645
Pulse	-	www.pulseeng.com	(619) 674-8100

**CS51411, CS51412, CS51413, CS51414**



**Figure 17. Additional Application Diagram, 5.0 V - 12 V to -5.0 V/400 mA Inverting Converter**



**Figure 18. Additional Application Diagram, 12 V to 5.0 V/1.0 A Buck Converter using the BIAS Pin**

# CS51411, CS51412, CS51413, CS51414

## ORDERING INFORMATION

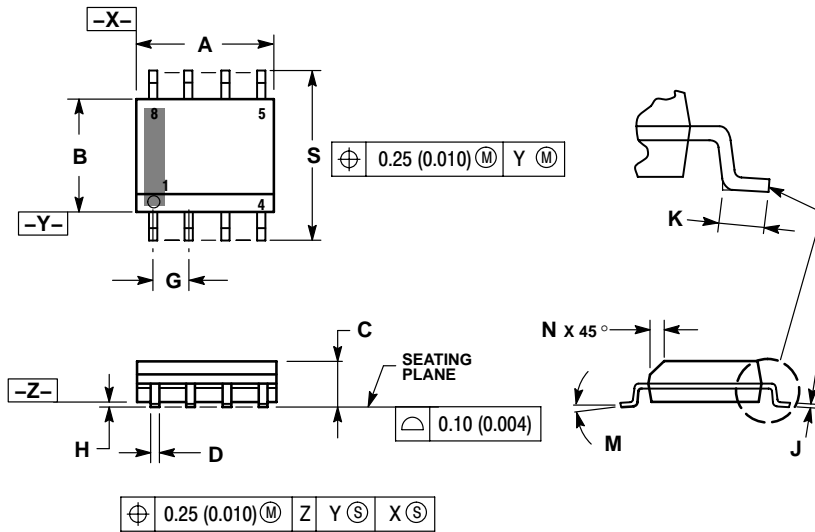
Device	Operating Temperature Range	Package	Shipping†	
CS51411ED8	-40°C < T <sub>A</sub> < 85°C	SOIC-8	98 Units/Rail	
CS51411ED8G		SOIC-8 (Pb-Free)	98 Units/Rail	
CS51411EDR8		SOIC-8	2500 Tape & Reel	
CS51411EDR8G		SOIC-8 (Pb-Free)	2500 Tape & Reel	
CS51412ED8		SOIC-8	98 Units/Rail	
CS51412ED8G		SOIC-8 (Pb-Free)	98 Units/Rail	
CS51412EDR8		SOIC-8	2500 Tape & Reel	
CS51412EDR8G		SOIC-8 (Pb-Free)	2500 Tape & Reel	
CS51413ED8		SOIC-8	98 Units/Rail	
CS51413ED8G		SOIC-8 (Pb-Free)	98 Units/Rail	
CS51413EDR8		SOIC-8	2500 Tape & Reel	
CS51413EDR8G		SOIC-8 (Pb-Free)	2500 Tape & Reel	
CS51414ED8		SOIC-8	98 Units/Rail	
CS51414ED8G		SOIC-8 (Pb-Free)	98 Units/Rail	
CS51414EDR8		SOIC-8	2500 Tape & Reel	
CS51414EDR8G		SOIC-8 (Pb-Free)	2500 Tape & Reel	
CS51411GD8		0°C < T <sub>A</sub> < 70°C	SOIC-8	98 Units/Rail
CS51411GD8G			SOIC-8 (Pb-Free)	98 Units/Rail
CS51411GDR8	SOIC-8		2500 Tape & Reel	
CS51411GDR8G	SOIC-8 (Pb-Free)		2500 Tape & Reel	
CS51412GD8	SOIC-8		98 Units/Rail	
CS51412GD8G	SOIC-8 (Pb-Free)		98 Units/Rail	
CS51412GDR8	SOIC-8		2500 Tape & Reel	
CS51412GDR8G	SOIC-8 (Pb-Free)		2500 Tape & Reel	
CS51413GD8	SOIC-8		98 Units/Rail	
CS51413GD8G	SOIC-8 (Pb-Free)		98 Units/Rail	
CS51413GDR8	SOIC-8		2500 Tape & Reel	
CS51413GDR8G	SOIC-8 (Pb-Free)		2500 Tape & Reel	
CS51414GD8	SOIC-8		98 Units/Rail	
CS51414GD8G	SOIC-8 (Pb-Free)		98 Units/Rail	
CS51414GDR8	SOIC-8		2500 Tape & Reel	
CS51414GDR8G	SOIC-8 (Pb-Free)		2500 Tape & Reel	

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

# CS51411, CS51412, CS51413, CS51414

## PACKAGE DIMENSIONS

SOIC-8 NB  
CASE 751-07  
ISSUE AG

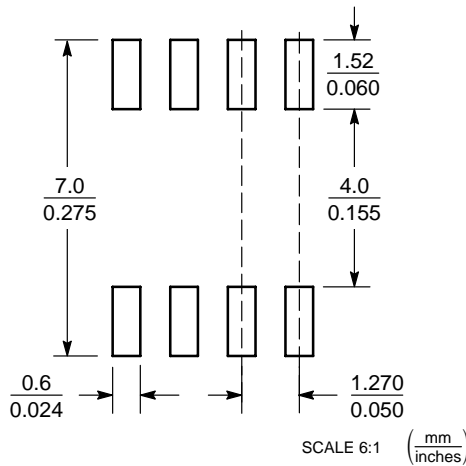


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751-01 THRU 751-06 ARE OBSOLETE. NEW STANDARD IS 751-07.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0°	8°	0°	8°
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

### SOLDERING FOOTPRINT\*




\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

### PACKAGE THERMAL DATA

Parameter		SOIC-8	Unit
R <sub>θJC</sub>	Typical	45	°C/W
R <sub>θJA</sub>	Typical	165	°C/W



V<sup>2</sup> is a trademark of Switch Power, Inc.

**ON Semiconductor** and  are registered trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

#### PUBLICATION ORDERING INFORMATION

**LITERATURE FULFILLMENT:**

Literature Distribution Center for ON Semiconductor  
P.O. Box 61312, Phoenix, Arizona 85082-1312 USA  
**Phone:** 480-829-7710 or 800-344-3860 Toll Free USA/Canada  
**Fax:** 480-829-7709 or 800-344-3867 Toll Free USA/Canada  
**Email:** orderlit@onsemi.com

**N. American Technical Support:** 800-282-9855 Toll Free  
USA/Canada

**Japan:** ON Semiconductor, Japan Customer Focus Center  
2-9-1 Kamimeguro, Meguro-ku, Tokyo, Japan 153-0051  
**Phone:** 81-3-5773-3850

**ON Semiconductor Website:** <http://onsemi.com>

**Order Literature:** <http://www.onsemi.com/litorder>

For additional information, please contact your  
local Sales Representative.