

4 x 4 REGISTER FILE

- SIMULTANEOUS READ/WRITE OPERATION
- EXPANDABLE TO 512 WORDS OF n-BIT
- TYPICAL ACCESS TIME OF 20 ns
- LOW LEAKAGE OPEN COLLECTOR OUTPUTS FOR EXPANSION
- TYPICAL POWER DISSIPATION OF 125 mW
- INPUT CLAMP DIODE LIMIT HIGH SPEED TERMINATION EFFECTS
- FULLY COMPATIBLE

DESCRIPTION

The T74LS170 is a high speed, low power 4 x 4 Register File organized as four word by four bits. Separate read and write inputs, both address and enable, allow simultaneous read and write operation.

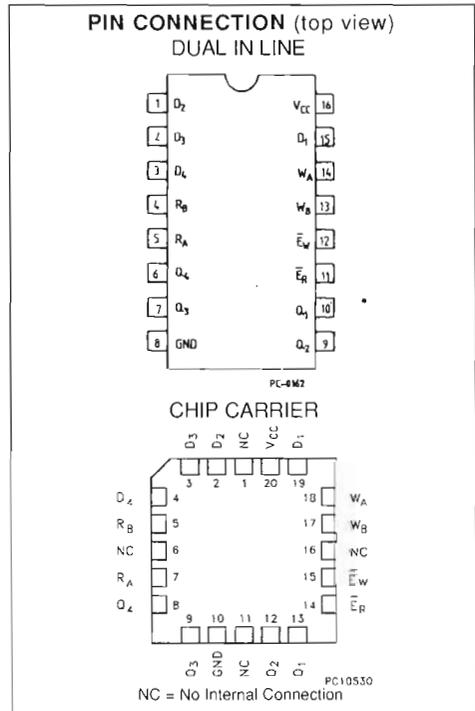
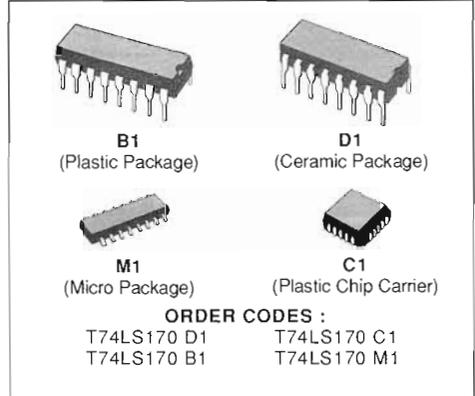
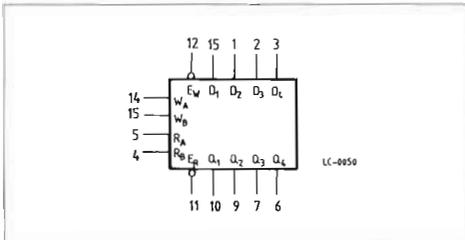
Open Collector outputs make it possible, to connect up to 128 outputs in a wired-AND configuration to increase the word capacity up to 512 words. Any number of these devices can be operated in parallel to generate an n-bit length.

The T74LS670 provides a similar function to this device but it features 3-state outputs.

PIN NAMES

D ₁ -D ₄	Data Inputs
W _A -W _B	Write Address Inputs
\bar{E}_W	Write Enable (Active LOW) Input
R _A -R _B	Read Address Inputs
\bar{E}_R	Read Enable (Active LOW) Input
Q ₁ -Q ₄	Outputs

LOGIC DIAGRAM



WRITE TRUTH TABLE

WRITE INPUTS			WORD			
W _B	W _A	Ē _W	0	1	2	3
L	L	L	Q = D	Q ₀	Q ₀	Q ₀
L	H	L	Q ₀	Q = D	Q ₀	Q ₀
H	L	L	Q ₀	Q ₀	Q = D	Q ₀
H	H	L	Q ₀	Q ₀	Q ₀	Q = D
X	X	H	Q ₀	Q ₀	Q ₀	Q ₀

NOTES: H= HIGH Level, L = LOW Level, X = Don't Care
(Q = D) = The four selected internal flip-flop outputs will assume the states applied to the four external data inputs.
Q₀ = The level of Q before the indicated input conditions were established.
W₀B₁ = The first bit of word 0 etc.

READ TRUTH TABLE

READ INPUTS			OUTPUTS			
R _B	R _A	Ē _R	Q ₁	Q ₂	Q ₃	Q ₄
L	L	L	W ₀ B ₁	W ₀ B ₂	W ₀ B ₃	W ₀ B ₄
L	H	L	W ₁ B ₁	W ₁ B ₂	W ₁ B ₃	W ₁ B ₄
H	L	L	W ₂ B ₁	W ₂ B ₂	W ₂ B ₃	W ₂ B ₄
H	H	L	W ₃ B ₁	W ₃ B ₂	W ₃ B ₃	W ₃ B ₄
X	X	H	H	H	H	H

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V _{CC}	Supply Voltage	- 0.5 to 7	V
V _I	Input Voltage, Applied to Input	- 0.5 to 15	V
V _O	Output Voltage, Applied to Output	0 to 10	V
I _I	Input Current, into Inputs	- 30 to 5	mA
I _O	Output Current, into Outputs	50	mA

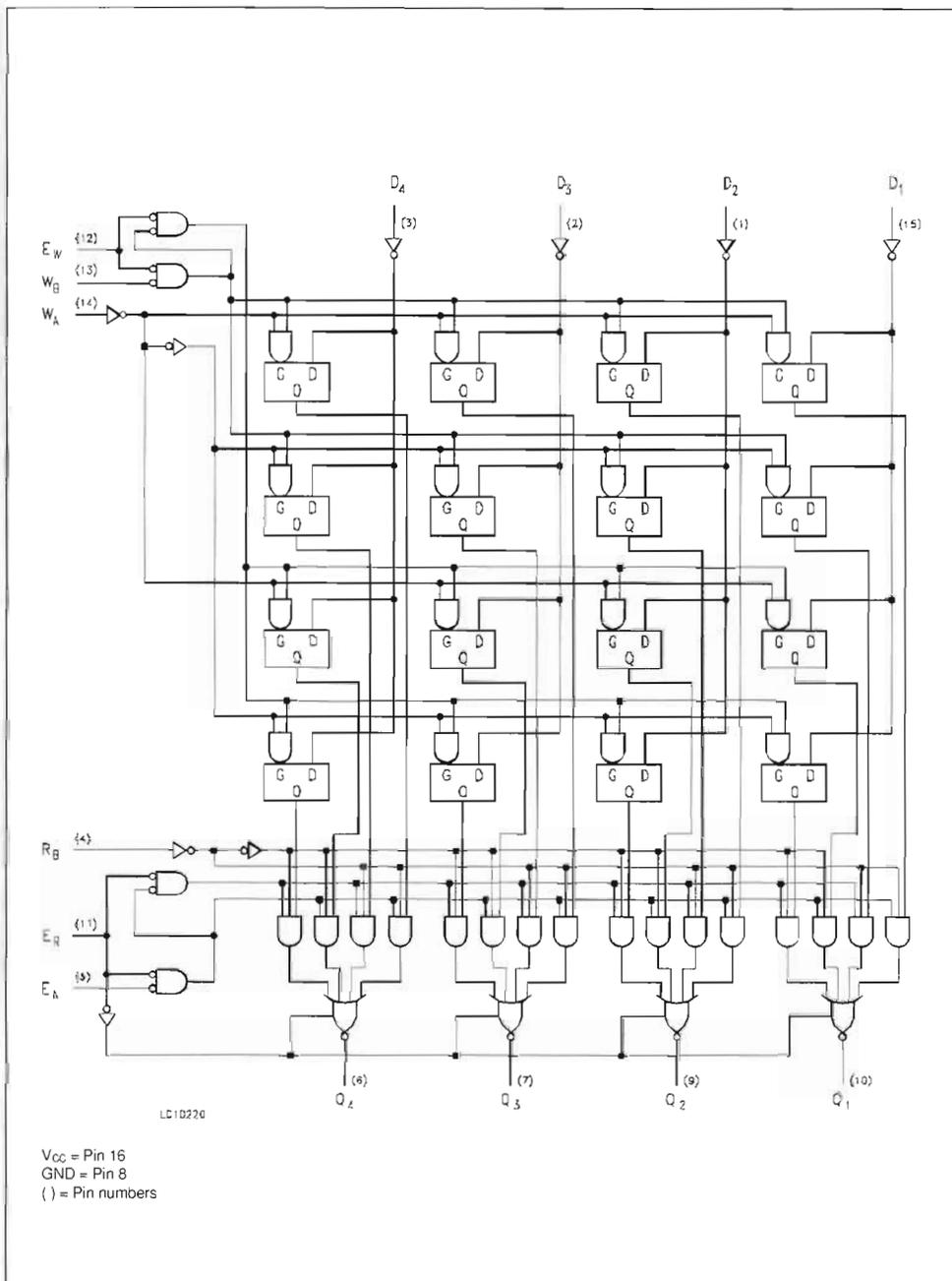
Stresses in excess of those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions in excess of those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

GUARANTEED OPERATING RANGE

Part Numbers	Supply Voltage			Temperature
	Min.	Typ.	Max.	
T74LS170XX	4.75 V	5.0 V	5.25 V	0 °C to + 70 °C

XX = package type.

LOGIC DIAGRAMS



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

Symbol	Parameter	Limits			Test Condition (note 1)	Unit	
		Min.	Typ. (*)	Max.			
V _{IH}	Input HIGH Voltage	2.0			Guaranteed Input HIGH Voltage for All Inputs	V	
V _{IL}	Input LOW Voltage			0.8	Guaranteed Input LOW Voltage for All Inputs	V	
V _{CD}	Input Clamp Diode Voltage		- 0.65	- 1.5	V _{CC} = MIN, I _{IN} = -18 mA	V	
I _{OH}	Output HIGH Current			20	V _{CC} = MIN, V _{OH} = - 5.5 V V _{IN} = V _{IH} or V _{IL} per Truth Table	μA	
V _{OL}	Output LOW Voltage		0.25	0.4	I _{OL} = 4.0 mA	V _{CC} = MIN, V _{IN} = V _{IH} or V _{IL} per Truth Table	V
			0.35	0.5	I _{OL} = 8.0 mA		V
I _{IH}	Input HIGH Current Any D, R or W E _R or E _W			20 40	V _{CC} = MAX, V _{IN} = 2.7 V	μA	
	Any D, R or W E _R or E _W			0.1 0.2	V _{CC} = MAX, V _{IN} = 7.0 V	mA	
I _{IL}	Input LOW Current Any D, R or W E _R or E _W			- 0.4 - 0.8	V _{CC} = MAX, V _{IN} = 0.4 V	mA	
I _{CC}	Power Supply Current (Note 2)		25	40	V _{CC} = MAX	mA	

- Notes : 1. For conditions shown as MIN or MAX, use the appropriate value specified under guaranteed operating ranges.
2. I_{CC} is measured under the following worst case conditions: 4.5 V is applied to all data inputs and both enable inputs, all address inputs are grounded, and all outputs are open.

(*) Typical values are at V_{CC} = 5.0 V, T_A = 25 °C.

AC CHARACTERISTICS: T_A = 25 °C

Symbol	Parameter	Limits			Test Conditions	Units	
		Min.	Typ.	Max.			
t _{PLH} t _{PHL}	Propagation Delay, Negative Going E _R to Q Outputs		20 20	30 30	Figures 1	V _{CC} = 5.0 V C _L = 15 pF R _L = 2 KΩ	ns
t _{PLH} t _{PHL}	Propagation Delay, RA or R _B to Q Outputs		25 24	40 40	Figures 2		ns
t _{PLH} t _{PHL}	Propagation Delay, Negative Going E _W to Q Outputs		30 26	40 40	Figures 1		ns
t _{PLH} t _{PHL}	Propagation Delay, Data Inputs to Q Outputs		30 22	45 35	Figures 1		ns

AC SET-UP REQUIREMENTS: $T_A = 25\text{ }^\circ\text{C}$

Symbol	Parameter	Limits			Test Conditions	Units
		Min.	Typ.	Max.		
t_w	Clock Pulse Width (LOW) for \bar{E}_w	25			$V_{CC} = 5.0\text{ V}$ Fig. 3	ns
t_{sD} (Note 3)	Set-up Time, Data Inputs with Respect to Positive-Going \bar{E}_w	10				ns
t_{hD} (Note 4)	Hold Time, Data Inputs with Respect to Positive-Going \bar{E}_w	15				ns
t_{sW} (Note 5)	Set-up Time, Write Select Input W_A and W_B with Respect to Positive-Going \bar{E}_w	15				ns
t_{hW} (Note 4)	Hold Time, Write Select Input W_A and W_B with Respect to Positive-Going \bar{E}_w	15				ns
t_{LATCH}	Latch Time	25				ns

- Notes:**
- 3) The Data to Enable Set-up Time is defined as the time required for the logic level to be present at the Data input prior to the enable transition for LOW to HIGH in order from the latch to recognize and store the new data.
 - 4) The Hold Time (t_h) is defined as the minimum time following the enable transition from LOW to HIGH that the logic level must be maintained at the input in order to ensure continued recognition.
 - 5) The address to Enable Set-up Time is the time before the HIGH to LOW Enable transition the Address must be stable so that the correct latch is addressed and the other latches are not affect.

AC WAVEFORM

Fig 1.

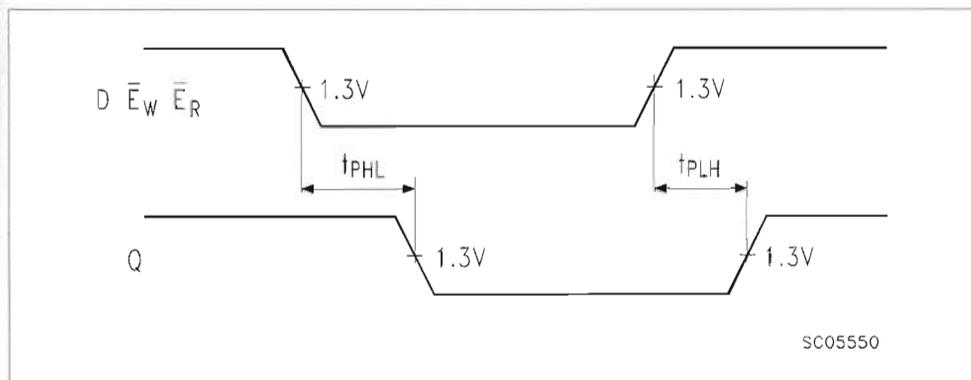


Fig 2.

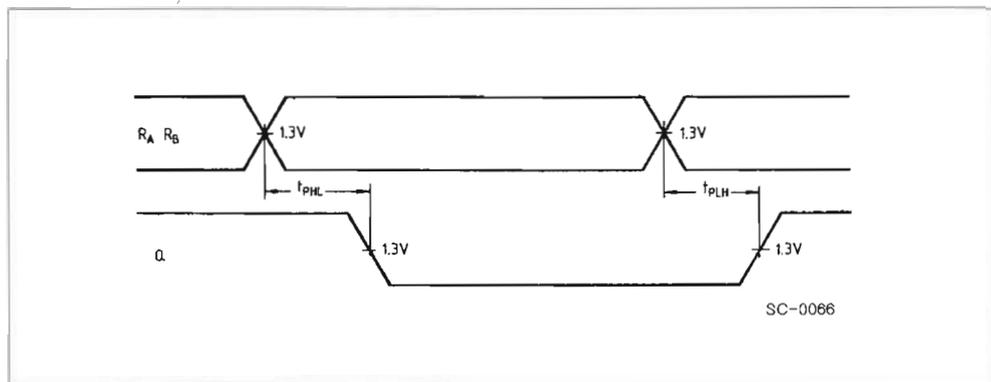
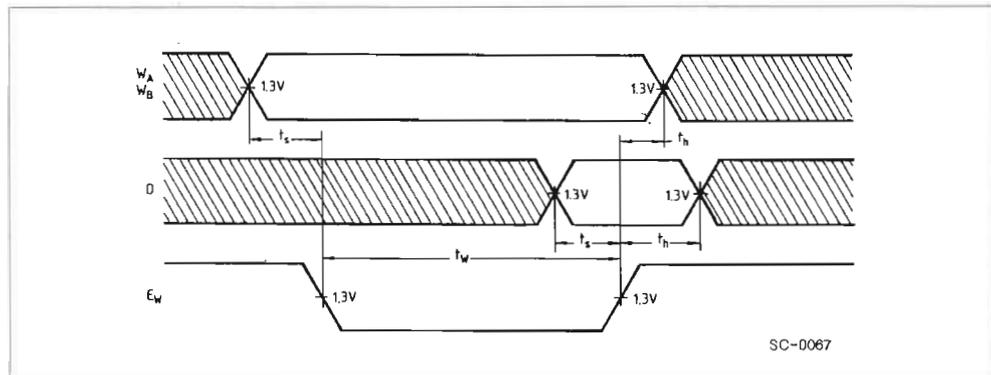


Fig 3.



The shaded areas indicate when the inputs are permitted to change for predictable output performance.