TELEDYNE SEMICONDUCTOR

TSC7126

3 1/2 Digit A/D Converter

• Low Power Dissipation - 900 μW Max.

General Description

The single chip CMOS TSC7126 incorporates all the active devices for a 3 1/2 digit analog-to-digital converter to directly drive an LCD display. The internal oscillator, voltage reference and display segment/backplane drivers simplify system integration, reduce board space requirements and lower total cost. A low cost, high resolution -0.05% - indicating meter requires only a display, four resistors, four capacitors and a 9 V battery. The flat package option eases the mechanical design of low cost, hand held multimeters and systems.

The TSC7126 dual slope conversion technique rejects interference signals when the integration time is set to a multiple of the interference signal period. This is especially useful in industrial measurement environments where 50, 60 and 400 Hz line frequency signals are present.

With an auto-zero error less than 10 μV, zero drift less than 1 μV/° C, input bias current of 10 pA max and rollover error of less than one count, the TSC7126 brings exceptional value to the portable battery powered field.

In addition, the differential input and reference allows the measurement on load cells, strain gauges and other bridge type transducers. The low power TSC7126 can be used as a plug-in replacement for the TSC7106 by changing only the values of seven passive components.

For applications needing a low drift internal voltage reference refer to the TSC7126A data sheet.

Features

- Long Battery Life .... 8000 Hours Typical
- Auto-Zero Cycle
- Guaranteed Zero Reading With Zero Input
- Low Noise .... 15 μV_{p-p}
- High Resolution (0.05%) and Wide Dynamic Range (72 dB)
- Low Input Leakage Current .... 1 pA Typical
  10 pA Maximum
- Direct LCD Display Drive - No External Components.
- Precision Null Detection With True Polarity at Zero
- High Impedance Differential Input
- Convenient 9 V Battery Operation With Low Power Dissipation .... 500 μW Typical
  900 μW Maximum
- Internal Clock Circuit
- Drop-In Replacement for ICL7126
- Available in Compact Flat Package
- Industrial Temperature Range Device

7

Typical Applications

- Thermometry
- Bridge Readouts (Strain Gauges, Load Cells, Null Detectors)
- Digital Meters
  - — Voltage/Current/Ohms/Power
  - — pH
  - — Capacitance/Inductance
  - — Fluid Flow Rate/Viscosity/Level
- Digital Scales
- LVDT Indicators
- Portable Instrumentation
- Power Supply Readouts
- Process Monitors
- Photometers

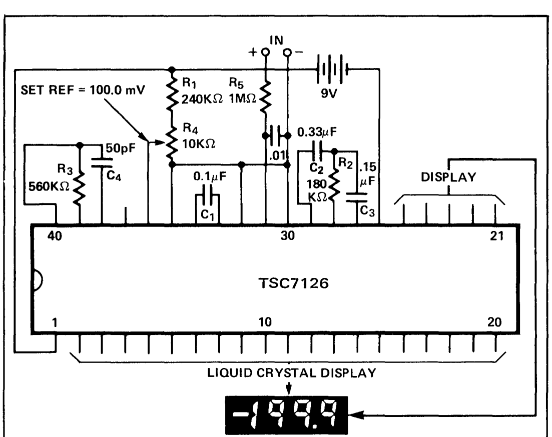


Figure 1: TSC7126 Clock Frequency 16 kHz (1 reading/sec.)

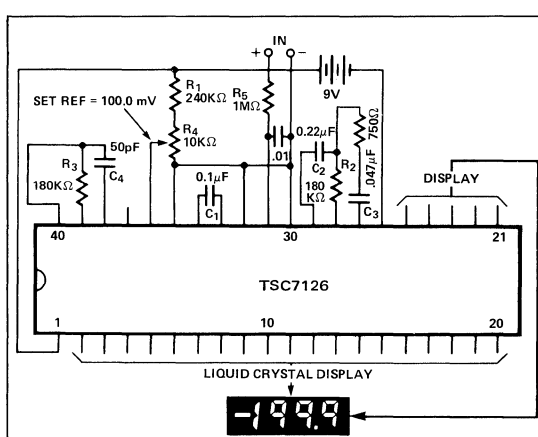


Figure 2: TSC7126 Clock Frequency 48 kHz (3 readings/sec.)

Absolute Maximum Ratings*

Supply voltage (V^+ to V^-) .... 15 V
Analog Input Voltage (either input) [1] .... V^+ to V^-
Reference Input Voltage (either input) .... V^+ to V^-
Clock Input .... Test to V^+
Power Dissipation [2]
  Ceramic Package .... 1000 mW
  Plastic Package .... 800 mW
Operating Temperature
  (C Device) .... 0°C to +70°C
  (I Device) .... -25°C to +85°C
Storage Temperature .... -65°C to +160°C
Lead Temperature (Soldering, 60 sec) .... 300°C

Electrical Characteristics [3]

CHARACTERISTICS	CONDITIONS	MIN	TYP	MAX	UNITS
Zero Input Reading	V_{IN} = 0.0V Full Scale = 200.0 mV	-000.0	±000.0	+000.0	Digital Reading
Ratiometric Reading	$V_{IN} = V_{REF}$ V_{REF} = 100 mV	999	999/1000	1000	Digital Reading
Rollover Error (Difference in reading for equal positive and negative reading near Full Scale)	$-V_{IN} = +V_{IN} \approx$ 200.0 mV	-1	±0.2	+1	Counts
Linearity (Max. deviation from best straight line fit)	Full Scale = 200 mV or Full Scale = 2.000 V	-1	±0.2	+1	Counts
Common Mode Rejection Ratio[4]	V_{CM} = ±1V, V_{IN} = 0V. Full Scale = 200.0 mV	—	50	—	μV/V
Noise (Pk - Pk value not exceeded 95% of time)	V_{IN} = 0V Full Scale = 200.0 mV	—	15	—	μV
Leakage Current @ Input	V_{IN} = 0V	—	1	10	pA
Zero Reading Drift	V_{IN} = 0 $0° < T_A < 70°C$	—	0.2	1	μV/°C
Scale Factor Temperature Coefficient	V_{IN} = 199.0 mV $0 < T_A < 70°C$ (Ext. Ref. 0 ppm/°C)	—	1	5	ppm/°C
Supply Current (Does not include Common current)	V_{IN} = 0 (Note 6)	—	50	100	μA
Analog Common Voltage (with respect to positive supply)	250KΩ between Common and positive supply	2.4	2.8	3.2	V
Temp. Coeff. of Analog Common (with respect to positive supply)	250KΩ between Common and positive supply	—	80	—	ppm/°C
Pk-Pk Segment Drive Voltage (Note 5)	V^+ to V^- = 9V	4	5	6	V
Pk-Pk Backplane Drive Voltage (Note 5)	V^+ to V^- = 9V	4	5	6	V
Power Dissipation Capacitance	vs. Clock Frequency	—	40	—	pF

Notes:
1. Input voltages may exceed the supply voltages provided the input current is limited to ±100 μA.
2. Dissipation rating assumes device is mounted with all leads soldered to printed circuit board.
3. Unless otherwise noted, specifications apply at T_A = 25° C. f_{CLOCK} = 16 kHz and are tested in the circuit of Figure 1.
4. Refer to "Differential Input" discussion on page 4.
5. Backplane drive is in phase with segment drive for 'off' segment, 180° out of phase for 'on' segment. Frequency is 20 times conversion rate. Average DC component is less than 50 mV.
6. During auto-zero phase, current is 10-20 μA higher. 48 kHz oscillator, Figure 2, increases current by 8 μa (typ.).

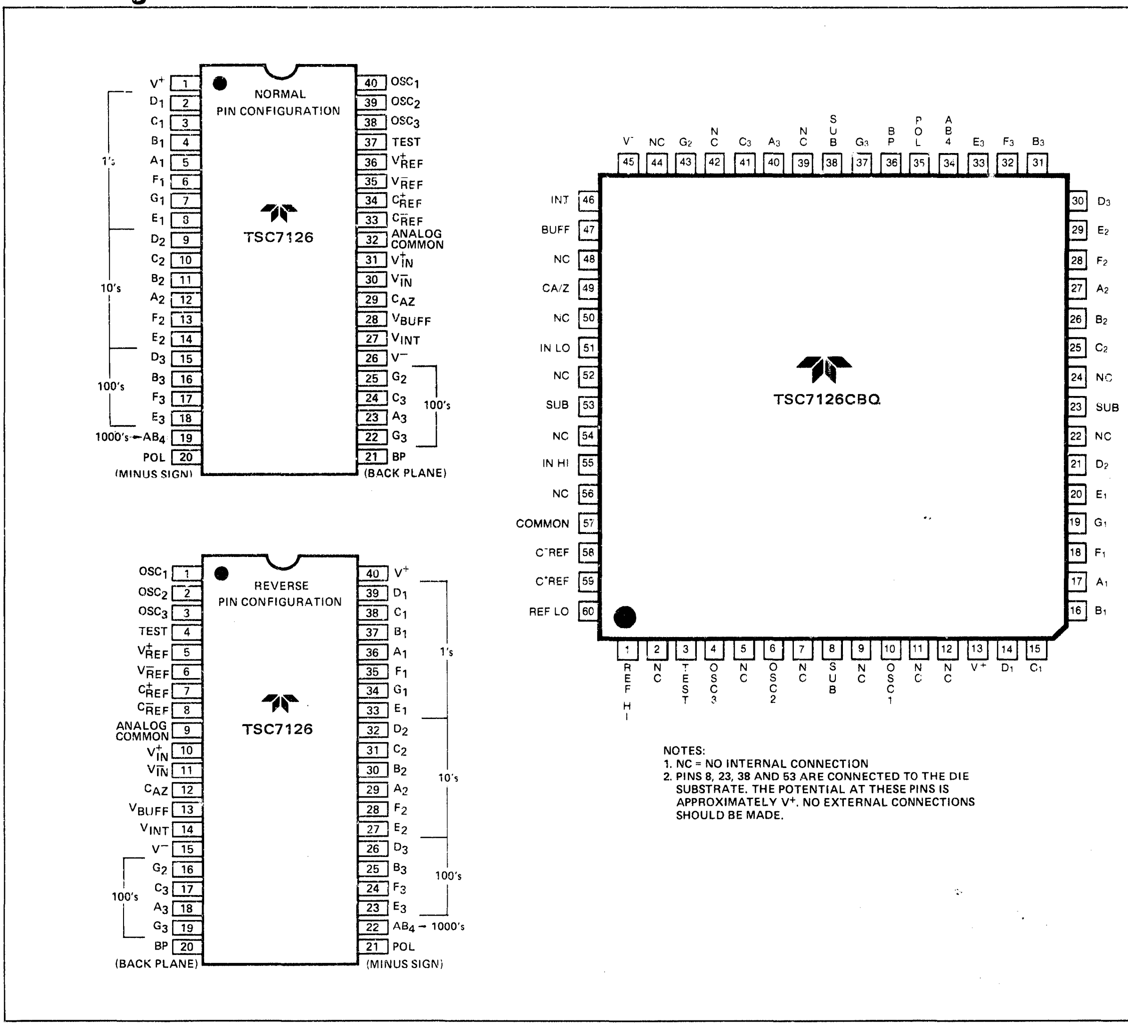
* Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may effect device reliability.

Ordering Information

Part No.	Package	Pin Layout	Temp. Range
TSC7126CPL	40-Pin Plastic Dip	Normal	0°C to 70°C
TSC7126RCPL	40-Pin Plastic Dip	Reversed	0°C 70°C
TSC7126IJL	40-Pin CerDIP	Normal	-25°C to +85°C
TSC7126CBQ	60-Pin Plastic Flat	Formed Leads	0°C to 70°C

Part No.	Package	Pin Layout	Temp. Range
TSC7126CSQ	60-Pin Plastic Flat	Unformed Leads	0°C to 70°C
Devices with 160 Hour, +125°C Burn-In			
TSC7126CPL/BI	40-Pin Plastic Dip	Normal	0°C to 70°C
TSC7126IJL/BI	40-Pin CerDIP	Normal	-25°C to +85°C

Pin Configuration



Pin Description

40-Pin DIP Pin Number Normal	(Reverse)	60-Pin Flat Package Pin Number	Name	Description
1	(40)	13	V^+	Positive supply voltage.
2	(39)	14	D_1	Activates the D section of the units display.
3	(38)	15	C_1	Activates the C section of the units display.
4	(37)	16	B_1	Activates the B section of the units display.
5	(36)	17	A_1	Activates the A section of the units display.
6	(35)	18	F_1	Activates the F section of the units display.
7	(34)	19	G_1	Activates the G section of the units display.
8	(33)	20	E_1	Activates the E section of the units display.

Pin Description (Cont.)

40-Pin DIP Pin Number Normal	(Reverse)	60-Pin Flat Package Pin Number	Name	Description
9	(32)	21	D_2	Activates the D section of the tens display.
10	(31)	25	C_2	Activates the C section of the tens display.
11	(30)	26	B_2	Activates the B section of the tens display.
12	(29)	27	A_2	Activates the A section of the tens display.
13	(28)	28	F_2	Activates the F section of the tens display.
14	(27)	29	E_2	Activates the E section of the tens display.
15	(26)	30	D_3	Activates the D section of the hundreds display.
16	(25)	31	B_3	Activates the B section of the hundreds display.
17	(24)	32	F_3	Activates the F section of the hundreds display.
18	(23)	33	E_3	Activates the E section of the hundreds display.
19	(22)	34	AB_4	Activates both halves of the 1 in the thousands display.
20	(21)	35	POL	Activates the negative polarity display.
21	(20)	36	BP	Backplane drive output.
22	(19)	37	G_3	Activates the G section of the hundreds display.
23	(18)	40	A_3	Activates the A section of the hundreds display.
24	(17)	41	C_3	Activates the C section of the hundreds display.
25	(16)	43	G_2	Activates the G section of the tens display.
26	(15)	45	V^-	Negative power supply voltage.
27	(14)	46	V_{INT}	The integrating capacitor should be selected to give the maximum voltage swing that ensures component tolerance build up will not allow the integrator output to saturate. When analog common is used as a reference and the conversion rate is 3 readings per second, a 0.047 μF capacitor may be used. The capacitor must have a low dielectric constant to prevent roll-over errors. See INTEGRATING CAPACITOR section for additional details.
28	(13)	47	V_{BUFF}	Integration resistor connection. Use a 180 kΩ for a 200 mV full-scale range and a 1.80 MΩ for 2 V full-scale range.
29	(12)	49	C_{AZ}	The size of the auto-zero capacitor influences the system noise. Use a 0.33 μF capacitor for a 200 mV full-scale, and a 0.033 μF capacitor for a 2 volt full-scale. See paragraph on AUTO-ZERO CAPACITOR for more details.
30	(11)	51	V_{IN}^-	The low input is connected to this pin.
31	(10)	55	V_{IN}^+	The high input signal is connected to this pin.
32	(9)	57	Analog Common	This pin is primarily used to set the analog common-mode voltage for battery operation or in systems where the input signal is referenced to the power supply. See paragraph on ANALOG COMMON for more details. It also acts as a reference voltage source.
33	(8)	58	C_{REF}^-	See pin 34.
34	(7)	59	C_{REF}^+	A 0.1 μF capacitor is used in most applications. If a large common mode voltage exists (for example the V_{IN}^- pin is not at analog common), and a 200 mV scale is used, a 1.0 μF is recommended and will hold the rollover error to 0.5 count.
35	(6)	60	V_{REF}^-	See pin 36.
36	(5)	1	V_{REF}^+	The analog input required to generate a full-scale output (1,999 counts). Place 100 mV between pins 35 and 36 for 199.9 mV full-scale. Place 1.00 volts between pins 35 and 36 for 2 volts full-scale. See paragraph on REFERENCE VOLTAGE.
37	(4)	3	Test	Lamp test. When pulled high (to V^+) all segments will be turned on and the display should read -1888. It may also be used as a negative supply for externally generated decimal points. See paragraph under TEST for additional information.
38	(3)	4	OSC_3	See pin 40.
39	(2)	6	OSC_2	See pin 40.
40	(1)	10	OSC_1	Pins 40, 39, 38 make up the oscillator section. For a 48 kHz clock (3 readings per section) connect pin 40 to the junction of a 180 kΩ resistor and a 50 pF capacitor. The 180 kΩ resistor is tied to pin 39 and the 50 pF capacitor is tied to pin 38.

Detailed Description

ANALOG SECTION

Figure 3 shows the Block Diagram of the Analog Section for the 7126. Each measurement cycle is divided into three phases. They are (1) auto-zero (A-Z), (2) signal integrate (INT) and (3) de-integrate, (DE).

1. Auto-zero phase

Input high and low are disconnected from the pins and internally shorted to analog COMMON. The reference capacitor is charged to the reference voltage. A feedback loop is closed around the system to charge the auto-zero capacitor C_{AZ} to compensate for offset voltages in the buffer amplifier, integrator, and comparator. Since the comparator is included in the loop, the A-Z accuracy is limited only by the noise of the system. The offset referred to the input is less than 10µV.

2. Signal Integrate phase

The auto-zero loop is opened, the internal short is removed, and the internal input high and low are connected to the external pins. The converter then integrates the differential voltage between IN HI and IN LO for a fixed time. This differential voltage can be within a wide common mode range; within one volt of either supply. If, on the other hand, the input signal has no return with respect to the converter power supply, IN LO can be tied to analog COMMON to establish the correct common-mode voltage. At the end of this phase, the polarity of the integrated signal is determined.

3. De-integrate Phase

The final phase is reference integrate or de-integrate. Input low is internally connected to analog common and input high is connected across the previously charged reference capacitor. Circuitry within the chip ensures that the capacitor will be connected with the correct polarity to cause the integrator output to return to zero. The time required for the output to return to zero is proportional to the input signal. The digital reading displayed is

$$1000 \times \frac{V_{IN}}{V_{REF}}$$

Differential Reference

The reference voltage can be generated anywhere within the power supply voltage of the converter. The main source of common mode error is a roll-over voltage caused by the reference capacitor losing or gaining charge to stray capacity on its nodes. If there is a large common mode voltage, the reference capacitor can gain charge (increase voltage) when called up to de-integrate a positive signal but lose charge (decrease voltage) when called up to deintegrate a negative input signal. This difference in reference for (+) or (—) input voltage will give a roll-over error. However, by selecting the reference capacitor large enough in comparison to the stray capacitance, this error can be held to less than 0.5 count for the worst case condition. See Component Values Selection.

Differential Input

The input can accept differential voltages anywhere within the common mode range of the input amplifier; or specifically from 1.0 volts below the positive supply to 1.0 volt above the negative supply. In this range the system has a CMRR of 86 dB typical. However, since the integrator also swings with the common mode voltage, care must be exercised to assure the integrator output does not saturate. A worst case condition would be a large positive common-mode voltage with a near full-scale negative differential input voltage. The negative input signal drives the integrator

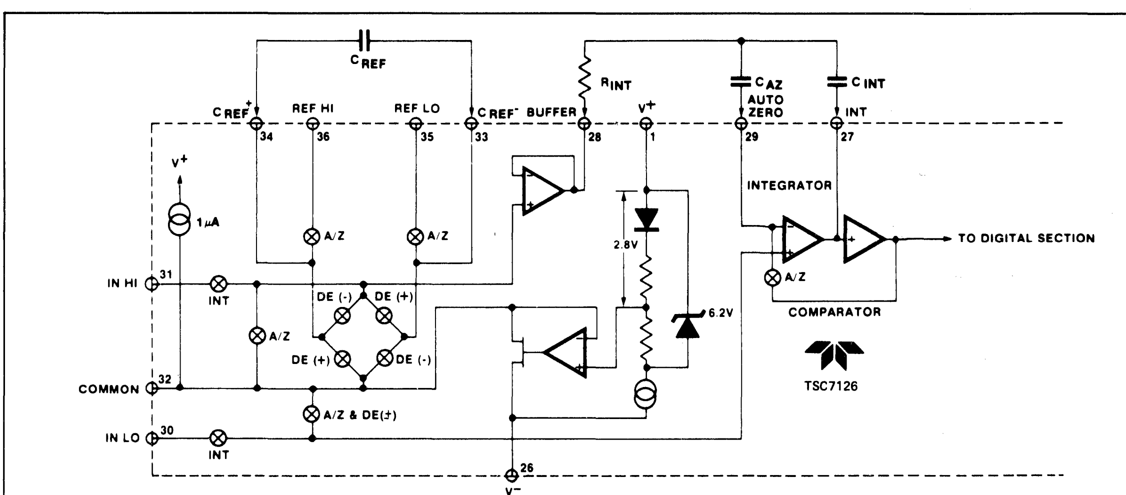


Figure 3: Analog Section of TSC7126.

positive when most of its swing has been used up by the positive common mode voltage. For these critical applications the integrator swing can be reduced to less than the recommended 2V full scale swing with little loss of accuracy. The integrator output can swing within 0.3 volts of either supply without loss of linearity.

Analog Common

This pin is included primarily to set the common mode voltage for battery operation or for any system where the input signals are floating with respect to the power supply. The common pin sets a voltage that is approximately 2.8 volts more negative than the positive supply. This is selected to give a minimum end-of-life battery voltage of about 6V. However, the analog common has some of the attributes of a reference voltage. When the total supply voltage is large enough to cause the zener to regulate (>7V), the common voltage will have a low voltage coefficient (0.001%/%), low output impedance (≈15Ω), and a temperature coefficient typically less than 80 ppm/°C.

An external reference may be added to improve temperature stability. The circuit is shown in Figure 4.

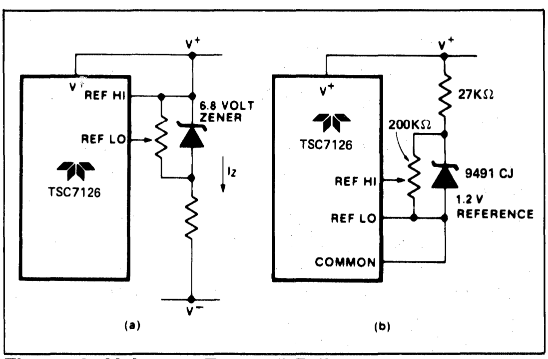


Figure 4: Using an External Reference

Analog common is also used as the IN LO return during auto-zero and de-integrate. If IN LO is different from analog COMMON, a common mode voltage exists in the system and is taken care of by the excellent CMRR of the converter. However, in some applications IN LO will be set at a fixed known voltage (power supply common for instance). In this application, analog COMMON should be tied to the same point, thus removing the common mode voltage from the converter. The same holds true for the reference voltage. If reference can be conveniently referenced to analog COMMON, it should be since this removes the common mode voltage from the reference system.

Within the IC analog COMMON is tied to an N-channel FET that can sink 100 μA or more of current to hold the voltage 2.8 volts below the positive supply (when a load is trying to pull the common line positive). However, there is only 1 μA of source current, so COMMON may easily be tied to a more negative voltage thus over-riding the internal reference.

Test

The TEST pin serves two functions. It is coupled to the internally generated digital supply through a 500Ω resistor. Thus it can be used as the negative supply for externally generated segment drivers such as decimal points or any other presentation the user may want to include on the LCD display. No more than a 1 mA load should be applied. Figures 5 and 6 show such an application.

The second function is a "lamp test". When TEST is pulled high (to V^+) all segments will be turned on and the display should read - 1888. The TEST pin will sink about 10 mA under these conditions.

Caution: In the lamp test mode, the segments have a constant d-c voltage (no square-wave) and may burn the LCD display if left in this mode for several minutes.

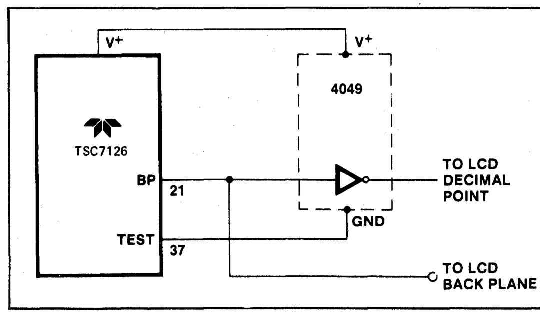


Figure 5: Simple Inverter for Fixed Decimal Point

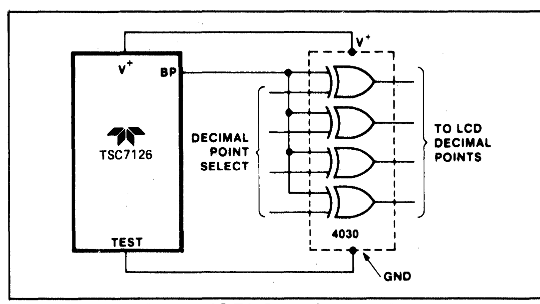


Figure 6: Exclusive 'OR' Gate for Decimal Point Drive

DIGITAL SECTION

Figure 8 shows the digital section for the 7126. An internal digital ground is generated from a 6 volt Zener diode and a large P channel source follower. This supply is made stiff to absorb the relative large capacitive currents when the backplane (BP) voltage is switched. The BP frequency is the clock frequency divided by 800. For three readings/second this is a 60 Hz square wave with a nominal amplitude of 5 volts. The segments are driven at the same frequency and amplitude and are in phase with

BP when OFF, but out of phase when ON. In all cases, negligible d-c voltage exists across the segments. The polarity indication is "ON" for negative analog inputs. If IN LO and IN HI are reversed, this indication can be reversed also, if desired.

System Timing

Three clocking methods may be used: (Figure 7)

1. An external oscillator connected to pin 40.
2. A crystal between pins 39 and 40.
3. An R-C oscillator using all three pins.

The oscillator frequency is divided by four before it clocks the decade counters. It is then further divided to form the three convert-cycle phases. These are signal integrate (1000 counts), reference de-integrate (0 to 2000 counts) and auto-zero (1000 to 3000 counts). For signals less than full scale, auto-zero gets the unused portion of reference integrate. This makes a complete measure cycle of 4,000 (16,000 clock pulses) independent of input voltage. For three readings/second, an oscillator frequency of 48 kHz would be used.

To achieve maximum rejection of 60 Hz pickup, the signal integrate cycle should be a multiple of 60 Hz. Oscillator frequencies of 60 kHz, 48 kHz, 40 kHz, 33-1/3 kHz, etc. should be selected. For 50 Hz rejection, Oscillator frequencies of 66-2/3 kHz, 50 kHz, 40 kHz, etc. would be suitable. Note that 40 kHz (2.5 readings/second) will reject both 50 and 60 Hz (also 400 and 440 Hz).

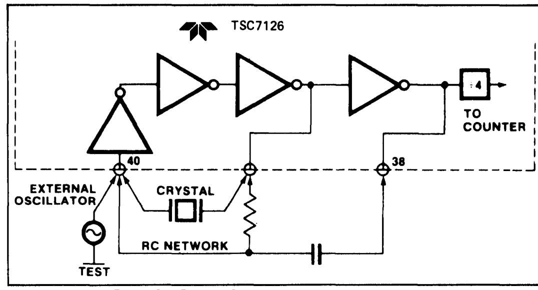


Figure 7: Clock Circuits

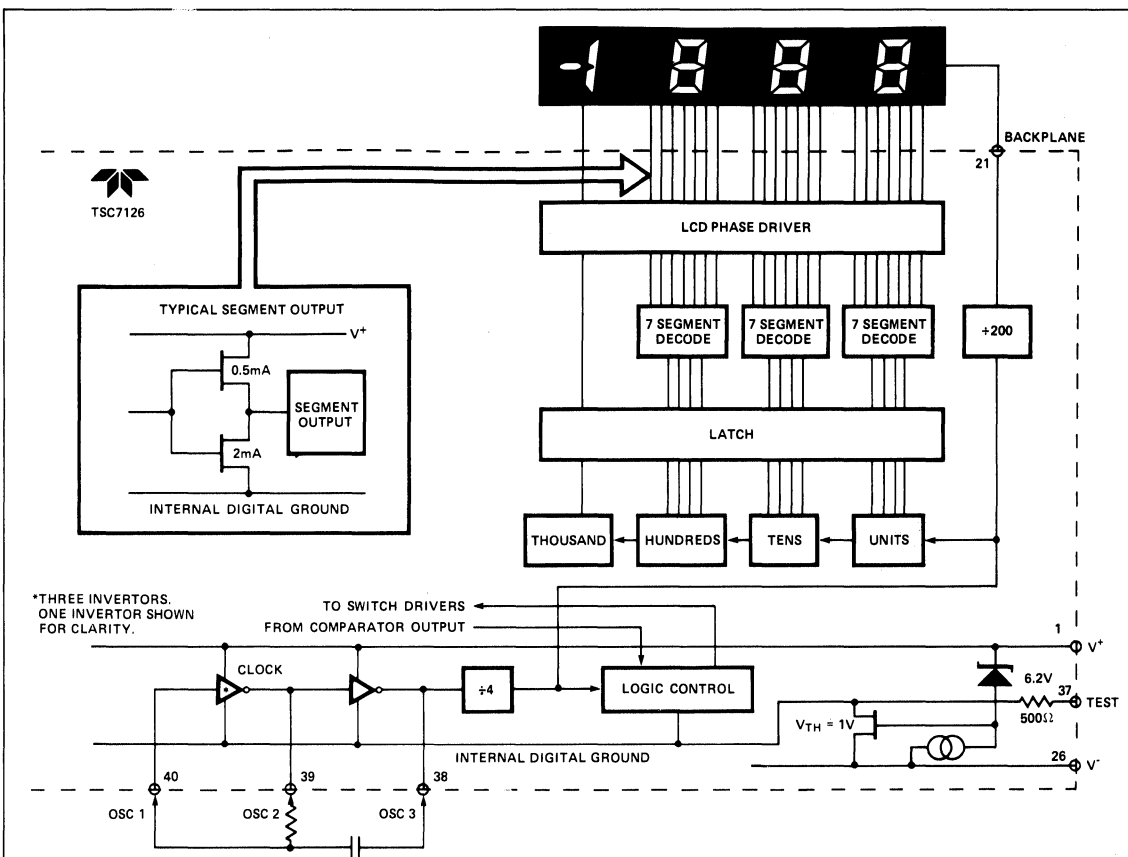


Figure 8: Digital Section

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Component Value Selection

1. Auto-zero Capacitor

The size of the auto-zero capacitor has some influence on the noise of the system. For 200 mV full scale where noise is very important, a 0.33 μF capacitor is recommended. On the 2 volt scale, a 0.033 μF capacitor increases the speed of recovery from overload and is adequate for noise on this scale.

2. Reference Capacitor

A 0.1 μF capacitor is acceptable in most applications. However, where a large common mode voltage exists (i.e. the REF LO pin is not at analog COMMON) and a 200 mV scale is used, a larger value is required to prevent roll-over error. Generally 1.0 μF will hold the roll-over error to 0.5 count in this instance.

3. Integrating Capacitor

The integrating capacitor should be selected to give the maximum voltage swing that ensures tolerance build-up will not saturate the integrator swing (approx. 0.3 volt from either supply). When the analog COMMON is used as a reference, a nominal ±2 volt full scale integrator swing is acceptable). For three readings/second (48 kHz clock) nominal value for C_{INT} is 0.047 μF, for one reading per second (16 kHz) use 0.15 μF.

If different oscillator frequencies are used, these values should be changed in inverse proportion to maintain the output swing.

The integrating capacitor must have low dielectric absorption to prevent roll-over errors. Polypropylene capacitors are recommended for this application.

At three readings/sec., a 750Ω resistor should be placed in series with the integrating capacitor, to compensate for comparator delay.

4. Integrating Resistor

Both the buffer amplifier and the integrator have a class A output stage with 6 μA of quiescent current. They can supply ~1 μA of drive current with negligible non-linearity. The integrating resistor should be large enough to remain in this very linear region over the input voltage range, but small enough that undue leakage requirements are not placed on the PC board. For 2 volt full scale, 1.8 MΩ is near optimum and similarly 180 KΩ for a 200.0 mV scale.

5. Oscillator Components

For all ranges of frequency a 50 pF capacitor is recommended and the resistor is selected from the approximate equation $f \sim \frac{45}{RC}$. For 48 kHz clock (3 readings/second), R = 180 KΩ.

6. Reference Voltage

The analog input required to generate full-scale output (2000 counts) is: $V_{IN} = 2 V_{REF}$. Thus, for the 200.0 mV and 2.000 volt scale, V_{REF} should equal 100.0 mV and 1.000 volt, respectively. However, in many applications where the A/D is connected to a transducer, there will exist a scale factor other than unity between the input voltage and the digital reading. For instance, in a weighing system, the designer might like to have a full scale reading when the voltage from the transducer is 0.682V. Instead of dividing the input down to 200.0 mV, the designer should use the input voltage directly and select V_{REF} = 0.341V. A suitable value for integrating resistor would be 330 KΩ. This makes the system slightly quieter and also avoids the necessity of a divider network on the input. Another advantage of this system occurs when a digital reading of zero is desired for $V_{IN} \neq 0$. Temperature and weighing systems with a variable tare are examples. This offset reading can be conveniently generated by connecting the voltage transducer between IN HI and COMMON and the variable (or fixed) offset voltage between COMMON and IN LO.

Typical Applications

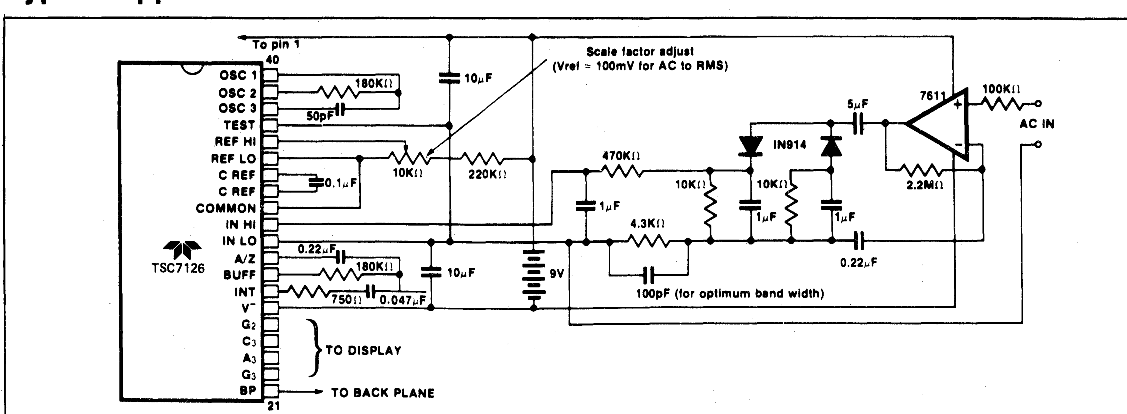

Figure 9: AC to DC Converter with TSC7126. Test is Used as a Common Mode Reference Level to Ensure Compatibility with Most Op-amps.

Typical Applications (Cont.)

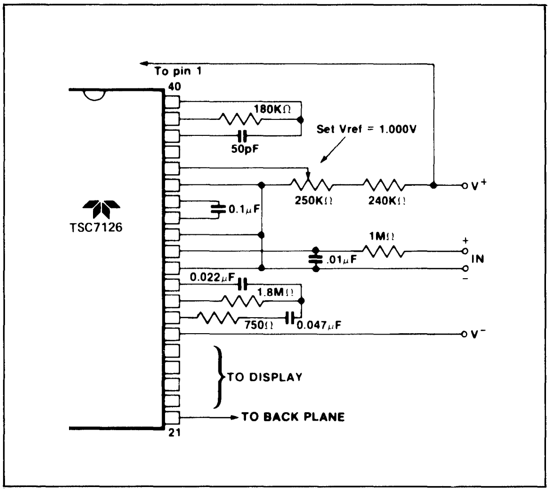

Figure 10: Recommended Values for 2.000 V Full-Scale, Three Readings Per Second.

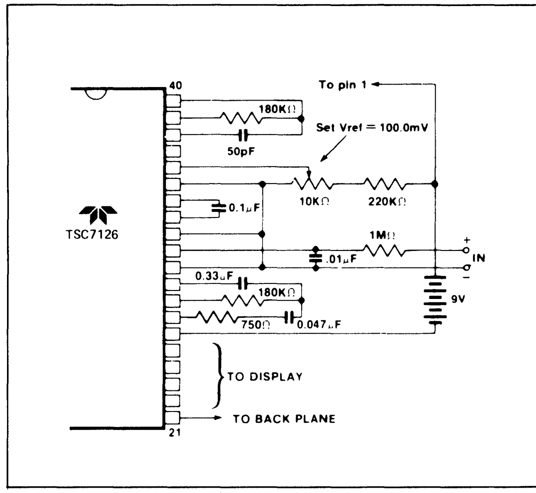

Figure 12: TSC7126 Using the Internal Reference. 200.0 mV Full-Scale, Three Readings Per Second, Floating Supply Voltage (9 V Battery).

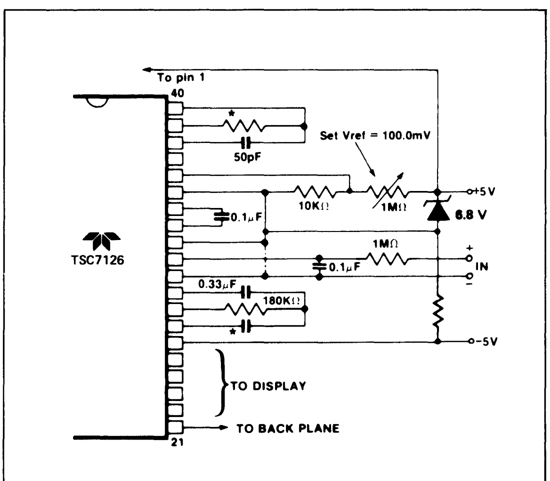

Figure 11: TSC7126 with Zener Diode Reference.

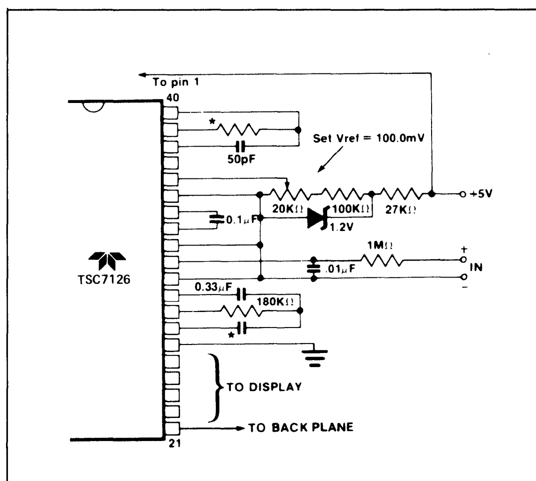

Figure 13: TSC7126 Operated From Single +5 V Supply. An External Reference Must Be Used.

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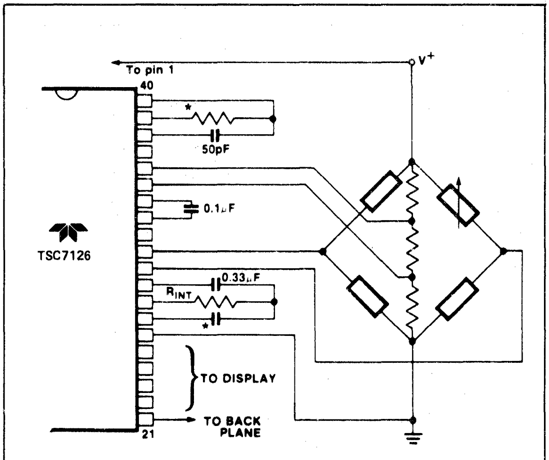
Typical Applications (Cont.)



*Values depend on clock frequency. See Figure 10, 12, 15.

Figure 14: TSC7126 Measuring Ratiometric Values of Quad Load Cell. The Resistor Values Within the Bridge are Determined by the Desired Sensitivity.

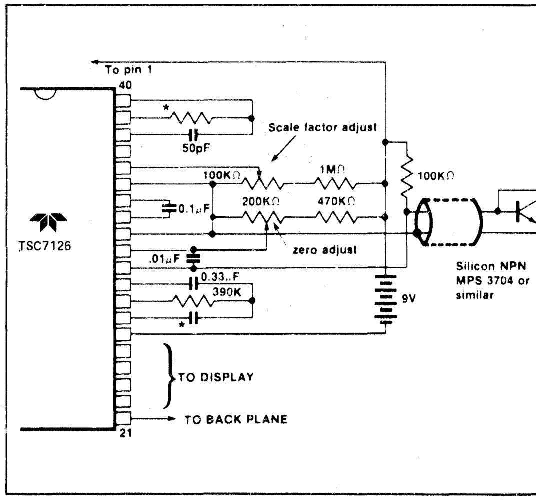


Figure 16: TSC7126 Used as a Digital Centigrade Thermometer. A Silicon Diode-Connected Transistor Has a Temperature Coefficient of About 2 mV/° C.

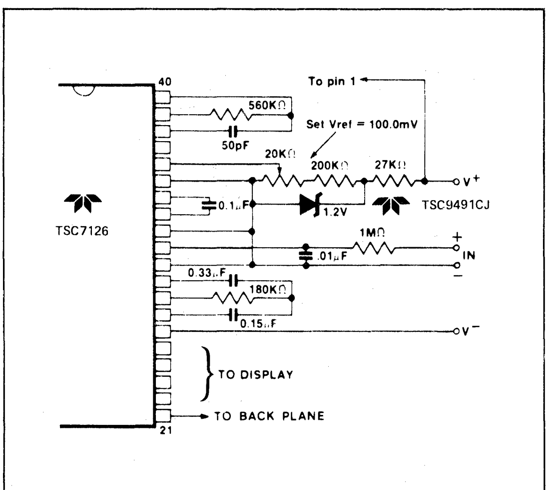


Figure 15: TSC7126 With an External Band-Gap Reference (1.2 V Typ) IN LO Is Tied to Common. Values Shown are for One Reading Per Second.

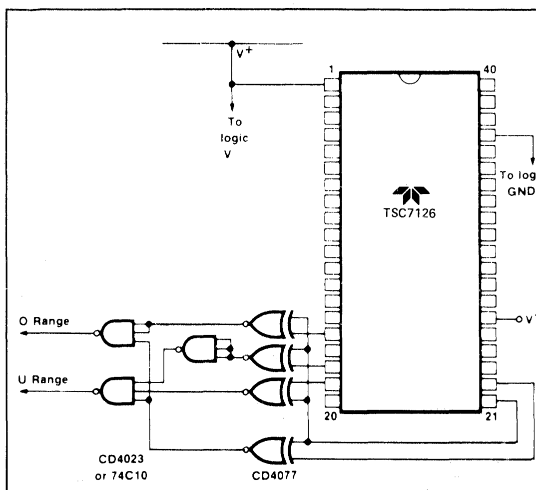
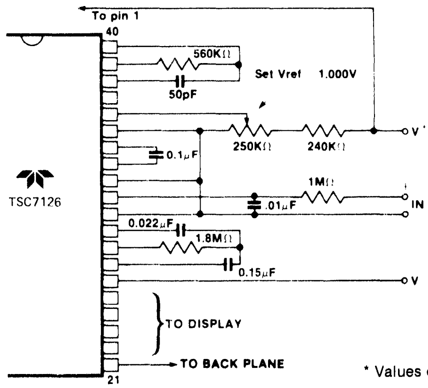


Figure 17: Circuit for Developing Underrange and Overrange Signals from TSC7126 Outputs.

Typical Applications (Cont.)

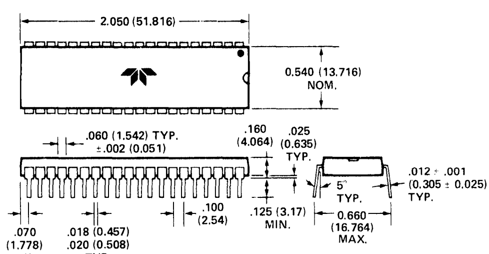


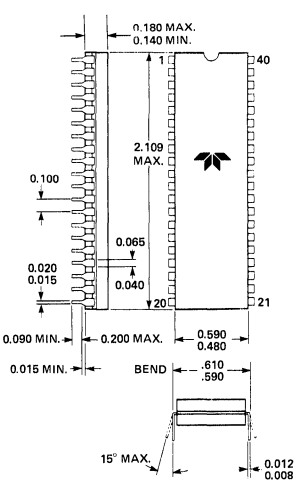
* Values depend on clock frequency. See Figure 10, 12, 15.

Figure 18: Recommended Component Values for 2.00 V Full-Scale, One Reading Per Second.

Package Information

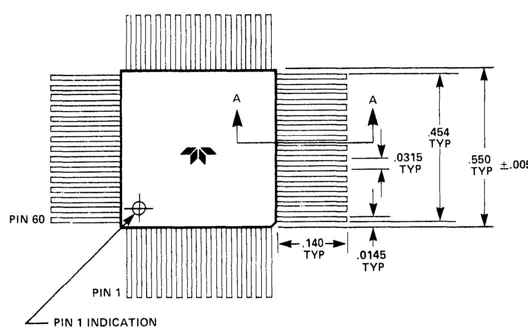
(Package #17)
40-Pin Plastic Dip (PL Package)



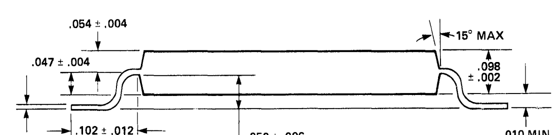


(Package #20)
40-Pin CerDIP

60-Pin Flat Package



"SQ" Package - Unformed Leads
(Package #22)



"BQ" Package - Formed Leads
(Package #21)