VINETIC®-CPE

Voice over IP Processor for Customer Premises Equipment

VINETIC®-2CPE (PEB/PEF 3332), Version 2.2
VINETIC®-1CPE (PEB/PEF 3331), Version 2.2

Preliminary

Data Sheet

Revision 2.0

Communication Solutions

Never stop thinking

Edition 2007-04-17

Published by
Infineon Technologies AG
81726 München, Germany

Legal Disclaimer

The information given in this document shall in no event be regarded as a guarantee of conditions or characteristics (“Beschaffenheitsgarantie”). With respect to any examples or hints given herein, any typical values stated herein and/or any information regarding the application of the device, Infineon Technologies hereby disclaims any and all warranties and liabilities of any kind, including without limitation warranties of non-infringement of intellectual property rights of any third party.

Information

For further information on technology, delivery terms and conditions and prices please contact your nearest Infineon Technologies Office (**www.infineon.com**).

Warnings

Due to technical requirements components may contain dangerous substances. For information on the types in question please contact your nearest Infineon Technologies Office.

Infineon Technologies Components may only be used in life-support devices or systems with the express written approval of Infineon Technologies, if a failure of such components can reasonably be expected to cause the failure of that life-support device or system, or to affect the safety or effectiveness of that device or system. Life support devices or systems are intended to be implanted in the human body, or to support and/or maintain and sustain and/or protect human life. If they fail, it is reasonable to assume that the health of the user or other persons may be endangered.

Voice and Internet Enhanced Telephony Interface Circuit
CONFIDENTIAL
Revision History: 2007-04-17, Revision 2.0

Previous Version: VINETIC®-2CPE/-1CPE (PEB/PEF 3332/-3331) Version 2.2 Prel. Data Sheet Rev. 1.0, 2007-07-07

Page	Subjects (major changes since last revision)
8,10,60,61	Packages PG-TQFP-64-8 & PG-TQFP-100-3 removed
32	Description of MCLK pin updated to reflect lack of internal Schmitt trigger and therefore no input hysteresis
63	Literature references updated

Table of Contents

List of Figures

List of Tables

Preface

This Preliminary Data Sheet describes the VINETIC®-2CPE/-1CPE, a member of the Voice and Internet Enhanced Telephony Interface Circuit (VINETIC®) chip set family. The VINETIC®-2CPE/-1CPE includes two/one analog lines connected via two/one single-channel SLIC chips.

To simplify matters, the following synonyms are used:

VINETIC®

Synonym used for the CODEC versions VINETIC®-2CPE/-1CPE Version 2.2.

PG-TQFP-100

Synonym used for the package PG-TQFP-100-18

PG-TQFP-64

Synonym used for the package PG-TQFP-64-17

SLIC

Synonym used for SLIC-DC Version 1.2 and SLIC-E/TSLIC-E Version 2.1.

Attention: TSLIC-E (PEF 4365) is a dual channel version of the SLIC-E (PEF 4265) with identical technical specifications for each channel. Therefore, whenever SLIC-E is mentioned in the specification, TSLIC-E can also be applied.

Organization of this Document

This document is divided into 6 chapters. It is organized as follows:

- **Chapter 1**
  A general description of the chip set, key features/requirements, and typical applications.
- **Chapter 2**
  Pin layout and pin description.
- **Chapter 3**
  Description of clocking, reset behavior, and test modes.
- **Chapter 4**
  Parallel (Intel, Motorola) and serial interfaces (PCM, SCI/SPI).
- **Chapter 5**
  Electrical parameters, operating range, power consumption, symbols, limit values etc.
- **Chapter 6**
  Illustrations and dimensions of the package outlines.
- **TAPI Interface Function Call Synonyms**
  List of synonyms for refered TAPI interface function calls.
- **Literature References** and **Standards References**
  List of referenced documents.
- **Terminology**
  List of abbreviations and descriptions of symbols.

1 Overview

The VINETIC® family of devices is designed for accessing analog telephone lines. VINETIC® devices are available in different granularity (0, 1, 2, 4 and 8 analog voice channels) and with different levels of DSP performance (CPE, VIP, M, C, S). Their seamless connection to a broad range of SLICs provides the most effective solution for each application.

Executive Summary

The VINETIC® family integrates the necessary DSP and RAM/ROM for voice processing into the CODEC/SLIC chip set, thereby offering a unique set of features for Voice over Packet (VoP):

- **Cost and board space reduction** - CODEC, DSP and RAM/ROM are integrated into one small package, significantly reducing cost and board space required.
- **Scalability** - VINETIC® supports each voice channel with the necessary amount of DSP performance, due to the encapsulation of CODEC and DSP.
- **Flexibility** - The VINETIC® family provides one to eight analog ports and various levels of DSP performance, while remaining pin-compatible (only for four or eight channels, respectively) and softwarecompatible.
- **World-wide usage** - The VINETIC® can be adapted to different country requirements without hardware changes (AC and DC path, ringing, metering, etc. are programmable).
- **Future-proof** - The integrated RAM (VINETIC®-4VIP, VINETIC®-2CPE/-1CPE) for downloading advanced CODECs or its own DSP software guarantees that the system will retain state-of-the-art technology and permit future remote updates.
- Designed for Voice over Packet (**VoIP, VoDSL, Packetcable, VoATM**).

(not all features are available in all VINETIC® versions)

Voice and Internet Enhanced Telephony Interface Circuit VINETIC®-2CPE VINETIC®-1CPE

PEB/PEF 3332
PEB/PEF 3331

Version 2.2

1.1 Features VINETIC®-2CPE/-1CPE

PG-TQFP-64-17

PG-TQFP-100-18

- Fully programmable 2- and 1-channel CODEC with enhanced signal-processing capabilities
- Glueless interface to the Infineon SLIC-DC Version 1.2 and SLIC-E/TSLIC-E Version 2.1
- Green package - RoHS compliant

1.1.1 Integrated DSP Features

- Integrated VoIP DSP with RAM and software download capability
- Enhanced signal processing
- Voice coding: G.711, G.711 Annex I (Packet Loss Concealment), G.711 Annex II (VAD + CNG), G.723.1, G.726, G.729 A, B, G.729 E, iLBC royalty free vocoder
- 4(2) VoIP channels with low-bitrate vocoding implemented in 2-channel (1-channel) VINETIC®
- RTP/RTCP packetization (packetization time programmable: 5 to 30 ms encoding, 5 to 60 ms decoding)
- Voice Activity Detection (VAD)
- Comfort Noise Generation (CNG)
- Algorithms for Line Echo Cancellation (LEC) exceeding G.165, G.168, G.168-2002/2004: 4 channel Near End Line Echo Cancellation (NLEC) up to 16 ms tail length or window-based line echo cancellation up to 128 ms tail length (programmable)
- Integrated DTMF generator
- Integrated DTMF receiver
- Integrated Caller ID (with Frequency Shift Keying (FSK)) generator according to V.23 and Bell 202
- Integrated fax/modem detection, In-band tone detection
- Multi-party conferencing
- T.38 Fax relay support with V.17, V.21, V.27ter, V.29
- Voice play-out (reordering, fixed and adaptive jitter buffer up to 200 ms, clock synchronization)
- Universal Tone Generator (UTG) including all Japanese tones
- Call Progress Tone Detector
- Caller-ID Detector for V.23 and Bell 202

Product Name	Product Type	Package
VINETIC®-2CPE/-1CPE	PEB 3332 F/-3331 F	PG-TQFP-64-17
	PEF 3332 F/-3331 F	PG-TQFP-64-17
	PEB 3332 HT/-3331 HT	PG-TQFP-100-18
	PEF 3332 HT/-3331 HT	PG-TQFP-100-18

1.1.2 CODEC/SLIC Features

- Specification in accordance with ITU-T Recommendation Q.552 for interface Z [9], ETSI Standard ES 202 971 [8] and others
- Internal ringing capability
- Sinusoidal ringing
- Loop start signaling
- Polarity reversal
- Automatic modes for POTS signaling
- Line Testing according to Telcordia GR-909-CORE [10]
- DC feeding capability according to ETSI Standard ES 202971 [8] and Telcordia GR-909-CORE [10]
- On-hook transmission
- Direct connection of DAA solution possible (FXO)

1.1.3 Interface Features

- PCM interface with one PCM highway
- Serial control interface, SCI (Infineon) compatible, SPI compatible
- Parallel host interface: Intel/Motorola compatible
- JTAG interface for boundary scan

1.2 Typical Applications

The VINETIC®-2CPE/-1CPE and SLIC-DC system is dedicated primarily to Customer Premises Equipment (CPE) and provides solutions for the following applications:

Access network:

- FTTH - TDM, VoIP
- WLL - TDM, VoIP

CPE:

- Residential Gateway/Home Gateway/Internet Telephony Gateway (ITG) - VoIP
- Integrated Access Device (IAD) - VoIP
- Cable Modems/Media Terminal Adapter (MTA) - VoIP
- Analog Telephony Adapter (ATA) - VoIP
- Router - VoIP
- SOHO IP PBX

1.3 Logic Symbols

1.3.1 Logic Symbols for VINETIC®-2CPE

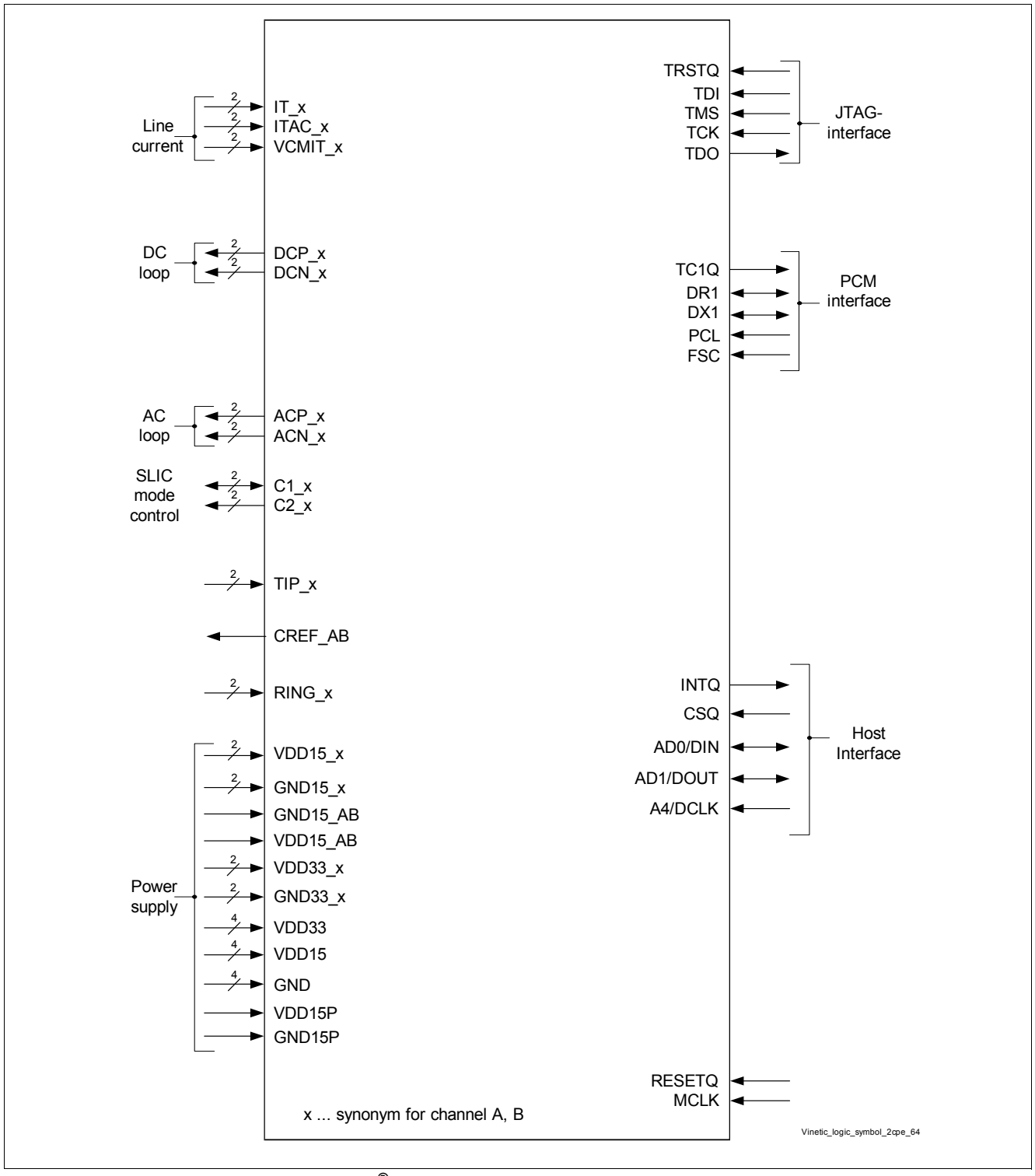

Figure 1 Logic Symbol for VINETIC®-2CPE (PG-TQFP-64)

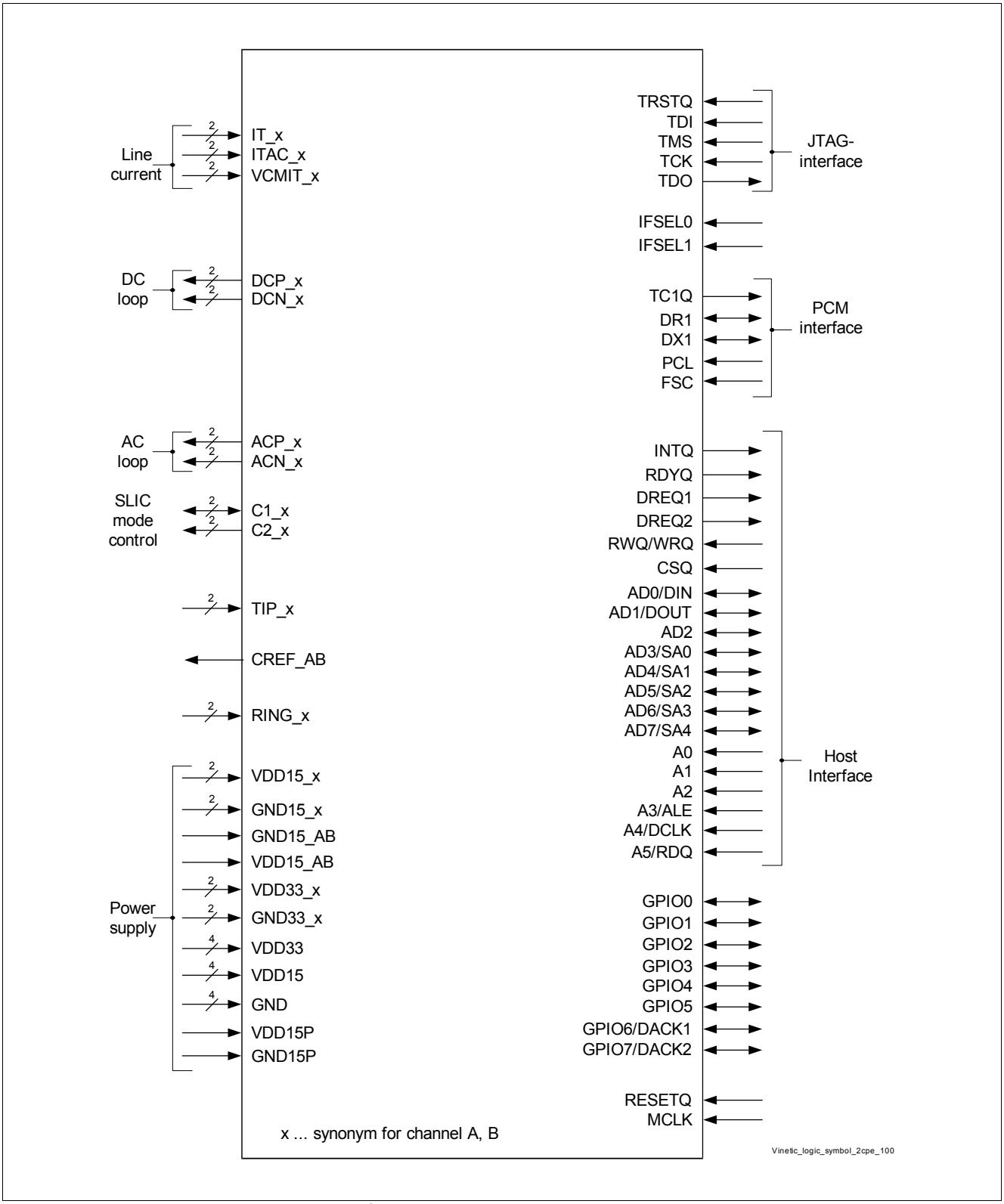

Figure 2 Logic Symbol for VINETIC®-2CPE (PG-TQFP-100)

1.3.2 Logic Symbols for VINETIC®-1CPE

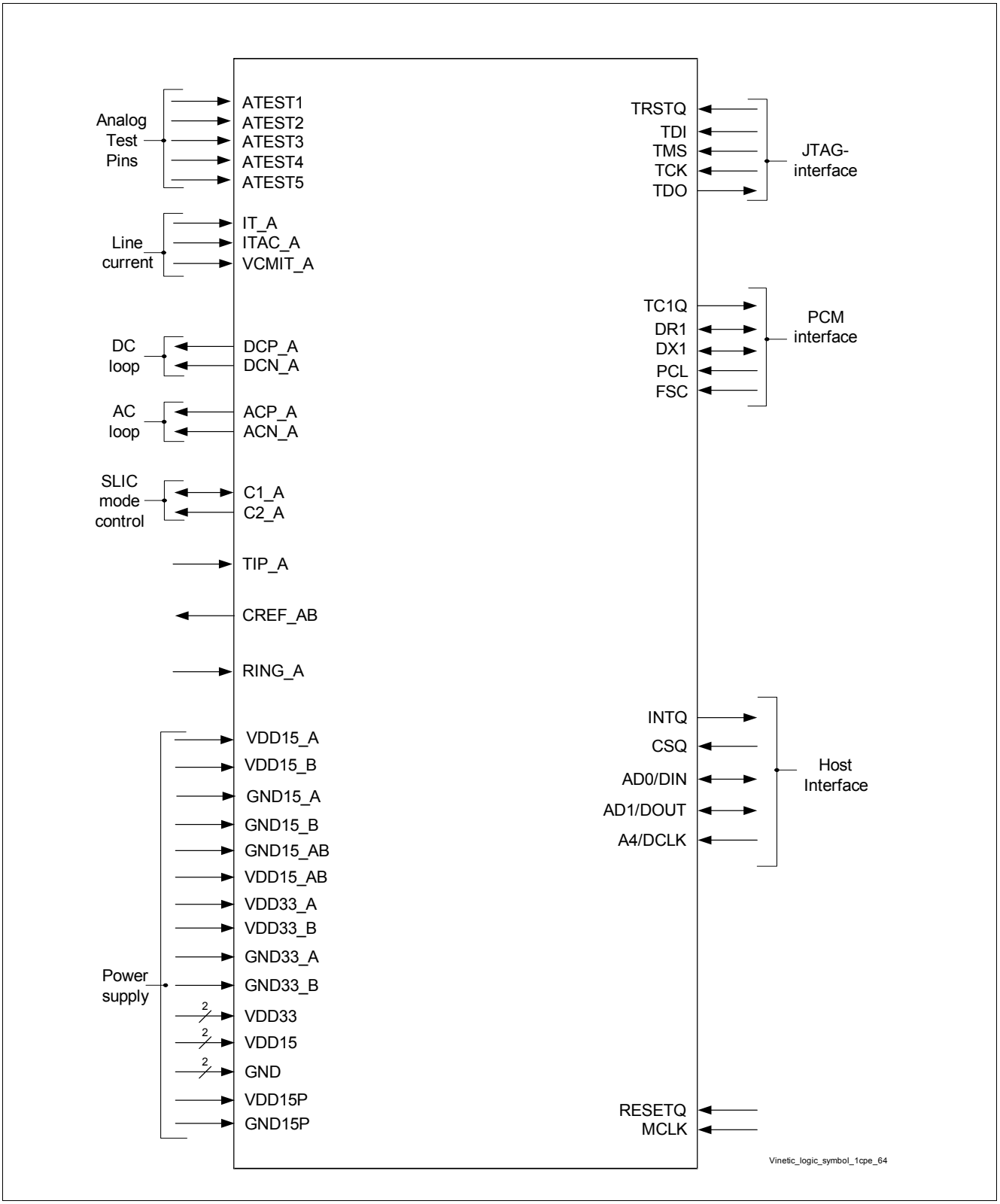

Figure 3 Logic Symbol for VINETIC®-1CPE (PG-TQFP-64)

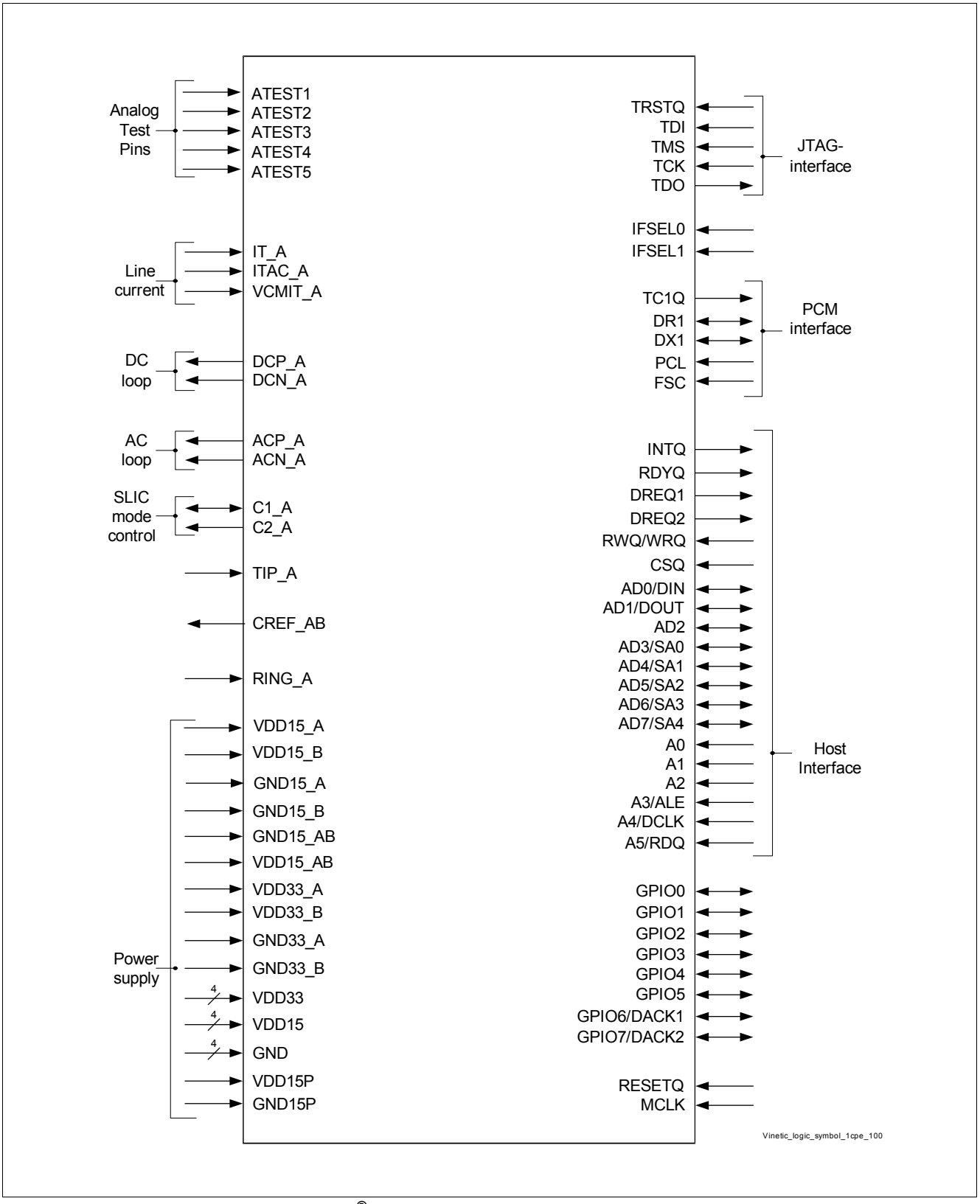

Figure 4 Logic Symbol for VINETIC®-1CPE (PG-TQFP-100)

2 Pin Description

2.1 Pin Diagrams for VINETIC®-2CPE

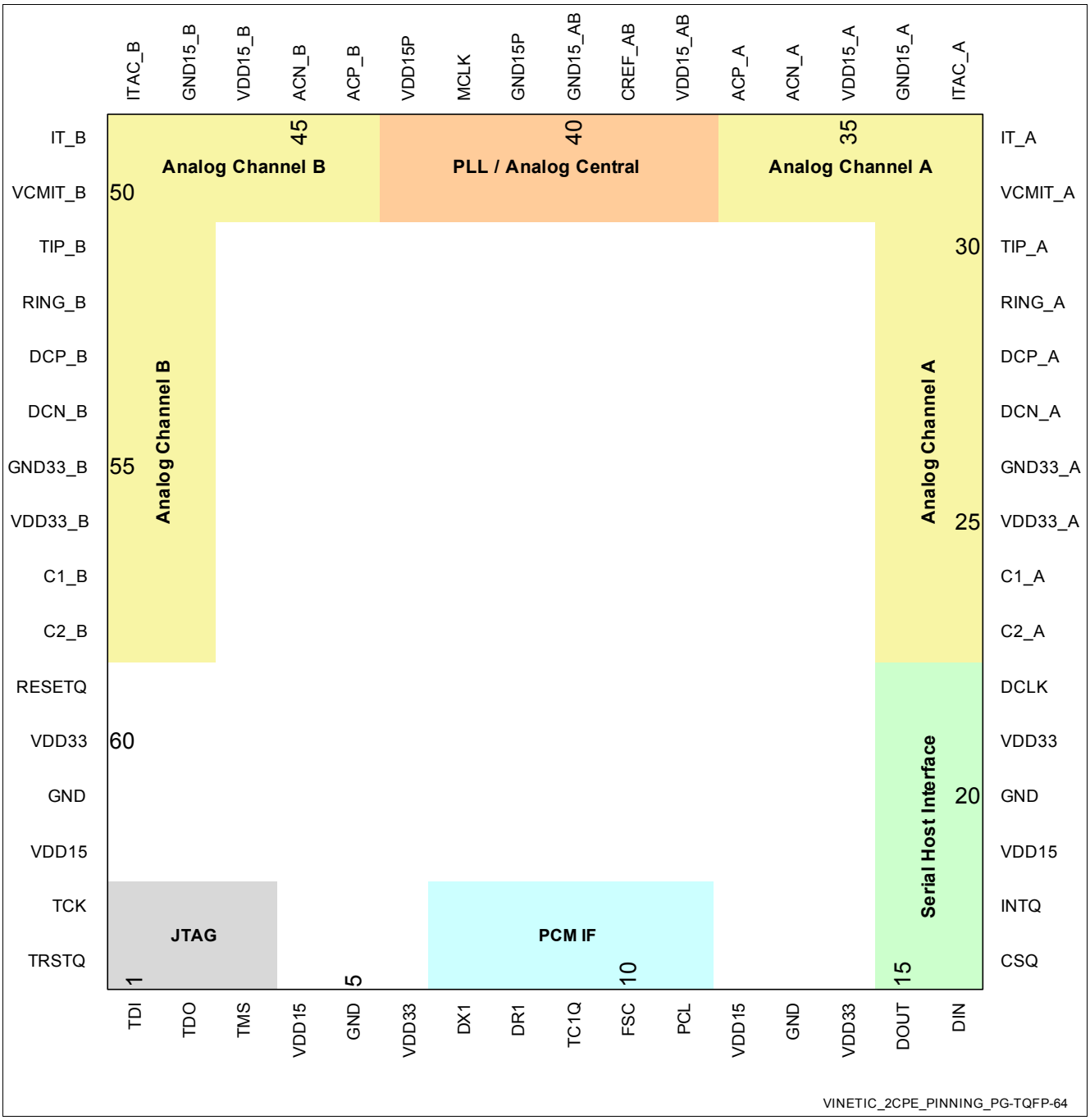

Figure 5 Pin Diagram (Top View) for VINETIC®-2CPE (PG-TQFP-64)

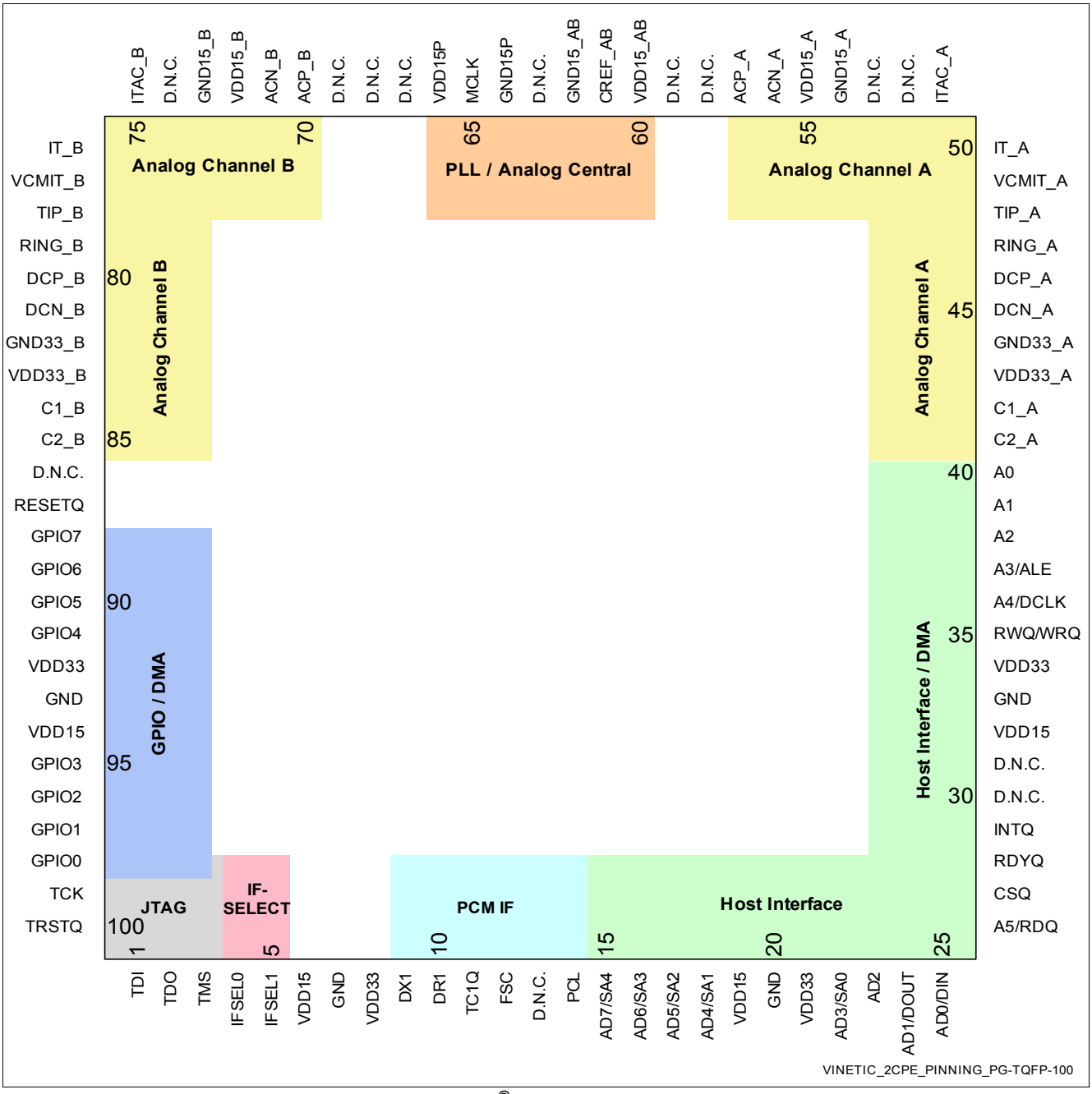

Figure 6 Pin Diagram (Top View) for VINETIC®-2CPE (PG-TQFP-100)

2.2 Pin Diagrams for VINETIC®-1CPE

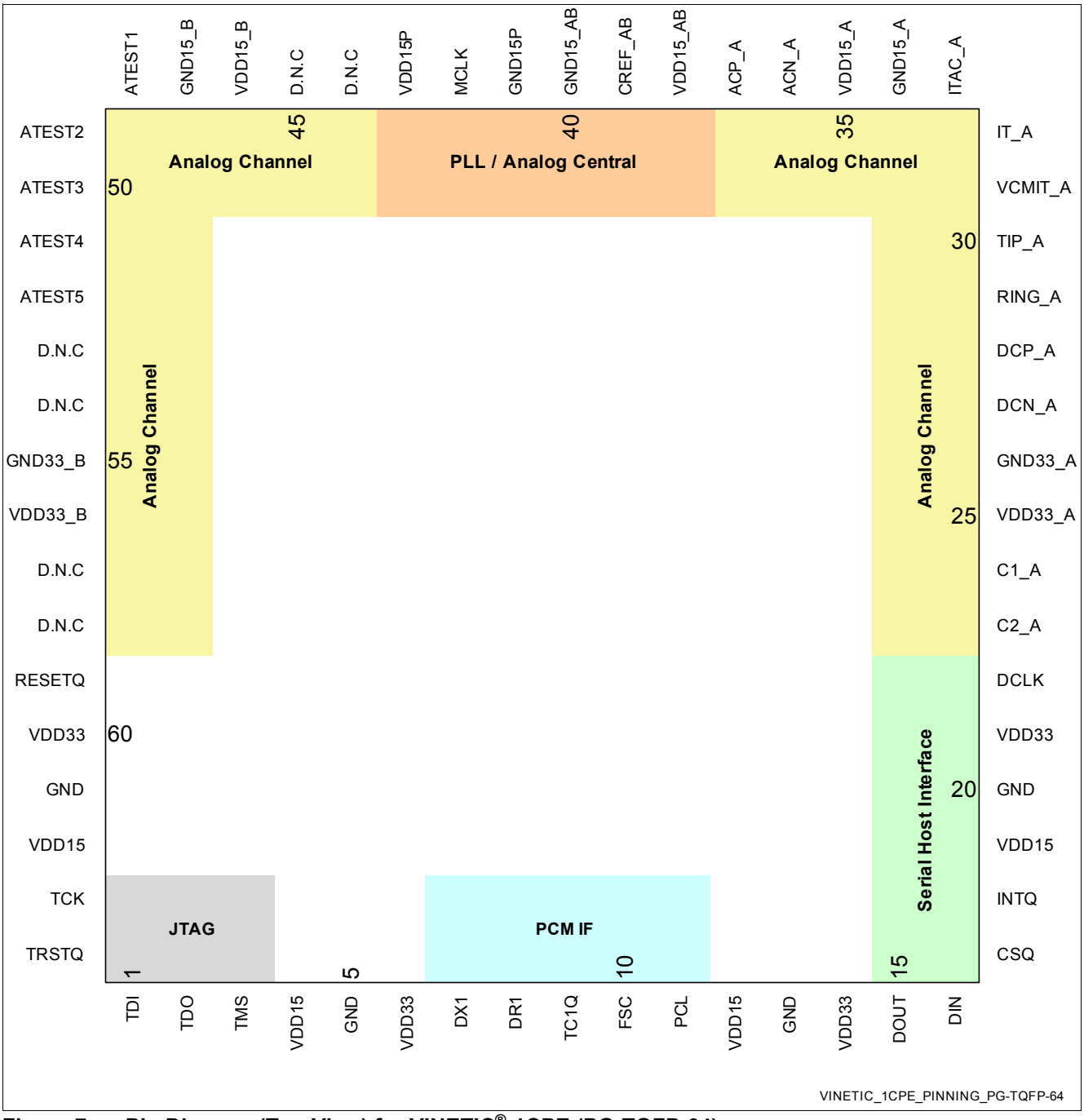

Figure 7 Pin Diagram (Top View) for VINETIC®-1CPE (PG-TQFP-64)

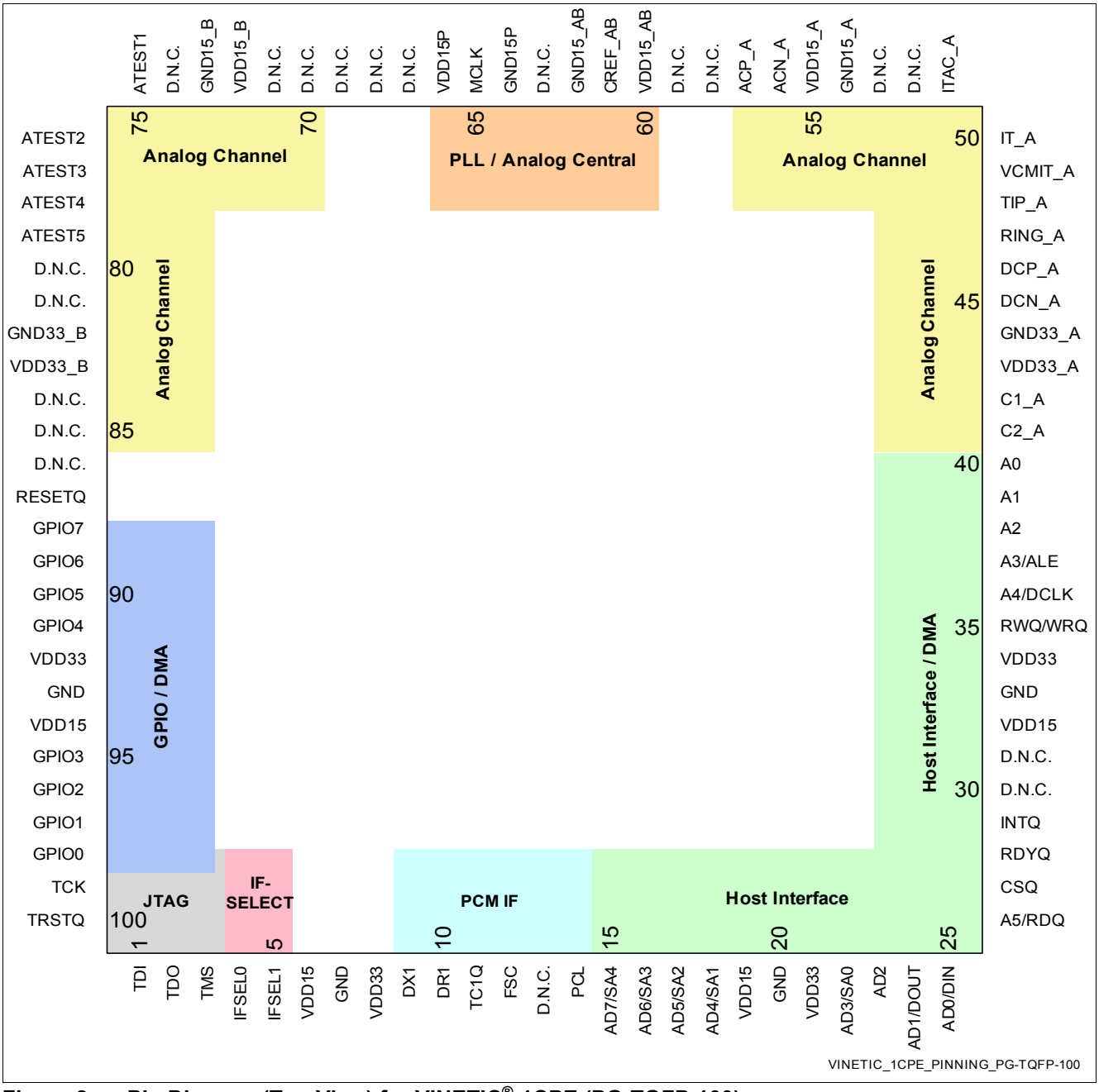

Figure 8 Pin Diagram (Top View) for VINETIC®-1CPE (PG-TQFP-100)

2.3 VINETIC®-2CPE Pins Sorted by Function

Table 1 Abbreviations for Pin Type

Abbreviations	Description
I	Standard input-only pin. Digital levels.
O	Output. Digital levels.
I/O	I/O is a bidirectional input/output signal.
AI	Input. Analog levels.
AO	Output. Analog levels.
AI/O	Input or output. Analog levels.
PWR	Power
GND	Ground
NU	Not Usable (JEDEC Standard)
NC	Not Connected (JEDEC Standard)

Table 2 Abbreviations for Buffer Type

Abbreviations	Description
PU	Pull-up
OD	Open-Drain. The corresponding pin has 2 operational states, active low and tristate, and allows multiple devices to share as a wire-OR. An external pull-up is required to sustain the inactive state until another agent drives it, and must be provided by the central resource.
TS	Tristate capability: The corresponding pin has 3 operational states: Low, high and high-impedance.
PP	Push-Pull. The corresponding pin has 2 operational states: Active-low and active-high (identical to output with no type attribute).

2.3.1 Common Pins for Analog Line Module (Channels A, B)

Table 3 Common Pins for Analog Line Module (Channels A, B)

Pin No.		Pin Name	Pin Type[1)]	Buffer Type[2)]	Function
PG-TQFP-64	PG-TQFP-100				
39	61	CREF_AB	AI/O	-	Connection to external capacitor for low-pass filtering of the reference voltage
40	62	GND15_AB	GND	-	Common ground for bias block
38	60	VDD15_AB	PWR	-	1.5 V power supply for bias

1) For explanation of abbreviations see **Table 1**

2) For explanation of abbreviations see **Table 2**

2.3.2 Pins for Analog Line Module (Channels A, B)

Table 4 Pins for Analog Line Module (Channels A, B)

Pin No.		Pin Name	Pin Type[1)]	Buffer Type[2)]	Function
PG-TQFP-64	PG-TQFP-100				
29 52	47 79	RING_A RING_B	AI	-	Analog input for measurement the voltage on ring line
30 51	48 78	TIP_A TIP_B	AI	-	Analog input for measurement the voltage on tip line
37 44	57 70	ACP_A ACP_B	AO	-	Differential two-wire AC output voltage controlling the RING/TIP pins at the SLIC
36 45	56 71	ACN_A ACN_B	AO	-	Differential two-wire AC output voltage controlling the RING/TIP pins at the SLIC
28 53	46 80	DCP_A DCP_B	AO	-	Differential two-wire DC output voltage controlling the RING/TIP pins at the SLIC
27 54	45 81	DCN_A DCN_B	AO	-	Differential two-wire DC output voltage controlling the RING/TIP pins at the SLIC
25 56	43 83	VDD33_A VDD33_B	PWR	-	3.3 V analog power supply
35 46	55 72	VDD15_A VDD15_B	PWR	-	1.5 V power supply
26 55	44 82	GND33_A GND33_B	GND	-	Analog ground 3.3 V
34 47	54 73	GND15_A GND15_B	GND	-	Analog ground 1.5 V
32 49	50 76	IT_A IT_B	AI	-	Transversal current input (AC + DC)
33 48	51 75	ITAC_A ITAC_B	AI	-	Transversal current input (AC)

Table 4 Pins for Analog Line Module (Channels A, B) (cont'd)

Pin No.		Pin Name	Pin Type[1)]	Buffer Type[2)]	Function
PG-TQFP-64	PG-TQFP-100				
31 50	49 77	VCMIT_A VCMIT_B	AI/O	-	Reference pin for transversal/longitudinal current sensing
23 58	41 85	C2_A C2_B	AO	-	Ternary logic output controlling the SLIC operation mode
24 57	42 84	C1_A C1_B	AI/O	-	Ternary logic output controlling the SLIC operation mode; indicating thermal overload of a SLIC if a current of typically 150 µA is drawn out by the SLIC's C1 pin

1) For explanation of abbreviations see **Table 1**
2) For explanation of abbreviations see **Table 2**

2.3.3 General Pins

Table 5 General Pins

Pin No.		Pin Name	Pin Type[1)]	Buffer Type[2)]	Function
PG-TQFP-64	PG-TQFP-100				
59	87	RESETQ	I	-	Hardware reset for the whole chip (low active)
42	65	MCLK	I	-	Master clock for the PLL input. The MCLK clock can vary from 512 kHz to 8192 kHz in multiples of 512 kHz. This pin must be directly connected to PCL. *Note: See **Chapter 3.2** and **Chapter 5.2**, **Table 37** for wave form requirements*
–	13, 30, 31, 52, 53, 58, 59, 63, 67, 68, 69, 74, 86	D.N.C.	NC	-	Do not connect

1) For explanation of abbreviations see **Table 1**
2) For explanation of abbreviations see **Table 2**

2.3.4 General-Purpose Input/Output Pins

Table 6 General-Purpose Input/Output Pins[1)]

Pin No.		Pin Name	Pin Type[2)]	Buffer Type[3)]	Function
PG-TQFP-64	PG-TQFP-100				
–	98	GPIO0	I/O	OD, PP, PU[4)]	General-Purpose I/O 0
–	97	GPIO1	I/O	OD, PP, PU[4)]	General-Purpose I/O 1
–	96	GPIO2	I/O	OD, PP, PU[4)]	General-Purpose I/O 2
–	95	GPIO3	I/O	OD, PP, PU[4)]	General-Purpose I/O 3
–	91	GPIO4	I/O	OD, PP, PU[4)]	General-Purpose I/O 4
–	90	GPIO5	I/O	OD, PP, PU[4)]	General-Purpose I/O 5
–	89	GPIO6	I/O	OD, PP, PU[4)]	General-Purpose I/O 6
–	88	GPIO7	I/O	OD, PP, PU[4)]	General-Purpose I/O 7

1) If a GPIO pin is not used, it should be connected to ground via a 10 kΩ resistor. If guaranteed that it is never configured as an output, this pin can directly be connected to ground.
2) For explanation of abbreviations see **Table 1**
3) For explanation of abbreviations see **Table 2**
4) Buffer Type is programmable, after reset the pull-up is disabled and the pin is configured as an input

2.3.5 Test-Mode Selection/JTAG (Boundary Scan) Interface Pins

Table 7 Test-Mode Selection/JTAG (Boundary Scan) Interface Pins

Pin No.		Pin Name	Pin Type[1]	Buffer Type[2]	Function
PG-TQFP-64	PG-TQFP-100				
1	1	TDI	I	-	JTAG data input[3]
3	3	TMS	I	-	JTAG test-mode switch[4]
63	99	TCK	I	-	JTAG clock[4]
2	2	TDO	O	TS	JTAG data output[3]
64	100	TRSTQ	I	-	JTAG reset[4]

1) For explanation of abbreviations see **Table 1**
2) For explanation of abbreviations see **Table 2**
3) Pull-up resistor of 10 kΩ must be applied
4) Pull-down resistor of 10 kΩ must be applied

2.3.6 Interface-Type Selection Pins

Table 8 Interface-Type Selection Pins

Pin No.		Pin Name	Pin Type[1]	Buffer Type[2]	Function
PG-TQFP-64	PG-TQFP-100				
–	4	IFSEL0	I	PU	Interface-select pin 0
–	5	IFSEL1	I	PU	Interface-select pin 1

1) For explanation of abbreviations see **Table 1**
2) For explanation of abbreviations see **Table 2**

2.3.7 PCM Interface Pins

Table 9 PCM Interface Pins

Pin No.		Pin Name	Pin Type[1]	Buffer Type[2]	Function
PG-TQFP-64	PG-TQFP-100				
7	9	DX1	I/O	TS	PCM interface data output
8	10	DR1	I/O	TS	PCM interface data input
9	11	TC1Q	O	OD	Control pin for external driver

Table 9 PCM Interface Pins (cont'd)

Pin No.		Pin Name	Pin Type[1]	Buffer Type[2]	Function
PG-TQFP-64	PG-TQFP-100				
10	12	FSC	I	-	Frame synchronization for PCM interface and PLL input
11	14	PCL	I	-	Input for the PCM interface data clock PCLK. The PCL clock can vary from 512 kHz to 8192 kHz in multiples of 512 kHz. This pin must be directly connected to MCLK.

1) For explanation of abbreviations see Table 1
2) For explanation of abbreviations see Table 2

2.3.8 Host Interface Pins

Table 10 Host Interface Pins

Pin No.		Pin Name	Pin Type[1]	Buffer Type[2]	Signal Name			
PG-TQFP-64	PG-TQFP-100				Intel Multi-plexed Mode	Intel Demulti-plexed Mode	Motorola	SPI
–	15	AD7/SA4	I/O	TS	A7/DIO7	DIO7	DATA7	SA4
–	16	AD6/SA3	I/O	TS	A6/DIO6	DIO6	DATA6	SA3
–	17	AD5/SA2	I/O	TS	A5/DIO5	DIO5	DATA5	SA2
–	18	AD4/SA1	I/O	TS	A4/DIO4	DIO4	DATA4	SA1
–	22	AD3/SA0	I/O	TS	A3/DIO3	DIO3	DATA3	SA0
–	23	AD2	I/O	TS	A2/DIO2	DIO2	DATA2	GND
15	24	AD1/DOUT	I/O	TS	A1/DIO1	DIO1	DATA1	DOUT[3]
16	25	AD0/DIN	I/O	TS	A0/DIO0	DIO0	DATA0	DIN[4]
–	26	A5/RDQ	I	-	RDQ	RDQ	ADDR5	GND
17	27	CSQ	I	-	CSQ	CSQ	CSQ	CSQ
–	28	RDYQ	O	OD	RDYQ	RDYQ	RDYQ	D.N.C.
18	29	INTQ	O	OD	INTQ	INTQ	INTQ	INTQ
–	35	RWQ/WRQ	I	-	WRQ	WRQ	RD/WRQ	GND
22	36	A4/DCLK	I	-	GND	A4	ADDR4	DCLK
–	37	A3/ALE	I	-	ALE	A3	ADDR3	GND
–	38	A2	I	-	GND	A2	ADDR2	GND
–	39	A1	I	-	GND	A1	ADDR1	GND
–	40	A0	I	-	GND	A0	ADDR0	GND

1) For explanation of abbreviations see Table 1
2) For explanation of abbreviations see Table 2
3) As the DOUT of the VINETIC® is set to high impedance for CSQ = high level, a pull-up resistor of 10 kΩ should be applied.
4) If the driver for the DIN signal may have high impedance, a pull-up resistor of 10 kΩ should be applied.

2.3.9 Digital Power/Ground Pins

Table 11 Digital Power/Ground Pins

Pin No.		Pin Name	Pin Type[1)]	Buffer Type[2)]	Function
PG-TQFP-64	PG-TQFP-100				
4 12 19 62	6 19 32 94	VDD15	PWR	-	1.5 V power supply for the digital part
43	66	VDD15P	PWR	-	1.5 V power supply for the PLL. The PLL is most important for the overall performance of the chip. Special care should be taken with respect to the filtering of the PLL power supply.
6 14 21 60	8 21 34 92	VDD33	PWR	-	Digital 3.3 V power supply for I/O pads
5 13 20 61	7 20 33 93	GND	GND	-	Digital ground
41	64	GND15P	GND	-	PLL ground Connect the PLL ground to a high quality ground.

1) For explanation of abbreviations see **Table 1**

2) For explanation of abbreviations see **Table 2**

2.4 VINETIC®-1CPE Pins Sorted by Function

2.4.1 Pins for Analog Line Module

Table 12 Pins for Analog Line Module

Pin No.		Pin Name	Pin Type[1)]	Buffer Type[2)]	Function
PG-TQFP-64	PG-TQFP-100				
39	61	CREF_AB	AI/O	-	Connection to external capacitor for low-pass filtering of the reference voltage
40	62	GND15_AB	GND	-	Common ground for bias block
38	60	VDD15_AB	PWR	-	1.5 V power supply for bias
29	47	RING_A	AI	-	Analog input for measurement the voltage on ring line
30	48	TIP_A	AI	-	Analog input for measurement the voltage on tip line
37	57	ACP_A	AO	-	Differential two-wire AC output voltage controlling the RING/TIP pins at the SLIC
36	56	ACN_A	AO	-	Differential two-wire AC output voltage controlling the RING/TIP pins at the SLIC
28	46	DCP_A	AO	-	Differential two-wire DC output voltage controlling the RING/TIP pins at the SLIC
27	45	DCN_A	AO	-	Differential two-wire DC output voltage controlling the RING/TIP pins at the SLIC
25 56	43 83	VDD33_A VDD33_B	PWR	-	3.3 V analog power supply
35 46	55 72	VDD15_A VDD15_B	PWR	-	1.5 V power supply
26 55	44 82	GND33_A GND33_B	GND	-	Analog ground 3.3 V
34 47	54 73	GND15_A GND15_B	GND	-	Analog ground 1.5 V
32	50	IT_A	AI	-	Transversal current input (AC + DC)
33	51	ITAC_A	AI	-	Transversal current input (AC)
31	49	VCMIT_A	AI/O	-	Reference pin for transversal/longitudinal current sensing
23	41	C2_A	AO	-	Ternary logic output controlling the SLIC operation mode
24	42	C1_A	AI/O	-	Ternary logic output controlling the SLIC operation mode; indicating thermal overload of a SLIC if a current of typically 150 µA is drawn out by the SLIC's C1 pin.

1) For explanation of abbreviations see **Table 1**
2) For explanation of abbreviations see **Table 2**

2.4.2 General Pins

Table 13 General Pins

Pin No.		Pin Name	Pin Type[1]	Buffer Type[2]	Function
PG-TQFP-64	PG-TQFP-100				
59	87	RESETQ	I	-	Hardware reset for the whole chip (active low)
42	65	MCLK	I	-	Master clock for the PLL input.The MCLK clock can vary from 512 kHz to 8192 kHz in multiples of 512 kHz. This pin must be directly connected to PCL. *Note: See **Chapter 3.2** and **Chapter 5.2**, **Table 37** for wave form requirements*
48 49 50 51 52	75 76 77 78 79	ATEST1 ATEST2 ATEST3 ATEST4 ATEST5	NU	-	Analog test pins. These pins have to be connected together externally (shortcut) and are not to be conneted to any potential or GND.
44, 45, 53, 54, 57, 58	13, 30, 31, 52, 53, 58, 59, 63, 67, 68, 69, 70, 71, 74, 80, 81, 84, 85, 86	D.N.C.	NC	-	Do not connect

1) For explanation of abbreviations see **Table 1**
2) For explanation of abbreviations see **Table 2**

2.4.3 General-Purpose Input/Output Pins

Table 14 General-Purpose Input/Output Pins[1]

Pin No.		Pin Name	Pin Type[2]	Buffer Type[3]	Function
PG-TQFP-64	PG-TQFP-100				
–	98	GPIO0	I/O	OD, PP, PU[4]	General-Purpose I/O 0
–	97	GPIO1	I/O	OD, PP, PU[4]	General-Purpose I/O 1
–	96	GPIO2	I/O	OD, PP, PU[4]	General-Purpose I/O 2
–	95	GPIO3	I/O	OD, PP, PU[4]	General-Purpose I/O 3
–	91	GPIO4	I/O	OD, PP, PU[4]	General-Purpose I/O 4
–	90	GPIO5	I/O	OD, PP, PU[4]	General-Purpose I/O 5
–	89	GPIO6	I/O	OD, PP, PU[4]	General-Purpose I/O 6
–	88	GPIO7	I/O	OD, PP, PU[4]	General-Purpose I/O 7

1) If a GPIO pin is not used, it should be connected to ground via a 10 kΩ resistor. If guaranteed that it is never configured as an output, this pin can directly be connected to ground.
2) For explanation of abbreviations see **Table 1**
3) For explanation of abbreviations see **Table 2**
4) Buffer type is programmable. After reset the pull-up is disabled and the pin is configured as an input

2.4.4 Test-Mode Selection/JTAG (Boundary Scan) Interface Pins

Table 15 Test-Mode Selection/JTAG (Boundary Scan) Interface Pins

Pin No.		Pin Name	Pin Type[1)]	Buffer Type[2)]	Function
PG-TQFP-64	PG-TQFP-100				
1	1	TDI	I	-	JTAG data input[3)]
3	3	TMS	I	-	JTAG test-mode switch[4)]
63	99	TCK	I	-	JTAG clock[4)]
2	2	TDO	O	TS	JTAG data output[3)]
64	100	TRSTQ	I	-	JTAG reset[4)]

1) For explanation of abbreviations see **Table 1**
2) For explanation of abbreviations see **Table 2**
3) Pull-up resistor of 10 kΩ must be applied
4) Pull-down resistor of 10 kΩ must be applied

2.4.5 Interface-Type Selection Pins

Table 16 Interface-Type Selection Pins

Pin No.		Pin Name	Pin Type[1)]	Buffer Type[2)]	Function
PG-TQFP-64	PG-TQFP-100				
–	4	IFSEL0	I	PU	Interface-select pin 0
–	5	IFSEL1	I	PU	Interface-select pin 1

1) For explanation of abbreviations see **Table 1**
2) For explanation of abbreviations see **Table 2**

2.4.6 PCM Interface Pins

Table 17 PCM Interface Pins

Pin No.		Pin Name	Pin Type[1]	Buffer Type[2]	Function
PG-TQFP-64	PG-TQFP-100				
7	9	DX1	I/O	TS	PCM interface data output (tristate)
8	10	DR1	I/O	TS	PCM interface data input
9	11	TC1Q	O	OD	Control pin for external driver (open drain)
10	12	FSC	I	-	Frame synchronization for PCM interface and PLL input
11	14	PCL	I	-	Input for the PCM interface data clock PCLK. The PCL clock can vary from 512 kHz to 8192 kHz in multiples of 512 kHz. This pin must be directly connected to MCLK.

1) For explanation of abbreviations see Table 1

2) For explanation of abbreviations see Table 2

2.4.7 Host Interface Pins

Table 18 Host Interface Pins

Pin No.		Pin Name	Pin Type[1]	Buffer Type[2]	Signal Name			
PG-TQFP-64	PG-TQFP-100				Intel Multi-plexed Mode	Intel Demulti-plexed Mode	Motorola	SPI
–	15	AD7/SA4	I/O	TS	A7/DIO7	DIO7	DATA7	SA4
–	16	AD6/SA3	I/O	TS	A6/DIO6	DIO6	DATA6	SA3
–	17	AD5/SA2	I/O	TS	A5/DIO5	DIO5	DATA5	SA2
–	18	AD4/SA1	I/O	TS	A4/DIO4	DIO4	DATA4	SA1
–	22	AD3/SA0	I/O	TS	A3/DIO3	DIO3	DATA3	SA0
–	23	AD2	I/O	TS	A2/DIO2	DIO2	DATA2	GND
15	24	AD1/DOUT	I/O	TS	A1/DIO1	DIO1	DATA1	DOUT[3]
16	25	AD0/DIN	I/O	TS	A0/DIO0	DIO0	DATA0	DIN[4]
–	26	A5/RDQ	I	-	RDQ	RDQ	ADDR5	GND
17	27	CSQ	I	-	CSQ	CSQ	CSQ	CSQ
–	28	RDYQ	O	OD	RDYQ	RDYQ	RDYQ	D.N.C.
18	29	INTQ	O	OD	INTQ	INTQ	INTQ	INTQ
–	35	RWQ/WRQ	I	-	WRQ	WRQ	RD/WRQ	GND
22	36	A4/DCLK	I	-	GND	A4	ADDR4	DCLK
–	37	A3/ALE	I	-	ALE	A3	ADDR3	GND
–	38	A2	I	-	GND	A2	ADDR2	GND

Table 18 Host Interface Pins (cont'd)

Pin No.		Pin Name	Pin Type[1]	Buffer Type[2]	Signal Name			
PG-TQFP-64	PG-TQFP-100				Intel Multi-plexed Mode	Intel Demulti-plexed Mode	Motorola	SPI
–	39	A1	I	-	GND	A1	ADDR1	GND
–	40	A0	I	-	GND	A0	ADDR0	GND

1) For explanation of abbreviations see Table 1
2) For explanation of abbreviations see Table 2
3) As the DOUT of the VINETIC® is set to high impedance for CSQ = high level, a pull-up resistor of 10 kΩ should be applied.
4) If the driver for the DIN signal may have high impedance, a pull-up resistor of 10 kΩ should be applied.

2.4.8 Digital Power/Ground Pins

Table 19 Digital Power/Ground Pins

Pin No.		Pin Name	Pin Type[1]	Buffer Type[2]	Function
PG-TQFP-64	PG-TQFP-100				
4 12 19 62	6 19 32 94	VDD15	PWR	-	1.5 V power supply for the digital part
43	66	VDD15P	PWR	-	1.5 V power supply for the PLL. The PLL is most important for the overall performance of the chip. Special care should be taken with respect to the filtering of the PLL supply.
6 14 21 60	8 21 34 92	VDD33	PWR	-	Digital 3.3 V power supply for I/O pads
5 13 20 61	7 20 33 93	GND	GND	-	Digital ground
41	64	GND15P	GND	-	PLL ground Connect the PLL ground to a high quality ground.

1) For explanation of abbreviations see Table 1
2) For explanation of abbreviations see Table 2

3 Hardware Behavior and Handling

3.1 Block Diagram VINETIC®-2CPE/-1CPE

Figure 9 is the block diagram of the VINETIC®-2CPE/-1CPE.

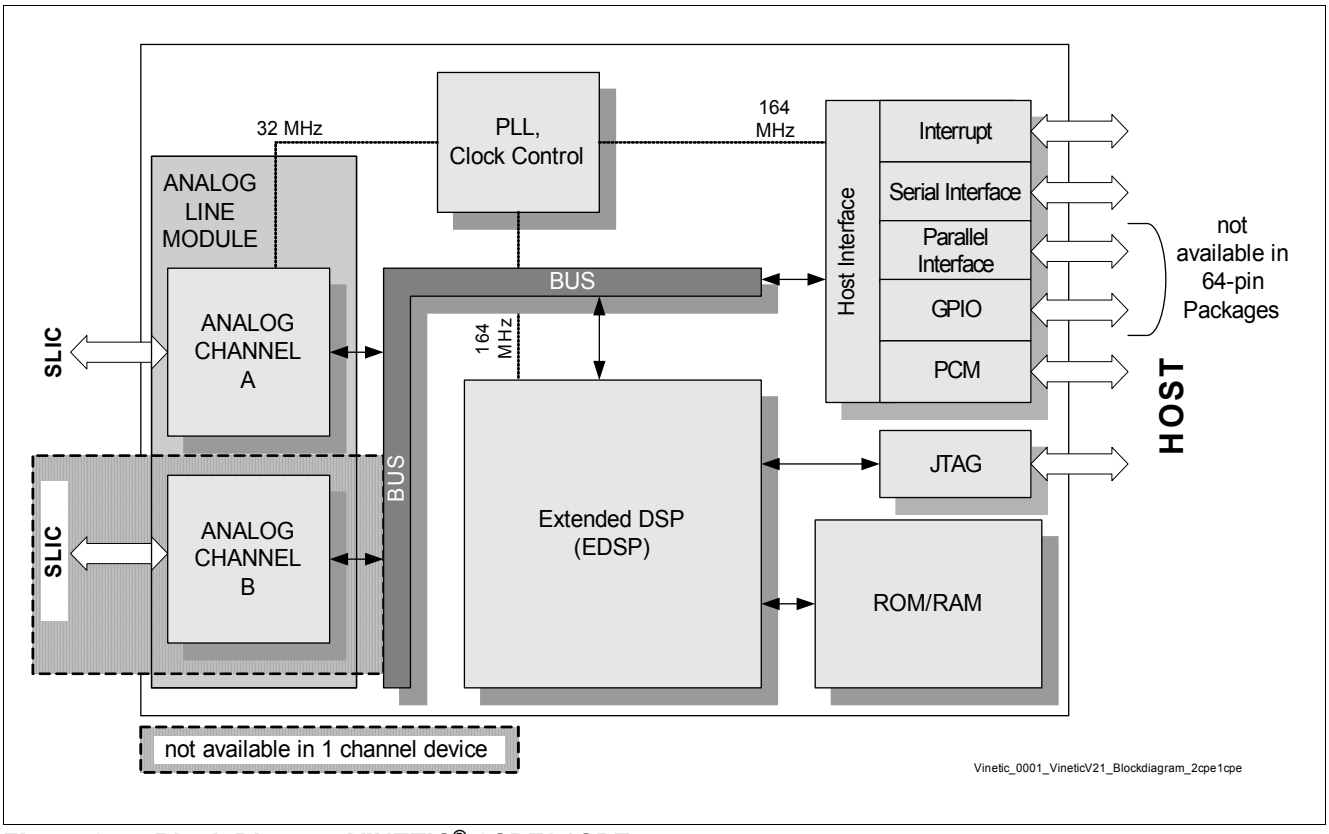

Figure 9 Block Diagram VINETIC®-2CPE/-1CPE

3.2 Clocking

The VINETIC®-2CPE/-1CPE needs the following clocks: master clock (MCLK), frame synchronization clock (FSC), and PCM interface clock (PCL).

MCLK has to fulfill the specification given in **Table 21** and **Figure 10** and has to be phase-locked to FSC. The FSC has to fulfill the specification described in **Chapter 4.3**.

PCL must be directly connected to MCLK and has to fulfill the specification of **Table 31**.

All clocks have to be provided regardless of the application. Even though the PCM interface might not be used, the clocks on MCLK, PCL and FSC have to be provided at all times to ensure correct operation of the device.

Clock failure bits (see **Figure 11**) of the VINETIC®-2CPE/-1CPE are able to indicate a clock synchronization problem. The bit SYNC-FAIL detects a clock divider synchronization failure and the bit MCLK-FAIL reports a PLL synchronization failure. In case of unlock of the PLL, all clocks are internally shut down and the chip operation is stopped. The current Analog Line Module (ALM) mode will be frozen.

The MCLK pin has no input hysteresis and therefore the MCLK input signal has to increase strictly monotonically between the maximum Low-level input voltage of 0.45 V and the minimum High-level input voltage of 1.1 V. Furthermore the MCLK input signal has to decrease strictly monotonically between the minimum High-level input voltage of 1.1 V and the maximum Low-level input voltage of 0.45 V. For digital input levels see **Chapter 5.2**, **Table 37**.

Table 20 Clocks

Pin	Description	Frequency
MCLK	Master clock (mandatory), only multiples of 512 kHz are allowed. Has to be phase-locked to FSC. For timing requirements of the MCLK signal, refer to **Table 21**.	64*f_{FSC} to 1024*f_{FSC} in steps of 64*f_{FSC}
FSC	Frame synchronization clock (mandatory), Synchronizes internal clocks and voice interface.	f_{FSC} = 8 kHz
PCL (PCM)	Clock for voice (PCM) interface (mandatory), only multiples of 512 kHz are allowed. The PCL pin must be directly connected to the MCLK pin.	64*f_{FSC} to 1024*f_{FSC} in steps of 64*f_{FSC} depending on the number of time slots (see **Table 31**).
TCK	Clock for boundary scan controller (optional)	1 MHz to 10 MHz

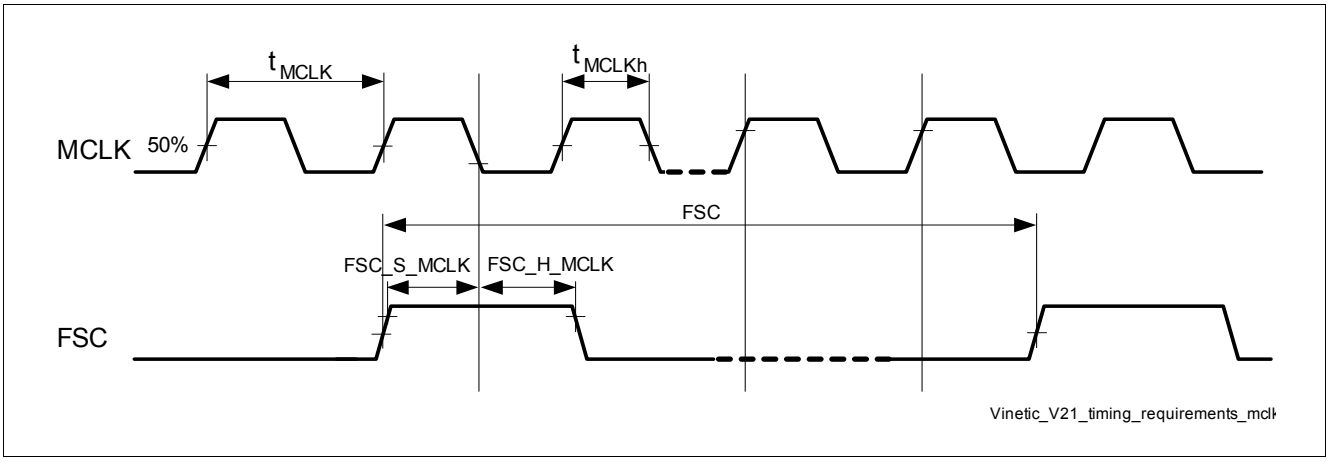

Figure 10 Timing Requirements MCLK

Table 21 Timing Requirements MCLK

Parameter	Symbol	Values			Note /Test Condition
		Min.	Typ.	Max.	
Period MCLK[1)]	t_{PCL}	1/8192	–	1/512	ms
Frequency tolerance		-100	–	100	ppm
MCLK high time	t_{PCLh}	0.4 x t_{MCLK}	–	0.6 x t_{MCLK}	µs
Period FSC[1)]	t_{FSC}	–	125	–	µs
FSC setup time	$t_{FSC\_S\_MCLK}$	10	–	–	ns
FSC hold time	$t_{FSC\_H\_MCLK}$	40	–	$t_{FSC} - t_{MCLK} - t_{FSC\_S\_MCLK}$[2)]	ns
MCLK jitter phase noise density 1 kHz frequency offset		–	–	-80	dBc[3)]/Hz
MCLK long term jitter		–	–	0.5	ns_{rms}

1) The MCLK frequency must be an integer multiple of the FSC frequency (n*64*f_{FSC}, n = 1..16).
2) This is to ensure that the FSC can be sampled low at least for one t_{MCLK} within t_{FSC}.
3) dBc = dB carrier.

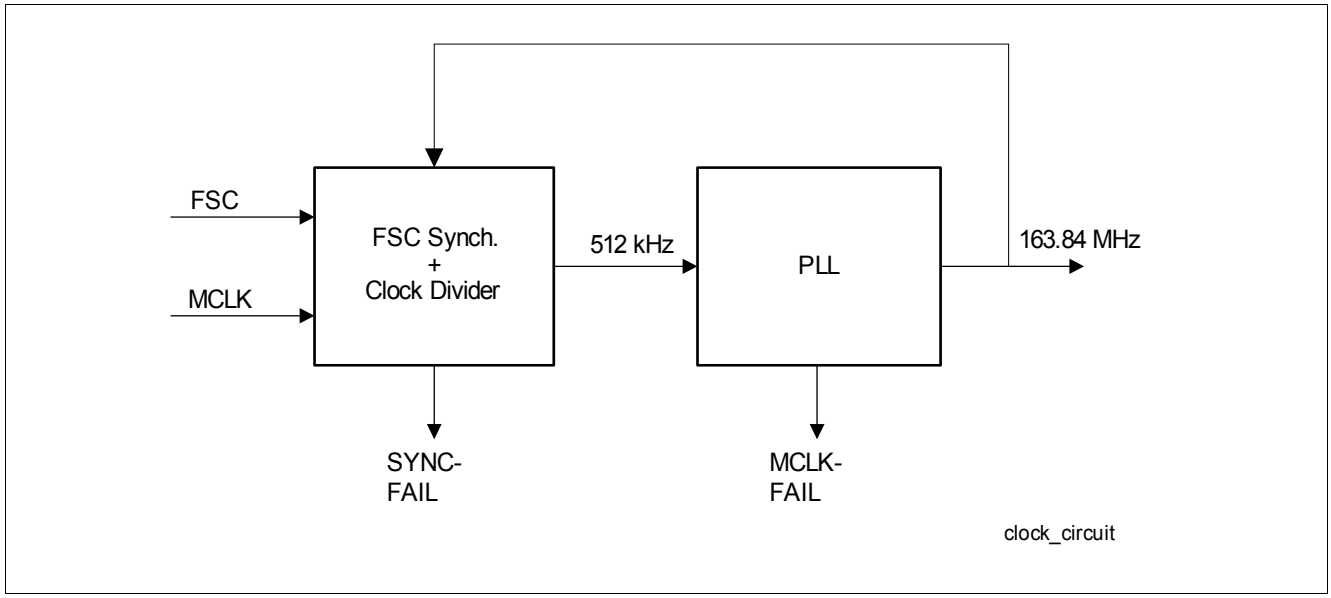

Figure 11 Clock Fail Indication

3.3 Reset

It is mandatory to apply a hardware reset after the power-up sequence.

A hardware reset of the VINETIC®-2CPE/-1CPE requires setting the signal at the RESETQ input pin to low level for at least 20 µs ($t_{res} \geq 20$ µs). RESETQ has a spike rejection function that will safely suppress spikes with a duration of less than 2 µs ($t_{rej} \leq 2$ µs).

By pulling the RESETQ input pin to low, the chip will be reset (see **Figure 12**) and the following actions will be performed:

- All I/O pins are deactivated (tristate high impedance)
- All outputs are inactive (e.g. DX1)
- The internal PLL is stopped
- VCMIT is floating
- The ternary pins C1_x[1)] and C2_x[1)], controlling the SLIC operation mode, are actively driven to 0 V.
- Internal clocks are deactivated
- The chip is in a Reset State

With the rising edge of the reset signal all external clocks need to be stable already, then the following actions are performed:

- Clock detection
- PLL synchronization
- Activation of reset routine: the internal reset routine requires approximately 16 frames (16 × 125 µs = 2 ms) to be finished (including PLL start-up and clock synchronization).
- No interrupt will be generated at the end of the reset routine.
- After the reset routine has finished, the ALM will be in PDH (Power Down High Impedance) mode and first access to the VINETIC®-2CPE/-1CPE is possible.

1) x = A, B

Figure 12 shows the reset sequence for the hardware reset caused by a signal at RESETQ pin.

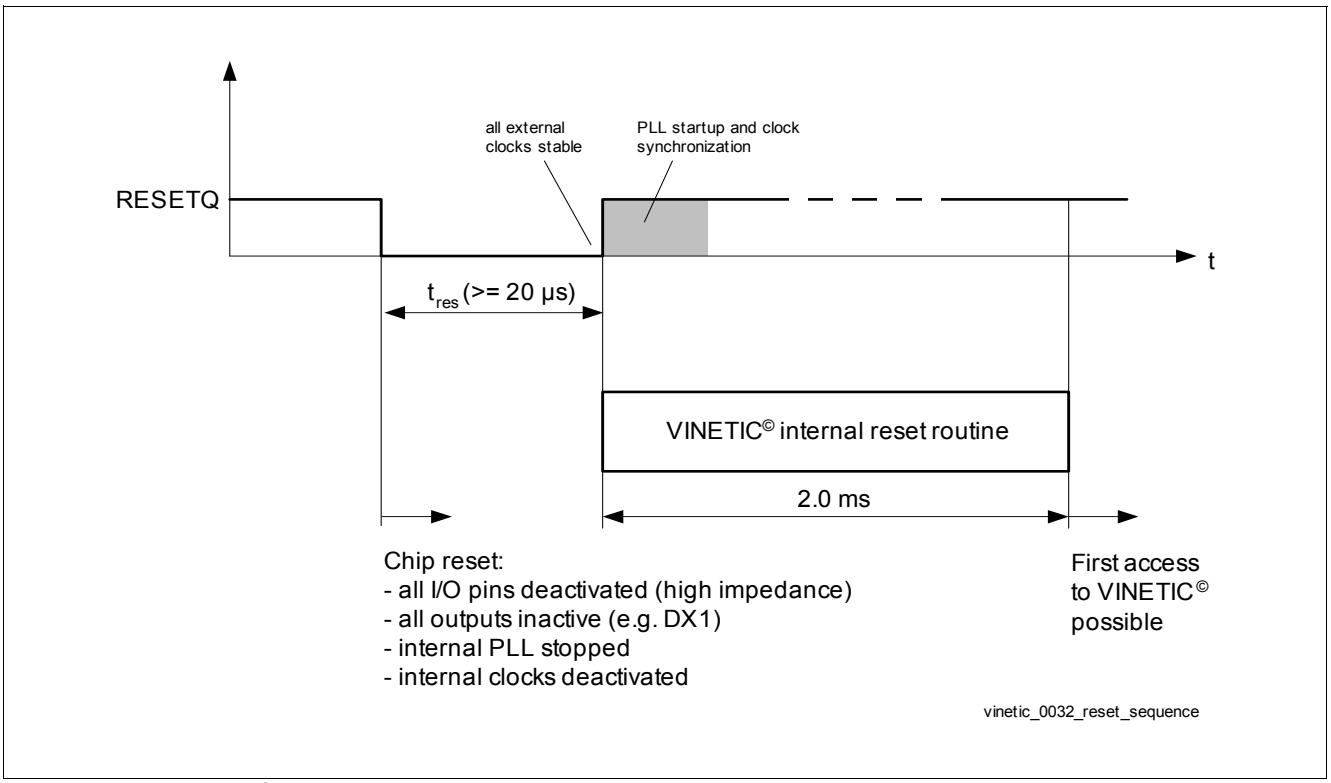

Figure 12 VINETIC® Reset Sequence

3.4 Test Modes of the VINETIC®-2CPE/-1CPE

3.4.1 Boundary Scan Test

The Boundary Scan Test (BST) is a standardized method for testing boards, also providing a standard interface to communicate with test circuits on an IC such as the VINETIC®-2CPE/-1CPE. The boundary scan standard specifies a four-wire interface using the four signals TDI, TDO, TCK and TMS. Additionally, an optional test reset signal TRSTQ is available.

These four (or five) dedicated signals on the test access port (TAP), are connected to the TAP controller inside the VINETIC®-2CPE/-1CPE. The TAP controller is a state machine clocked with the rising edge of TCK and the state transitions are controlled by TMS. The VINETIC®-2CPE/-1CPE supports fully IEEE 1149.1 compliant boundary scans that creates Boundary Scan Description Language (BSDL) files.

Boundary Scan Description Language (BSDL) is a standard way to describe the features and behavior of an IC such as the VINETIC®-2CPE/-1CPE that is capable of IEEE 1149.1-compliant boundary scans. It is also a standard way to pass information to test-generation software.

4 Interface Description

For programming the VINETIC® and performing data transfer from/to the VINETIC®, a parallel interface or a serial microcontroller interface can be used. Additionally, the VINETIC® has an interface for PCM data.

VINETIC® 8-bit Parallel Interfaces

- The parallel interface can be operated in Intel 8-bit mode (multiplexed/demultiplexed) or in Motorola 8-bit mode.

VINETIC® Serial Interfaces

- The VINETIC® serial microcontroller interface (µC interface = SCI) is compatible with the Motorola SPI and the Infineon SCI.

VINETIC® PCM Interface

- The VINETIC® PCM interface has two PCM highways that are internally cross-connected, and can be operated together with the serial µC interface or the parallel interface.

The VINETIC®-2CPE/-1CPE supports the most widely used microcontrollers: e.g. MPC850, MPC860, MPC8260, C165UTAH, ADM5120, Amazon, etc. All parallel and serial interfaces (host interfaces) use the same (multiplexed) pins. The desired interface type is selected by means of pin-strapping with pins IFSEL0 and IFSEL1[1)] for the PG-TQFP-100. With PG-TQFP-64, only the serial interface is available.

Note: Host interface and PCM interface can be used in parallel.

Table 22 shows the possible interface configurations:

Table 22 Interface Configurations

No.	Interface Type	IFSEL1	IFSEL0
1.	8-bit Intel Multiplexed	0	0
2.	8-bit Intel Demultiplexed	0	1
3.	8-bit Motorola	1	0
4.	SCI	1	1

Note: MCLK, PCL and FSC always have to be supplied even if no PCM interface is used.

1) The information on IFSEL0 and IFSEL1 must be stable and constant during the whole operation time of the device.

Input/Output Waveform for AC Interface Timing Characteristics

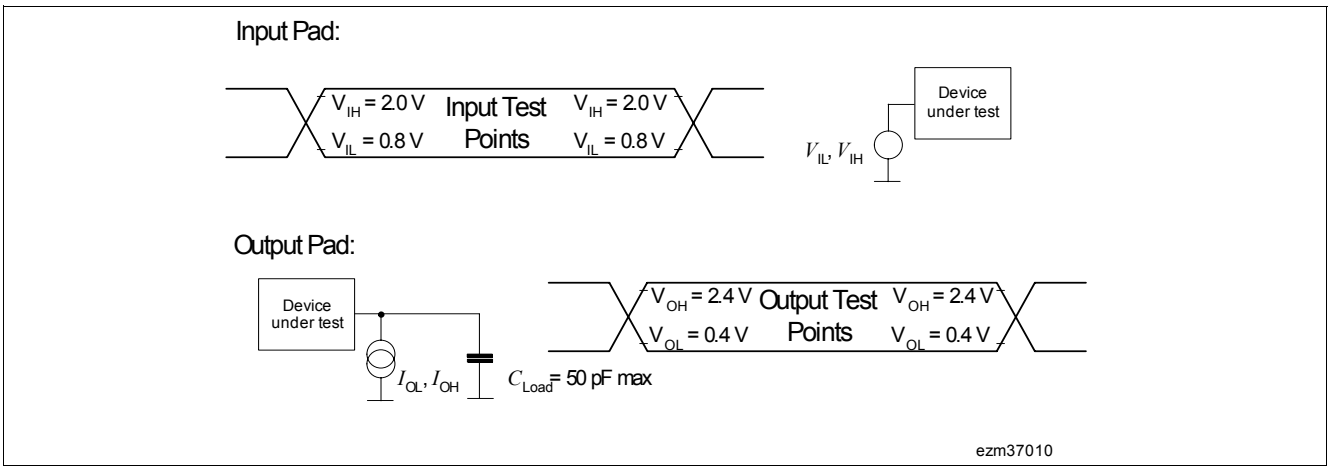

Figure 13 Waveform for AC Tests

As shown in **Table 13**, during AC-testing, the CMOS inputs are driven at a low level of 0.8 V and a high level of 2.0 V. The CMOS outputs are measured at 0.4 V and 2.4 V respectively.

4.1 Intel/Motorola-Mode Parallel Interfaces

4.1.1 Control for Intel/Motorola-Interfaces

The VINETIC®-2CPE/-1CPE uses five (Intel Demultiplexed Mode), six (Motorola Mode) or eight (Intel Multiplexed Mode) address bits. In the demultiplexed mode, the address information is taken from the pins A0 ... A4 (Intel Demultiplexed Mode) or from the pins A0 ... A5 (Motorola Mode). In the multiplexed mode, the address information is taken from the pins AD0 ... AD7 (Intel Multiplexed Mode).

4.1.2 Pin Description, Intel Interface

Table 23 Intel Demultiplexed Mode Interface Pins

Signal Name	Pin Name	Pin Type[1)]	Buffer Type[2)]	Function
CSQ	CSQ	I	-	Chip select input, start of data transfer with WRQ/RDQ (active low)
WRQ	RWQ/WRQ	I	-	Data-strobe input write (active low)
RDQ	A5/RDQ	I	-	Data-strobe input read (active low)
RDYQ	RDYQ	O	OD	Ready line (active low)
A[4:0]	A4..0	I	-	Address lines
DIO[7:0]	AD7..0	I/O	TS	Data bus

1) For explanation of abbreviations, see **Table 1**

2) For explanation of abbreviations see **Table 2**

Table 24 Intel Multiplexed Mode Interface Pins

Signal Name	Pin Name	Pin Type[1)]	Buffer Type[2)]	Function
ALE	A3/ALE	I	-	Address latch enable
CSQ	CSQ	I	-	Chip select input, start of data transfer with WRQ/RDQ (active low)
WRQ	RWQ/WRQ	I	-	Data-strobe input write (active low)
RDQ	A5/RDQ	I	-	Data-strobe input read (active low)
RDYQ	RDYQ	O	OD	Ready line (active low)
A[7:0], DIO[7:0]	AD7..0	I/O	TS	Address or Data bus

1) For explanation of abbreviations, see **Table 1**

2) For explanation of abbreviations see **Table 2**

4.1.3 Timing, Intel Demultiplexed Mode

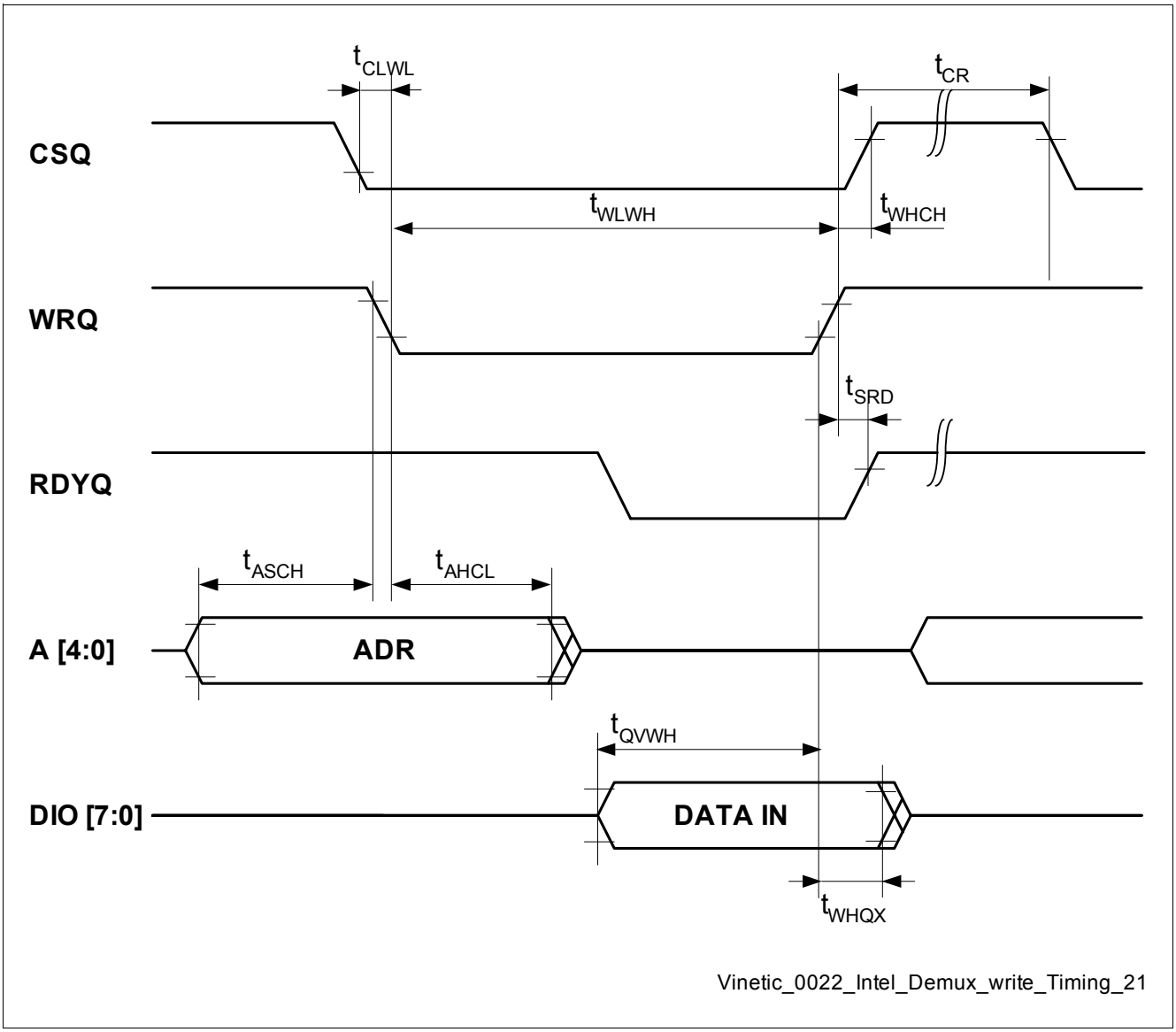

Figure 14 Write Access, Intel Demultiplexed Mode

Intel Demultiplexed: little-endian[1)].

1) Low-order byte is stored at the lower address and high-order byte is stored at the higher address.

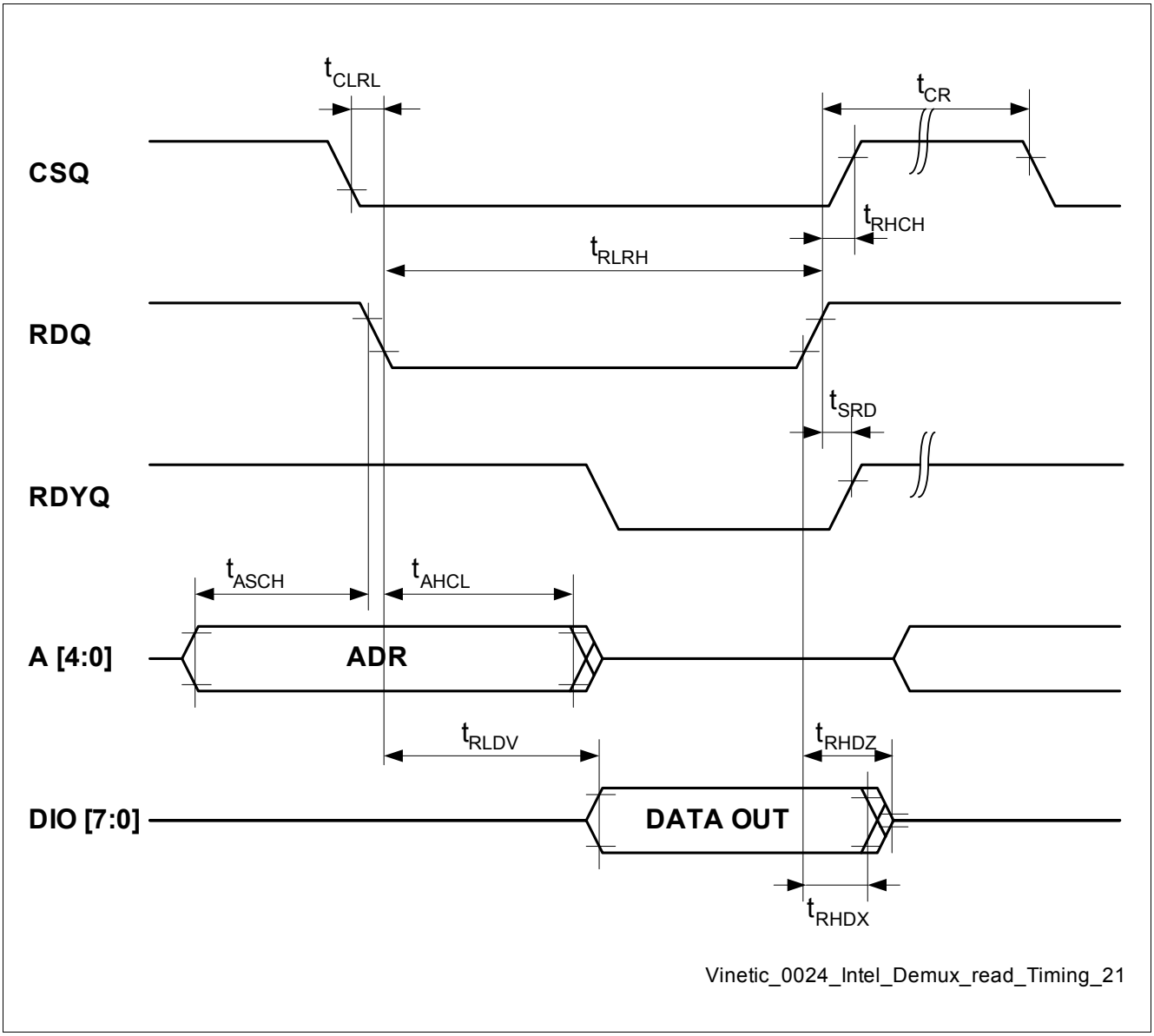

Figure 15 Read Access, Intel Demultiplexed Mode

Note: In the Intel Demultiplexed Mode the chip internal address latch signal is derived from an or-connection of the signals CSQ and WRQ for a write access and of the signals CSQ and RDQ for a read access respectively.

4.1.4 Timing, Intel Multiplexed Mode

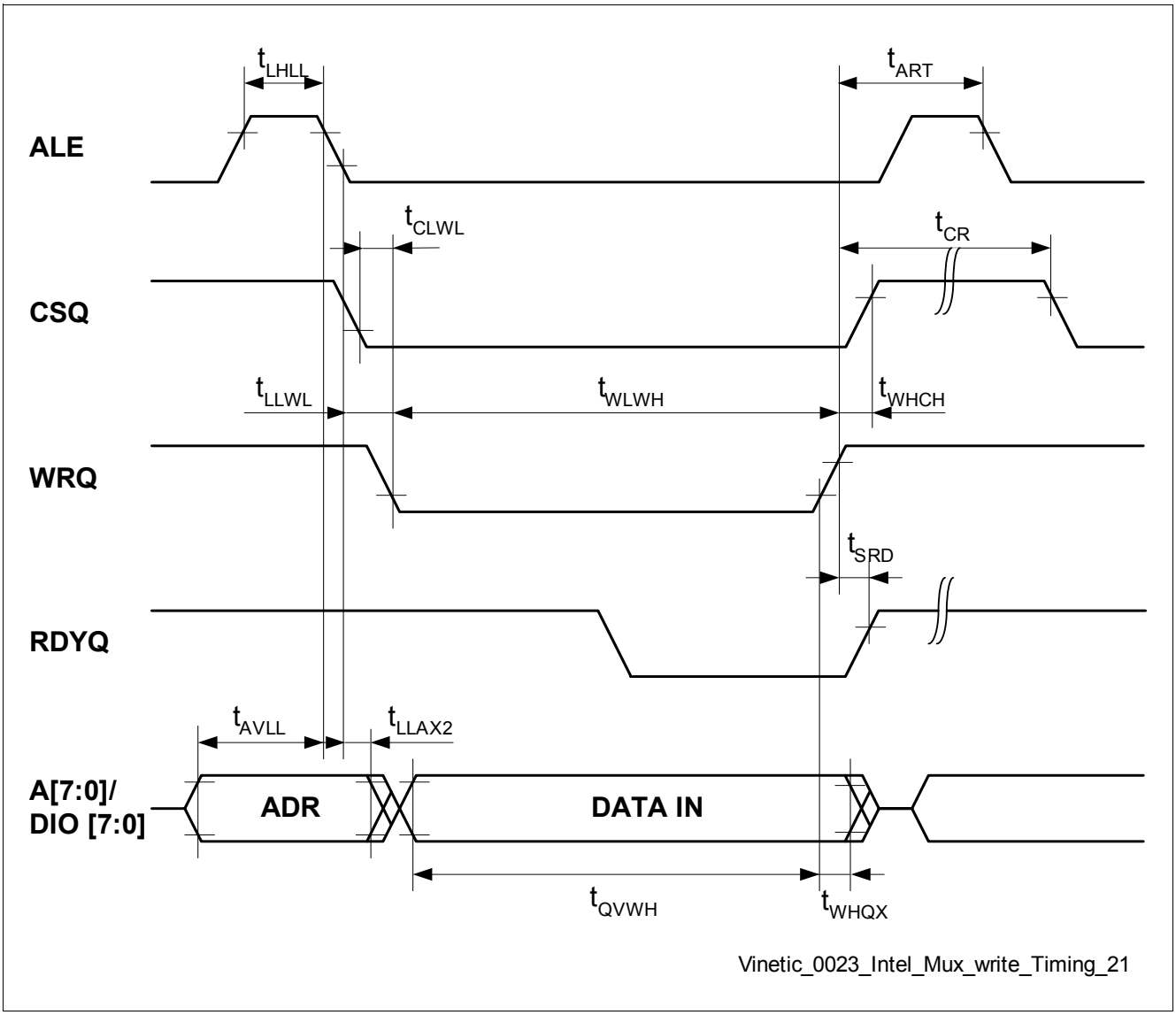

Figure 16 Write Access, Intel Multiplexed Mode

Intel Multiplexed: little-endian[1)].

1) Low-order byte is stored at the lower address and high-order byte is stored at the higher address.

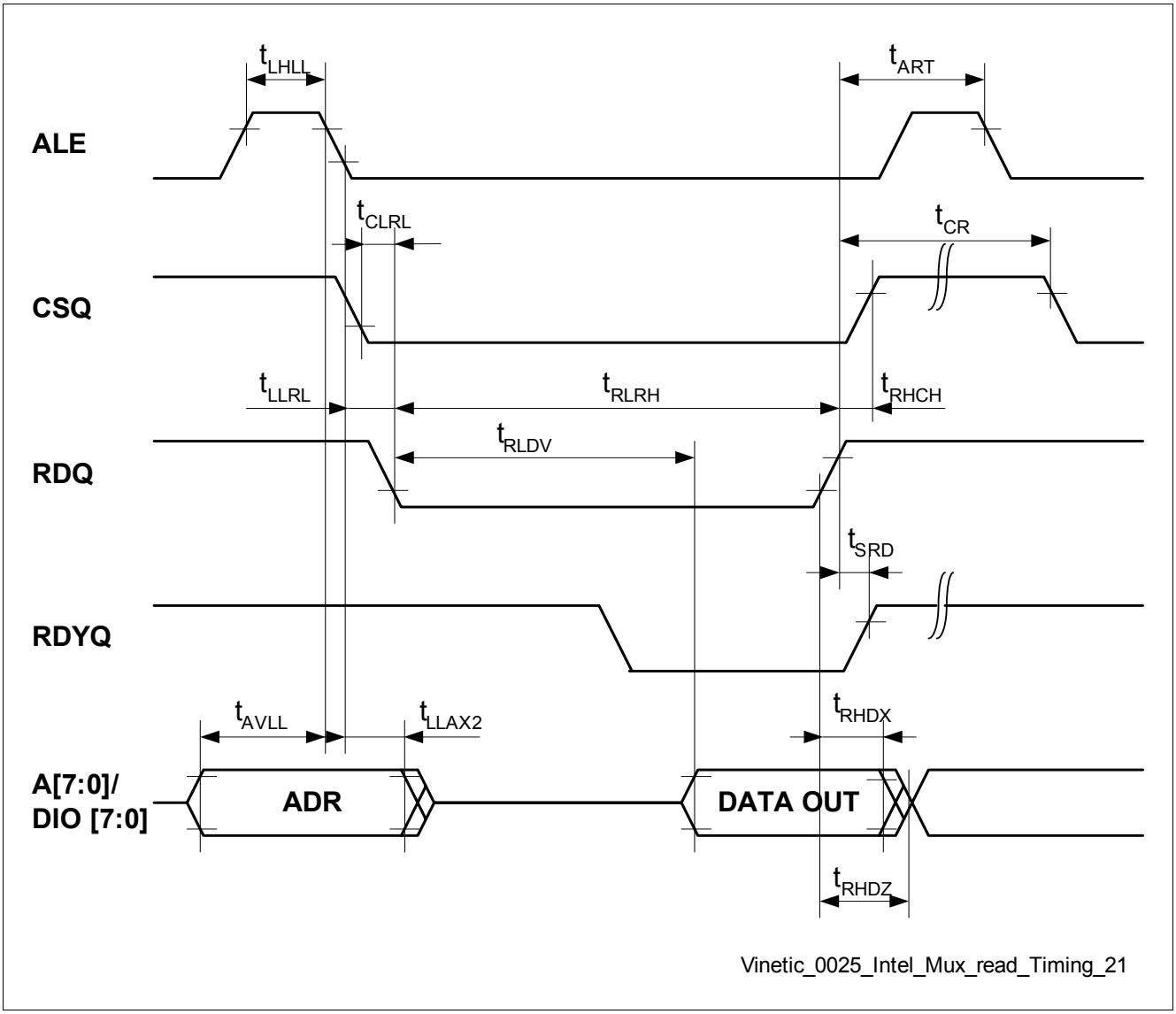

Figure 17 Read Access, Intel Multiplexed Mode

Table 25 Timing Specification, Intel Multiplexed/Demultiplexed Mode

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
ALE high time	t_{LHLL}	20	–	–	ns	–
Address setup to ALE	t_{AVLL}	10	–	–	ns	–
Address hold after ALE inactive	t_{LLAX2}	10	–	–	ns	–
Address recovery time	t_{ART}	50	–	–	ns	–
Address setup to CSQ	t_{ASCH}	10	–	–	ns	–
Address hold after CSQ	t_{AHCL}	10	–	–	ns	–
RDQ active to valid data out	t_{RLDV}	–	–	50	ns	–
Data hold after RDQ inactive	t_{RHDX}	0	–	–	ns	–
Data float after RDQ inactive	t_{RHDZ}	–	–	10	ns	–
Data setup before WRQ inactive	t_{QVWH}	20	–	–	ns	–

Table 25 Timing Specification, Intel Multiplexed/Demultiplexed Mode (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Data hold after WRQ inactive	t_{WHQX}	2.5	–	–	ns	–
RDQ active after ALE inactive	t_{LLRL}	20	–	–	ns	–
WRQ active after ALE inactive	t_{LLWL}	0	–	–	ns	–
RDQ pulse width	t_{RLRH}	70	–	–	ns	–
WRQ pulse width	t_{WLWH}	60	–	–	ns	–
CSQ low to WRQ low[1)]	t_{CLWL}	0	–	–	ns	–
WRQ high to CSQ high[1)]	t_{WHCH}	0	–	–	ns	–
CSQ low to RDQ low[1)]	t_{CLRL}	0	–	–	ns	–
RDQ high to CSQ high[1)]	t_{RHCH}	0	–	–	ns	–
Strobe signal to RDYQ delay time	t_{SRD}	–	–	10	ns	–
Command recovery time	t_{CR}	20	–	–	ns	–

1) These parameters are for reference only; they can also be negative. The control inputs RDQ and WRQ are OR-gated internally with CSQ. If the active CSQ is shorter (embedded), the active RDQ or WRQ always refer to the resulting OR-gated signal.

4.1.5 Pin Description, Motorola Interface

Table 26 Motorola Interface Pins

Signal Name	Pin Name	Pin Type[1)]	Buffer Type[2)]	Function
ADDR[5:0]	A5/RDQ, A4/DCLK, A3/ALE, A2, A1, A0	I	-	Address lines
DATA[7:0]	AD7..0	I/O	TS	Data bus
CSQ	CSQ	I	-	Chip select, data strobe with RD/WRQ (active low)
RD/WRQ	RWQ/WRQ	I	-	Read/write, data-strobe signal. (read → active high, write → active low)
RDYQ	RDYQ	O	OD	Ready line (active low)

1) For explanation of abbreviations, see **Table 1**
2) For explanation of abbreviations see **Table 2**

Motorola: big-endian[1)].

1) High-order byte is stored at the lower address and the low-order byte at the higher address.

4.1.6 Timing, Motorola Interface

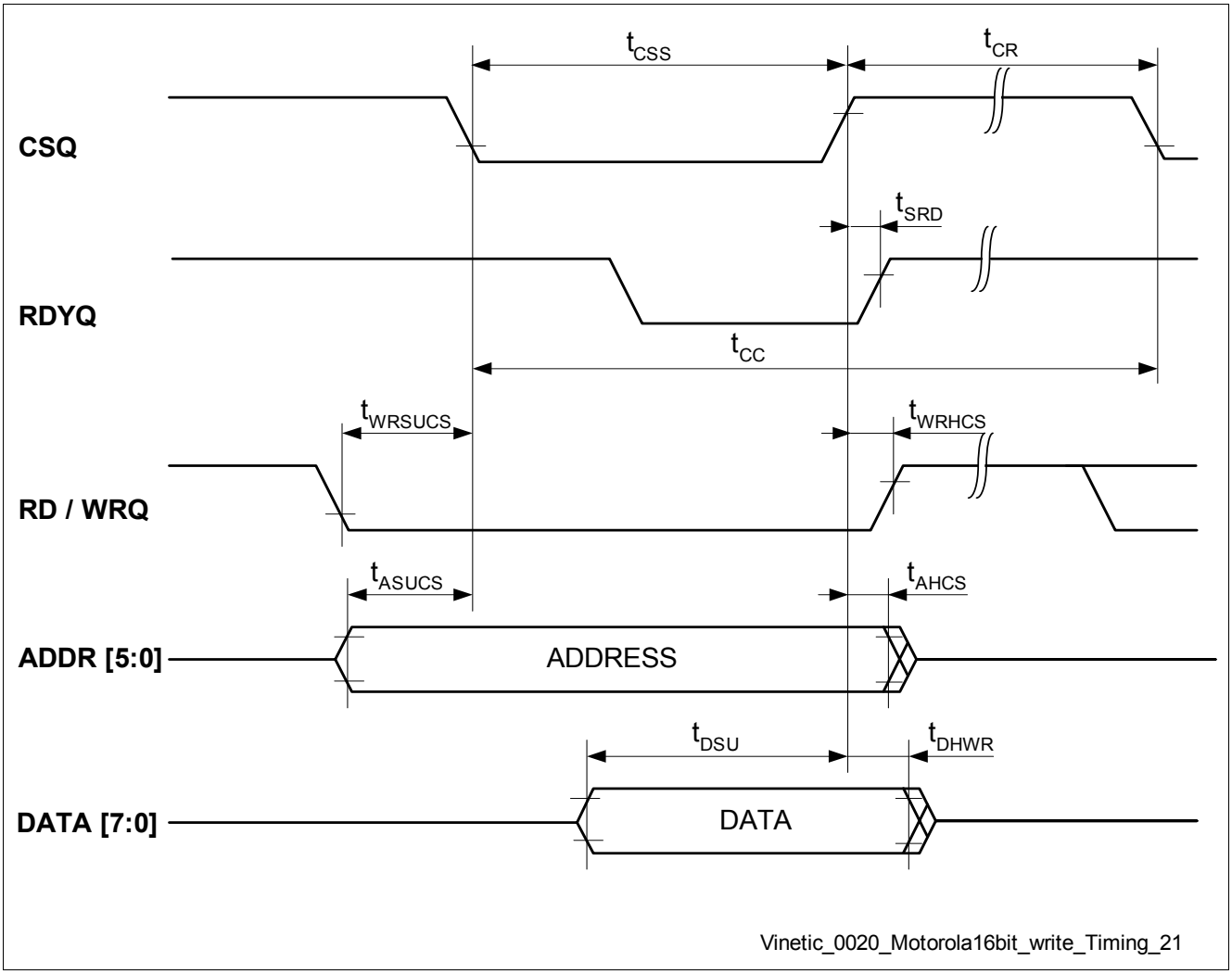

Figure 18 Write Access, Motorola Mode

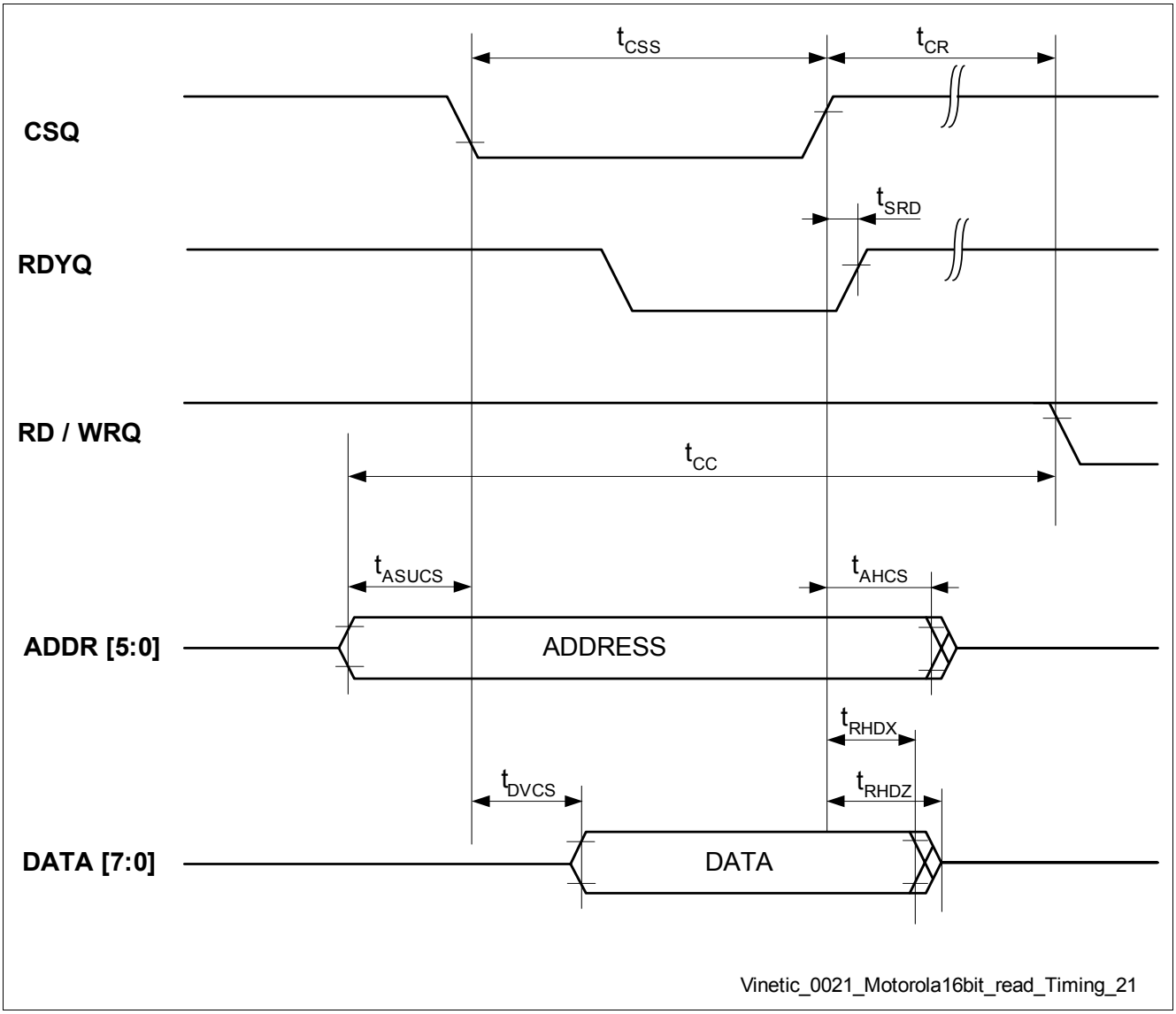

Figure 19 Read Access, Motorola Mode

Table 27 Timing Specifications for the Motorola Mode

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
CSQ strobe-pulse width	t_{CSS}	70[1)]	–	–	ns	–
Address setup time to CSQ	t_{ASUCS}	5	–	–	ns	–
Write setup time to CSQ	t_{WRSUCS}	5	–	–	ns	–
Write hold time to CSQ	t_{WRHCS}	5	–	–	ns	–
Data setup time to CSQ strobe	t_{DSU}	10	–	–	ns	–
Data hold time after write access	t_{DHWR}	2.5	–	–	ns	–
Strobe signal to RDYQ delay time	t_{SRD}	–	–	10	ns	–
Command recovery time	t_{CR}	20	–	–	ns	–
Command cycle time	t_{CC}	90	–	–	ns	–
Data valid after CSQ	t_{DVCS}	–	–	50	ns	–

Table 27 Timing Specifications for the Motorola Mode (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Data hold after read access	t_{RHDX}	0	–	–	ns	–
Data float after read access	t_{RHDZ}	–	–	10	ns	–
Address hold time to CSQ	t_{AHCS}	10	–	–	ns	–

1) If RDYQ is used, these values may be lower.

4.1.7 Reset of Interrupt Status Registers in Case of 8-Bit Interfaces

All interrupt status bits are cleared by reading respectively writing the associated interrupt register. If any 8-bit interface is used, the interrupt status register is cleared when the first byte of the register is read by the host controller. **Figure 20** shows that the INTQ line is released after reading the first byte of the interrupt status register. This means that the INTQ line is deasserted before the read command is finished.

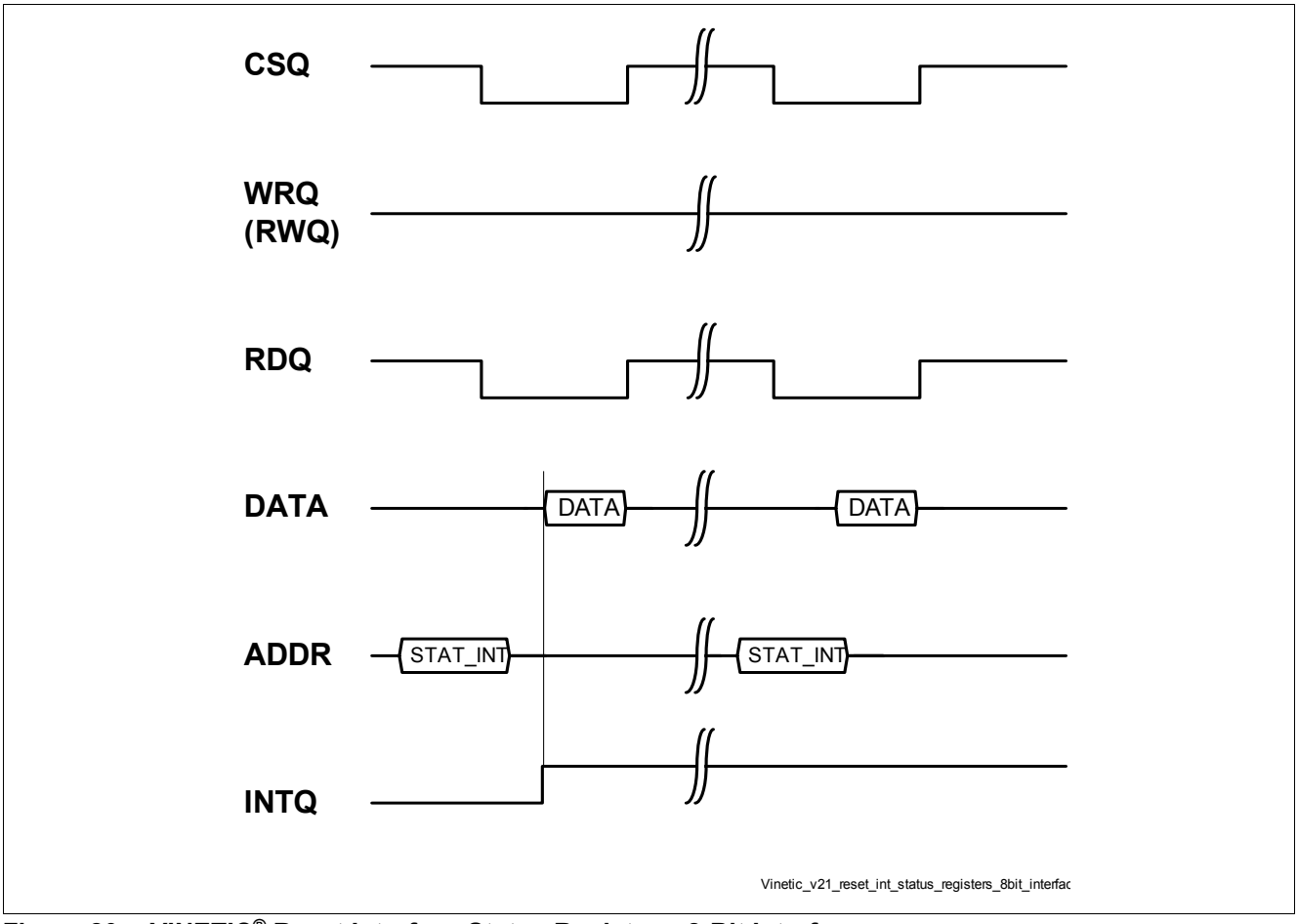

Figure 20 VINETIC® Reset Interface Status Registers, 8-Bit Interface

4.2 SCI/SPI Interface

The SCI interface of the VINETIC®-2CPE/-1CPE represents one mode of the SPI interface of the Motorola PowerQUICC® family (SPI slave mode). The data are serialized with the MSB first.

Note: The VINETIC®-2CPE/-1CPE always works as a slave.

4.2.1 Pin Description, SCI/SPI Interface

Table 28 SCI/SPI Interface Pins

Signal Name	Pin Name	Pin Type[1)]	Buffer Type[2)]	Function
CSQ	CSQ	I	-	Chip select signal starting a read or write access to VINETIC®-2CPE/-1CPE
DCLK	A4/DCLK	I	-	Data Clock supplied to VINETIC®-2CPE/-1CPE
DIN	AD0/DIN	I	-	Data input carries data from the master device to the VINETIC®-2CPE/-1CPE
DOUT	AD1/DOUT	O	TS	Data output carries data from VINETIC®-2CPE/-1CPE to a master device
SA[4:0]	SA4...SA0	I		SCI Slave address

1) For explanation of abbreviations, see **Table 1**
2) For explanation of abbreviations see **Table 2**

4.2.2 Timing, SCI/SPI Interface

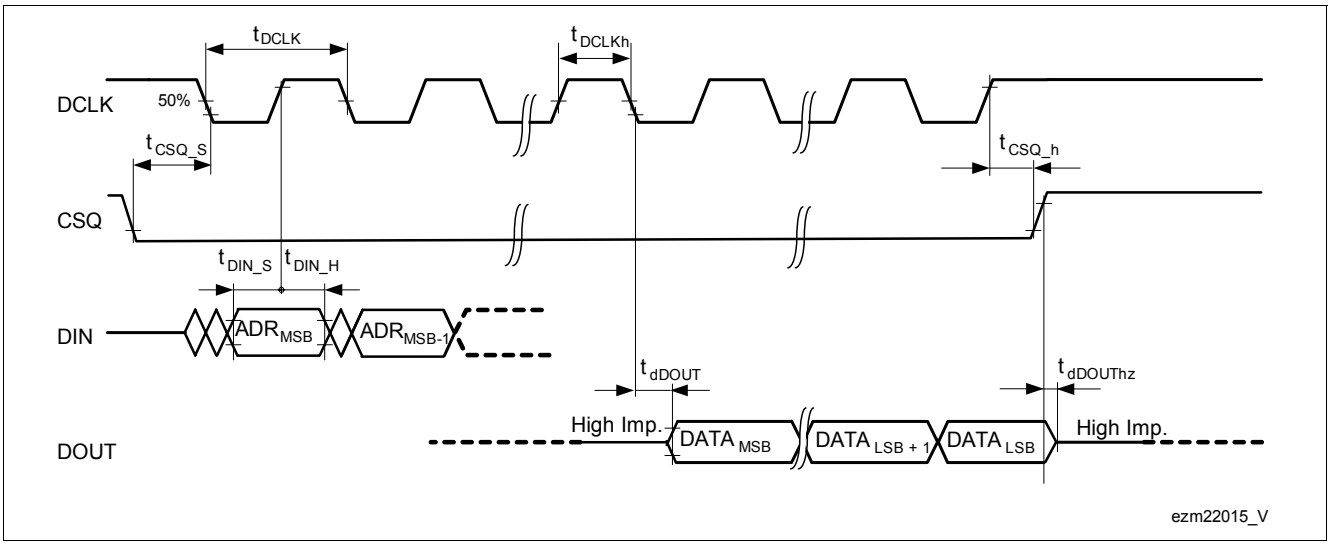

Figure 21 SCI/SPI Interface Timing

Note: In case of SCI/SPI, the RDYQ line has no function. The data clock DCLK must only be applied during the data transfer

Table 29 Timing Values, SCI/SPI Interface

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Period DCLK	t_{DCLK}	1/8192	–	–	ms	–
DCLK high time	t_{DCLKh}	0.4 x t_{DCLK}	0.5 x t_{DCLK}	0.6 x t_{DCLK}	µs	–
CSQ setup time	t_{CSQ_s}	10	–	–	ns	–
CSQ hold time	t_{CSQ_h}	30	–	–	ns	–
DIN setup time	t_{DIN_s}	10	–	–	ns	–

Table 29 Timing Values, SCI/SPI Interface (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
DIN hold time	t_{DIN_h}	10	–	–	ns	–
DOUT delay time[1)]	t_{dDOUT}	40	–	t_{dDOUT_min} + 0.4[ns/pF] x C_{Load}[pF])	ns	–
DOUT delay time to high Z	$t_{dDOUThz}$	–	–	10	ns	–

1) All delay times are made up by two components: an intrinsic time (min.-time) caused by internal processing, and a second component caused by external circuitry (C_{Load})

4.3 PCM Interface

The serial PCM interface is used to transfer A-Law or µ-Law or ADPCM-compressed voice data. The PCM interface can also transfer linear data. In this case, two successive time slots are used. The five signals of the PCM interface are used as follows (internally two cross-connected PCM highways available):

4.3.1 Pin Description, PCM Interface

Table 30 PCM Interface Pins

Signal Name	Pin Name	Pin Type[1)]	Buffer Type[2)]	Function
PCLK	PCL	I	–	PCM interface data clock
FSC	FSC	I	–	Frame synchronization for PCM interface and PLL input
DX1	DX1[3)]	I/O	TS	PCM interface data output
DR1	DR1[3)]	I/O	TS	Data input for highway one of PCM interface
TC1Q	TC1Q	O	OD	Control pin for external driver

1) For explanation of abbreviations, see **Table 1**

2) For explanation of abbreviations see **Table 2**

3) The two PCM highways are internally cross connected to enable internal conferencing between channel A and channel B. For details refer to **[2]**.

The FSC pulse identifies the beginning of a receive and transmit frame for both highways (see **Figure 22**). The PCLK clock signal synchronizes the data transfer on the DX1 and DR1 lines. In each active time slot, bytes are serialized with the MSB first. As a default setting, the rising edge indicates the start of the bit, while the falling edge is used to latch the contents of the received data on DR1. If double-clock rate is selected (PCLK clock rate is twice the data rate), the first rising edge indicates the start of a bit, while, by default, the second falling edge is used to latch the contents of the data line DR1.

The VINETIC®-2CPE/-1CPE allows for flexible programming of the PCM interface (see **[3]**, **[4]**).

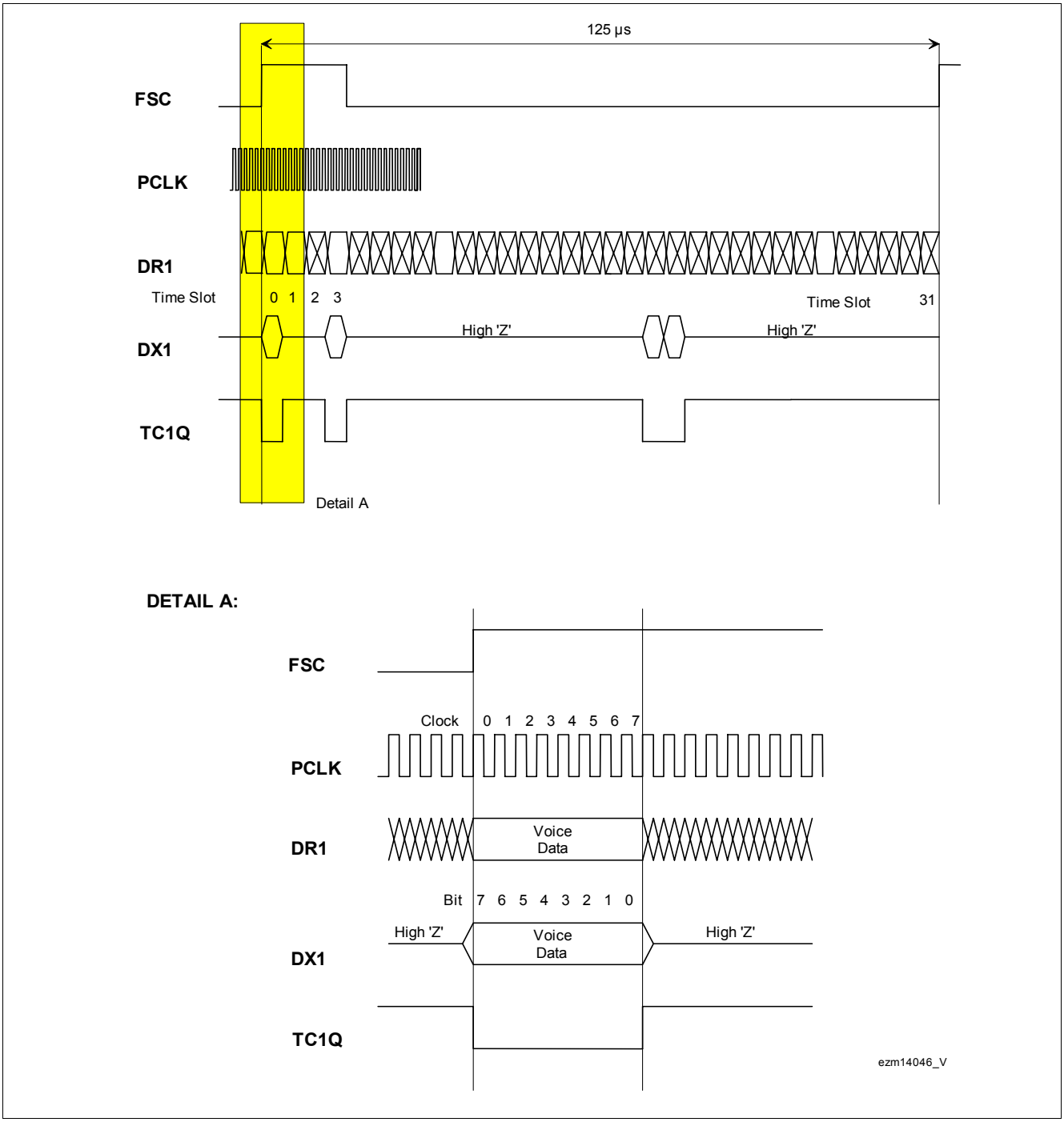

Figure 22 General PCM Interface Timing

The data rate of the interface can vary from 256 kbit/s to 8192 kbit/s. A frame may consist of up to 128 time slots of 8 bits each. The time slot assignment for each VINETIC®-2CPE/-1CPE channel can be programmed. Receive and transmit time slots can also be programmed individually (see **[3]**, **[4]**).

When the VINETIC®-2CPE/-1CPE is transmitting data on DX1, the TC1Q pin is switched to low to enable an external connected driving device.

Table 31 shows PCM interface frequency examples; other frequencies between 512 kHz and 8.192 MHz are also possible (such as 1536 kHz). The number of valid time slots is defined by the formulas at the end of **Table 31**:

Table 31 VINETIC®-2CPE/-1CPE PCM Interface Configuration

Clock Rate PCLK [kHz]	Single/Double Clock [1/2]	Time Slots [per highway]	Data Rate [kbit/s]
512	2	4	256
512	1	8	512
1024	2	8	512
1024	1	16	1024
2048	2	16	1024
2048	1	32	2048
4096	2	32	2048
4096	1	64	4096
8192	2	64	4096
8192	1	128	8192
$f = n*64*f_{FSC}$, $n \in [1,16]$ [1)]	1	f/64	f
$f = n*64*f_{FSC}$, $n \in [1,16]$ [1)]	2	f/128	f/2

1) n ... integer values, f_{FSC} = 8 kHz

4.3.2 Timing, PCM Interface

4.3.2.1 Single-Clocking Mode

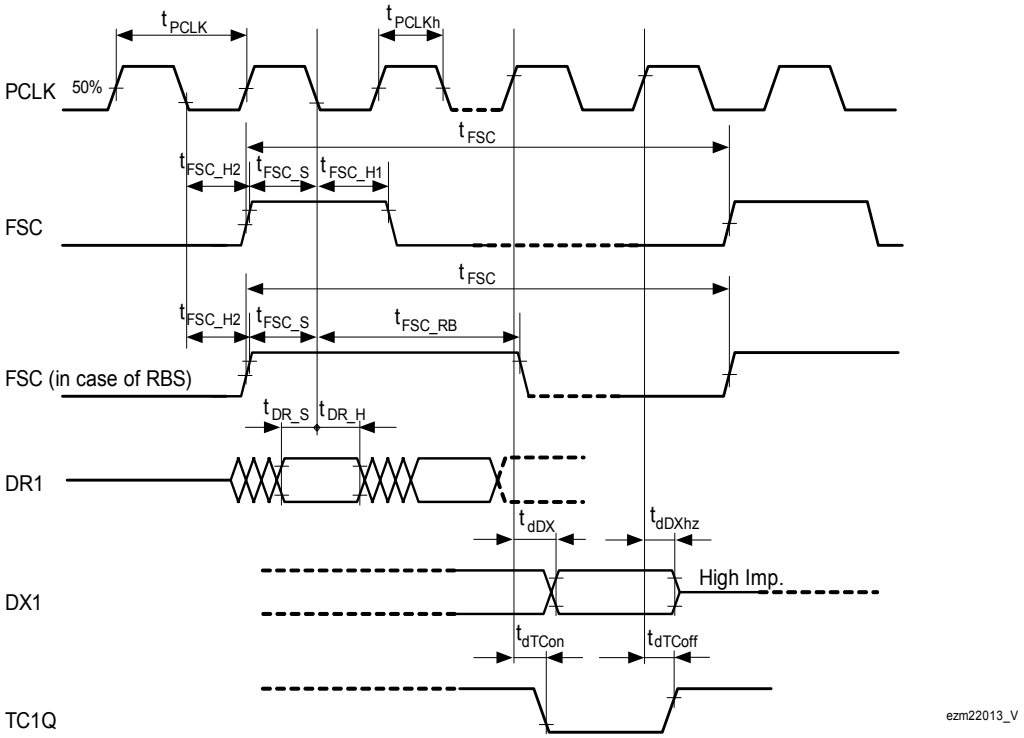

Figure 23 PCM Interface Timing – Single-Clocking Mode

Table 32 Timing Values, PCM Interface (Single-Clocking Mode)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Period PCLK[1)]	t_{PCLK}	1/8192	–	1/512	ms	–
PCLK high time	t_{PCLKh}	0.4 x t_{PCLK}	–	0.6 x t_{PCLK}	µs	–
Period FSC[1)]	t_{FSC}	–	125	–	µs	–
FSC setup time	t_{FSC_S}	10	–	–	ns	–
FSC hold time 1	t_{FSC_H1}	40	–	$t_{FSC} - t_{PCLK} - t_{FSC\_S}$[2)]	ns	–
FSC hold time in case of RBS	t_{FSC_RB}	$t_{FSC\_H1} + t_{PCLK}$	–	$t_{FSC} + 2 \times t_{PCLK} - t_{FSC\_S}$[2)]	ns	–
FSC hold time 2	t_{FSC_H2}	40	–	–	ns	–
DR1 setup time	t_{DR_S}	10	–	–	ns	–
FSC jitter time		–	–	± 0.2 x t_{PCLK}	ms	–
DR1 hold time	t_{DR_H}	10	–	–	ns	–
DX1 delay time[3)]	t_{dDX}	25	–	t_{dDX_min} + 0.4[ns/pF] x C_{Load}[pF]	ns	–
DX1 delay time to high Z	t_{dDXhz}	–	–	50	ns	–

Table 32 Timing Values, PCM Interface (Single-Clocking Mode) (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
TC1Q delay time on	t_{dTCon}	25	–	t_{dTCon_min} + 0.4[ns/pF] x C_{Load}[pF]	ns	–
TC1Q delay time off	t_{dTCoff}	25	–	t_{dTCoff_min} + 2 x R_{Pullup}[kΩ] x C_{Load}[pF]	ns	–

1) The PCLK frequency must be an integer multiple of the FSC frequency (n*64*f_{FSC}, n = 1..16).
2) This is to ensure that the FSC can be sampled low at least for one t_{PCLK} within t_{FSC}.
3) All delay times are made up of two components: an intrinsic time (min-time), caused by internal processing, and a second component caused by external circuitry (C_{Load}, R_{Pullup} > 1.5 kΩ)

4.3.2.2 Double-Clocking Mode

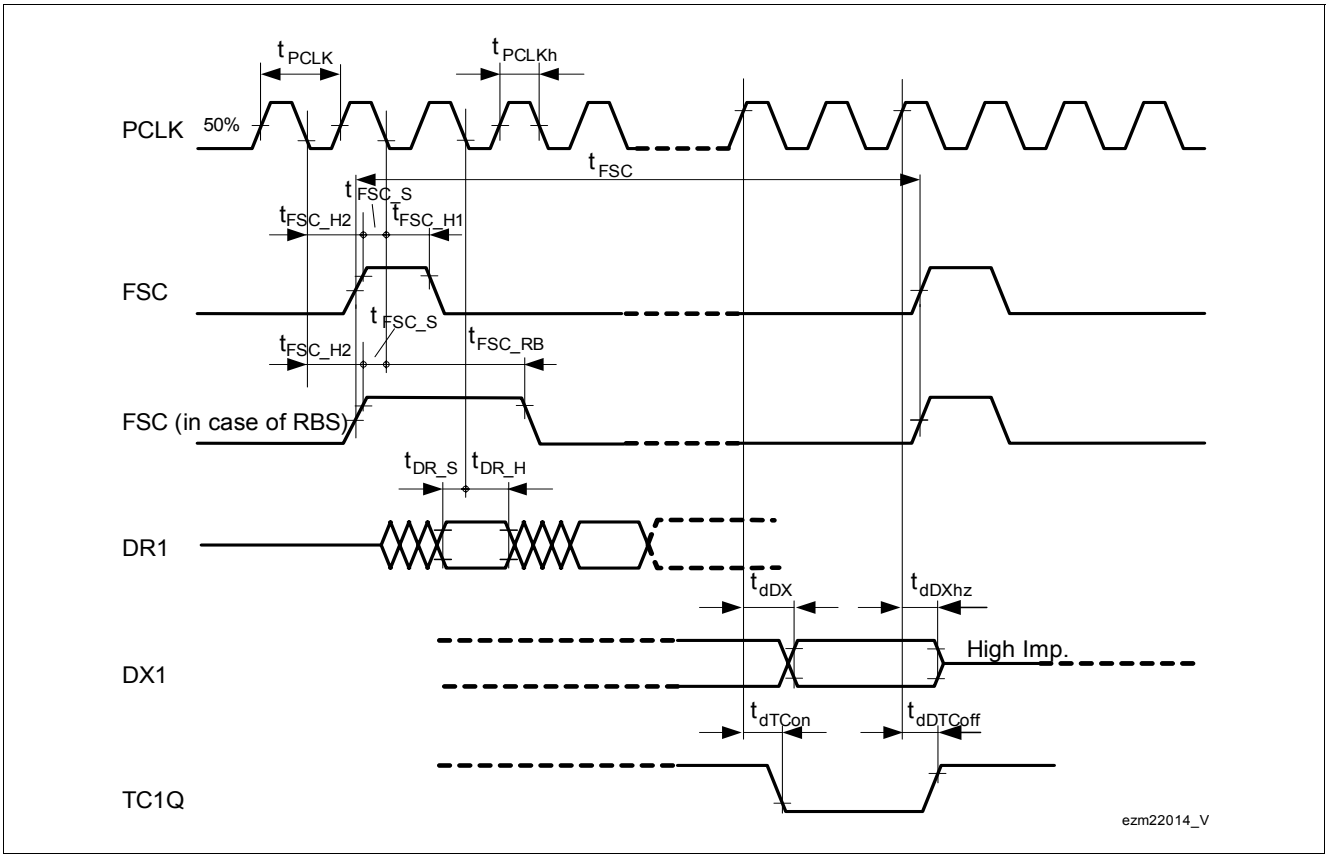

Figure 24 PCM Interface Timing – Double-Clocking Mode

Table 33 Timing Values PCM Interface (Double-Clocking Mode)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Period PCLK[1)]	t_{PCLK}	1/8192	–	1/512	ms	–
PCLK high time	t_{PCLKh}	0.4 x t_{PCLK}	–	0.6 x t_{PCLK}	µs	–
Period FSC[1)]	t_{FSC}	–	125	–	µs	–

Table 33 Timing Values PCM Interface (Double-Clocking Mode) (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
FSC setup time	t_{FSC_S}	10	–	–	ns	–
FSC hold time 1	t_{FSC_H1}	40	–	$t_{FSC} - t_{PCLK} - t_{FSC\_S}$ 2)	ns	–
FSC hold time 2	t_{FSC_H2}	40	–	–	ns	–
FSC hold time in case of RBS	t_{FSC_RB}	$t_{FSC\_H1} + t_{PCLK}$	–	$t_{FSC} + 2 \times t_{PCLK} - t_{FSC\_S}$ 2)	ns	–
FSC jitter time		–	–	$\pm 0.2 \times t_{PCLK}$	ms	–
DR1 setup time	t_{DR_S}	10	–	–	ns	–
DR1 hold time	t_{DR_H}	10	–	–	ns	–
DX1 delay time 3)	t_{dDX}	25	–	t_{dDX_min} + 0.4[ns/pF] x C_{Load}[pF]	ns	–
DX1 delay time to high Z	t_{dDXhz}	–	–	50	ns	–
TC1Q delay time on	t_{dTCon}	25	–	t_{dTCon_min} + 0.4[ns/pF] x C_{Load}[pF]	ns	–
TC1Q delay time off	t_{dTCoff}	25	–	t_{dTCoff_min} + 2 x R_{Pullup}[kΩ] x C_{Load}[pF]	ns	–

1) The PCLK frequency must be an integer multiple of the FSC frequency (n*64*f_{FSC}, n = 1..16).
2) This is to ensure that the FSC can be sampled low at least for one t_{PCLK} within t_{FSC}.
3) All delay times are made up of two components: an intrinsic time (min-time), caused by internal processing, and a second component caused by external circuitry (C_{Load}, R_{Pullup} > 1.5 kΩ)

4.4 Test Interface (JTAG Interface)

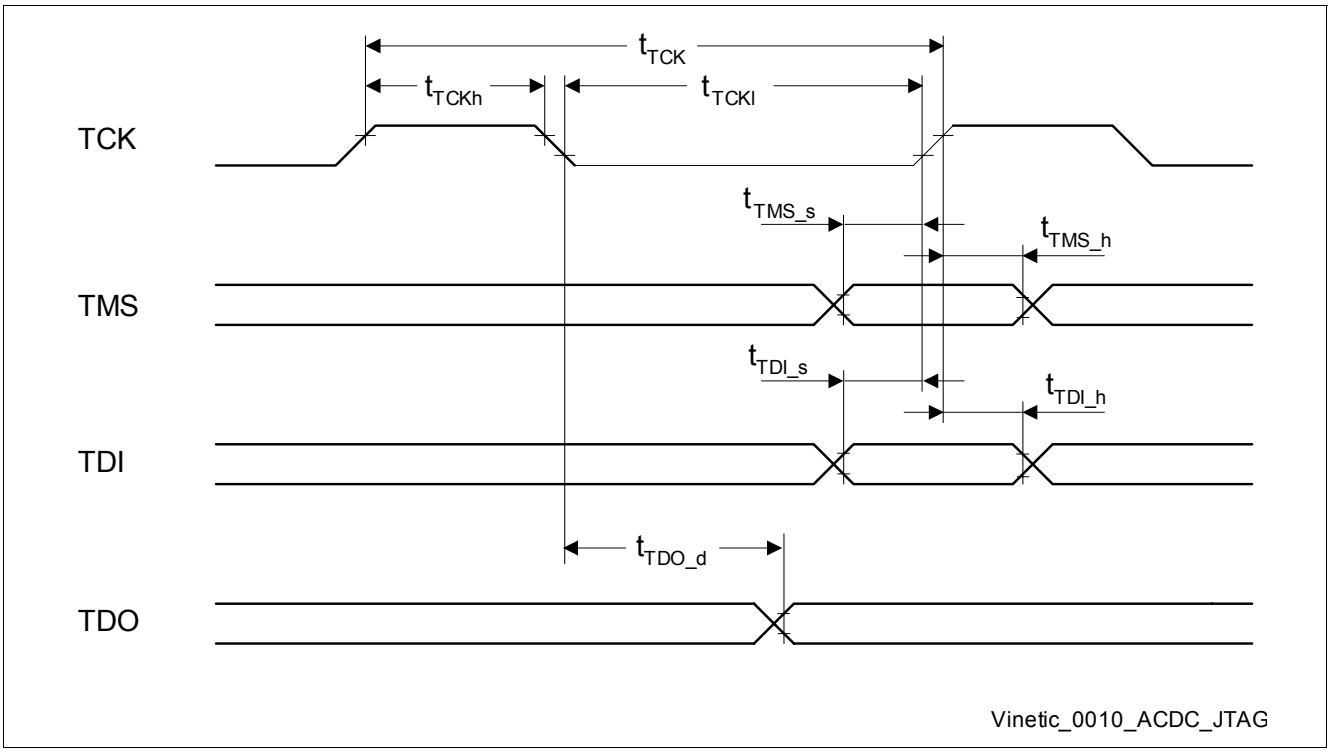

Figure 25 Test Interface (JTAG Interface) Timing

Table 34 Test Interface (JTAG Interface) Clocks

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
TCK Clock Period	t_{TCK}	100	–	–	ns	Pin TCK
TCK High Time	t_{TCKh}	40	–	–	ns	–
TCK Low Time	t_{TCKl}	40	–	–	ns	–

Table 35 Test Interface (JTAG Interface) Timing Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
TMS setup time	t_{TMS_s}	40	–	–	ns	Pin TMS
TMS hold time	t_{TMS_h}	40	–	–	ns	–
TDI setup time	t_{TDI_s}	40	–	–	ns	Pin TDI
TDI hold time	t_{TDI_h}	40	–	–	ns	–
Hold: TRSTQ after TCK	t_{TRSTQ_h}	10	–	–	ns	Pin TRSTQ
TDO valid delay	t_{TDO_d}	100	–	t_{dDOUT_min} + 0.4[ns/pF] x C_{Load}[pF]	ns	Pin TDO

4.5 SLIC Interface

The SLIC-DC (PEF 4268) Version 1.2 and the SLIC-E (PEF 4265, PEF 4365) Version 2.1 are controlled by ternary logic signals via the C1_x[1)] and C2_x[1)] pins.

For application circuits, please refer to **[2]**.

1) x stands for A, B or just for A - the 2 or 1 analog channels of the VINETIC®-2CPE/-1CPE

5 Electrical Characteristics

The following ratings are valid for all PEB/PEF 3332/-3331 product types.

In this chapter the following shortcuts for pin names and related voltages are used:

i = A, B, AB; x = A, B

Example: GND33_x = GND33_A, GND33_B; V_{GND15_i} = V_{GND15_A}, V_{GND15_B}, V_{GND15_AB}

5.1 Absolute Maximum Ratings VINETIC®-2CPE/-1CPE

Table 36 Absolute Maximum Ratings VINETIC®-2CPE/-1CPE

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Supply pins VDD15, VDD15_i, VDD15P referred to the corresp. ground pins GND, GND15_i, GND15P	–	–0.3	–	1.65	V	–
Supply pins VDD33, VDD33_x referred to the corresponding ground pins GND, GND33_x	–	–0.3	–	3.63	V	–
Ground pins GND15_i (GND33_x) referred to any other ground pins GND15_i, GND15P (GND33_x)	–	–0.3	–	0.3	V	–
Supply pins VDD15, VDD15_i referred to any other supply pin VDD15_i, VDD15P	–	–0.3	–	0.3	V	–
Analog input and output pins Pins DCP_x, DCN_x RING_x, TIP_x, IT_x, VCMIT_x, ITAC_x, ACP_x, ACN_x	 – –	 –0.3 –0.3	 – –	 3.63 1.65	 V V	V_{DD33_x} = 3.3 V, V_{DD15_i} = V_{DD15P} = 1.5 V, V_{GND15_i} = V_{GND15P} = V_{GND33_x} = 0 V
Digital input and output pins	–	–0.3	–	3.63	V	V_{DD33} = 3.3 V, V_{DD15} = 1.5 V, V_{GND} = 0 V
Digital input leakage current per pin	I_L	–50	–	50	µA	$0 \le V_{in} \le V_{DD33}$
DC input or output current at any input or output pin	–	–	–	100	mA	(free from latch-up)
Storage temperature	T_{STG}	–55	–	125	°C	–
Ambient temperature under bias	T_A	0 –40	– –	85 85	°C °C	For PEB 3332/-3331 for PEF 3332/-3331
Maximum junction temperature	T_J	–	–	125	°C	–
Power dissipation[1)]	P_D	– –	– –	0.8 1.1	W W	PG-TQFP-100 PG-TQFP-64

Table 36 Absolute Maximum Ratings VINETIC®-2CPE/-1CPE (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
ESD Robustness						
ESD voltage	–	–	–	2	kV	Human body model[2)]
ESD voltage, all pins	–	–	–	0.5	kV	SDM (Socketed Device Model)[3)]

1) According to JEDEC (four-layer board)
2) MIL STD 833D, method 3015.7 and ESD Assn. Standard S5.1-1993
3) EOS/ESD Assn. Standard DS5.3-1993

Attention: Stresses above the max. values listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Maximum ratings are absolute ratings; exceeding only one of these values may cause irreversible damage to the integrated circuit.

5.2 Operating Range VINETIC®-2CPE/-1CPE

$V_{GND} = V_{GND15\_i} = V_{GND15P} = V_{GND33\_x} = 0$ V

Table 37 Operating Range VINETIC®-2CPE/-1CPE

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Supply pins VDD15, VDD15_i, VDD15P referred to the corresp. ground pins GND, GND15_i, GND15P		1.425	1.5	1.575	V	–
Supply pins VDD33, VDD33_x referred to the corresponding ground pins GND, GND33_x		3.135	3.3	3.465	V	–
Analog input pins RING_x, TIP_x, IT_x referred to the corresp. pin VCMIT_x		–0.5	–	0.5	V	V_{DD15_i} = 1.5 V
Analog input pin ITAC_x referred to the corresp. pin VCMIT_x		–0.11	–	0.11	V	V_{DD15_i} = 1.5 V
Analog output pins: DCP_x, DCN_x ACP_x, ACN_x C1_x C2_x referred to the corresp. ground pins GND15_x, GND33_x		 0.25 0.2 0 0	 – – – –	 2.75 1.2 3.3 3.3	 V V V V	V_{DD33_x} = 3.3 V, V_{DD15_i} = 1.5 V $R_{DCP-DCN}$[1)] > 100 kΩ $R_{ACP-ACN}$[2)] > 20 kΩ I_{C1} < 220 µA
Analog pin VCMIT_x referred to the corresp. ground pin GND15_x		–	0.7	–	V	V_{DD15_AB} = 1.5 V
Analog pin for passive devices CREF_AB referred to the corresp. ground pin GND15_AB		0.5	0.7	0.9	V	V_{DD15_AB} = 1.5 V

Table 37 Operating Range VINETIC®-2CPE/-1CPE (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Digital Input/output Pins (I/O pins, GPIO pins)						
High-level input voltage	V_{IH}	2.0	–	3.6	V	V_{OUT} >= V_{OH} (min)
Low-level input voltage	V_{IL}	–0.3	–	0.8	V	V_{OUT} <= V_{OL} (max)
High-level output voltage	V_{OH}	2.4	–	–	V	I_{OH} = – 3 mA
Low-level output voltage	V_{OL}	–	–	0.4	V	I_{OL} = 3 mA
Average input leakage current per pin	I_{IL}	–	–	20	µA	V_{DD33} = 3.3 V, V_{GND} = 0 V; all other pins are floating, V_{IN} = 0 V or 3.3 V
Input capacitance at digital signal pins (except RING_x, TIP_x)		–	–	5	pF	–
Input transition rise or fall time at digital signal pins (except RING_x, TIP_x)		0	–	5	ns	–
Output transition rise or fall time at digital signal pins (except RING_x, TIP_x)		–	–	7.4	ns	$C_{Load,max}$ = 50 pF
Pull-up resistor on chip	$R_{pull-up}$	–	500	–	kΩ	–
Digital Input Pins (IFSEL0, IFSEL1)[3)]						
Pull up current[4)]		–15	–6.6	–3	µA	V_{pin} = 0 V
Digital Input Pin MCLK[5)]						
High-level input voltage	V_{IH}	1.1	–	3.6	V	
Low-level input voltage	V_{IL}	–0.3	–	0.45	V	
Analog Input Pins (RING_x, TIP_x)						
Input impedance (RING_x, TIP_x): single input measurement (RING_x, TIP_x to GND15_x)	$R_{RTinS,G}$[6)]	600	750	900	kΩ	
Input impedance (RING_x, TIP_x): differential measurement (RING_x to TIP_x)	R_{RTinD}[6)]	1200	1500	1800	kΩ	
Input impedance (RING_x, TIP_x): differential measurement (RING_x,TIP_x to VCMIT_x)	$R_{RTinD,V}$[6)]	800	1000	1200	kΩ	
Ambient temperature under bias	T_A	0 –40	– –	85 85	°C °C	For PEB 3332/-3331 for PEF 3332/-3331
Junction temperature under bias	T_J	0	–	125	°C	–

1) Resistance between DCP and DCN pins
2) Resistance between ACP and ACN pins
3) Only available in PG-TQFP-100 packages
4) On chip pull-up resistor
5) The MCLK pin has no input hysteresis. For wave form requirements refer to **Chapter 3.2**
6) Not subject for production test - verified by design/characterization

5.2.1 Thermal Resistance VINETIC®-2CPE/-1CPE

Table 38 Thermal Resistance VINETIC®-2CPE/-1CPE

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Junction to case	$R_{th,JC}$	– –	10 12.5	– –	K/W K/W	PG-TQFP-100 PG-TQFP-64
Junction to ambient for 4-layer 100x100 JEDEC board	$R_{th,JA}$	– –	44.1 35.3	– –	K/W K/W	PG-TQFP-100 PG-TQFP-64

5.2.2 Power Consumption VINETIC®-2CPE/-1CPE

T_A = 25 °C

V_{DD15} = V_{DD15_i} = V_{DD15P} = 1.5 V ± 5 %

V_{DD33} = V_{DD33_x} = 3.3 V ± 5 %

V_{GND} = V_{GND15_i} = V_{GND15P} = V_{GND33_x} = 0 V

Table 39 Power Consumption VINETIC®-2CPE

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Power Consumption in Operation Modes[1)]						
DISABLED all channels	$P_{DD15,DIS}$ $P_{DD33,DIS}$	– –	60 10[2)]	80 15[2)]	mW mW	Basic EDSP load of ~20 Mcycles/s included
STANDBY all channels	$P_{DD15,STBY}$ $P_{DD33,STBY}$	– –	65 10[2)]	85 15[2)]	mW mW	Basic EDSP load of ~20 Mcycles/s included
ACTIVE one channel, **DISABLED** other channel	$P_{DD15,ACT,DIS}$ $P_{DD33,ACT,DIS}$	– –	100[3)] 20[2)]	120[3)] 25[2)]	mW mW	Basic EDSP load plus 1ch. ALM and PCM load of ~26 Mcycles/s included
ACTIVE one channel, **STANDBY** other channel	$P_{DD15,ACT,STBY}$ $P_{DD33,ACT,STBY}$	– –	105[3)] 20[2)]	125[3)] 25[2)]	mW mW	Basic EDSP load plus 1ch. ALM and PCM load of ~26 Mcycles/s included
ACTIVE all channels	$P_{DD15,ACT}$ $P_{DD33,ACT}$	– –	125[3)] 25[2)]	150[3)] 30[2)]	mW mW	Basic EDSP load plus 2ch. ALM and PCM load of ~26 Mcycles/s included
EDSP Module[4)]						
ACTIVE	$P_{DD15,EDSP}$	–	1.5	2	mW/Mcycles	EDSP power consumption, max. EDSP load: 163.8 Mcycles/s

1) To calculate total power consumption, the values for both supply voltages (3.3 V and 1.5 V) have to be summed up.
2) Depends on the load of the external circuitry at the I/O pins.
3) Depends on the EDSP load used.
4) For estimation of power consumption with different EDSP loads.

Table 40 Power Consumption VINETIC®-1CPE

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Power Consumption in Operation Modes[1]						
DISABLED	$P_{DD15,DIS}$ $P_{DD33,DIS}$	– –	55 10[2]	75 15[2]	mW mW	Basic EDSP load of ~20 Mcycles/s included
STANDBY	$P_{DD15,STBY}$ $P_{DD33,STBY}$	– –	60 10[2]	80 15[2]	mW mW	Basic EDSP load of ~20 Mcycles/s included
ACTIVE	$P_{DD15,ACT}$ $P_{DD33,ACT}$	– –	90[3] 20[2]	110[3] 25[2]	mW mW	Basic EDSP load plus 1ch. ALM and PCM load of ~26 Mcycles/s included
EDSP Module[4]						
ACTIVE	$P_{DD15,EDSP}$	–	1.5	2	mW/Mcycles	EDSP power consumption, max. EDSP load: 163.8 Mcycles/s

1) To calculate total power consumption, the values for both supply voltages (3.3 V and 1.5 V) have to be summed up.
2) Depends on the load of the external circuitry at the I/O pins.
3) Depends on the EDSP load used.
4) For estimation of power consumption with different EDSP loads.

5.2.3 Power-On Sequence VINETIC®-2CPE/-1CPE

There are no particular requirements on the power-on sequence for the VDD15[1] and VDD33[2] supply voltages. It is mandatory to apply the signal voltages after the VDD15 and VDD33 voltages are supplied and stable.

5.3 Transmission Characteristics VINETIC®-2CPE/-1CPE

The AC transmission characteristics are specified in [3] and are referred to a complete system including the SLIC-DC Version 1.2 or SLIC-E Version 2.1 and external components.

1) VDD15, VDD15_i
2) VDD33, VDD33_x

6 Package Outlines

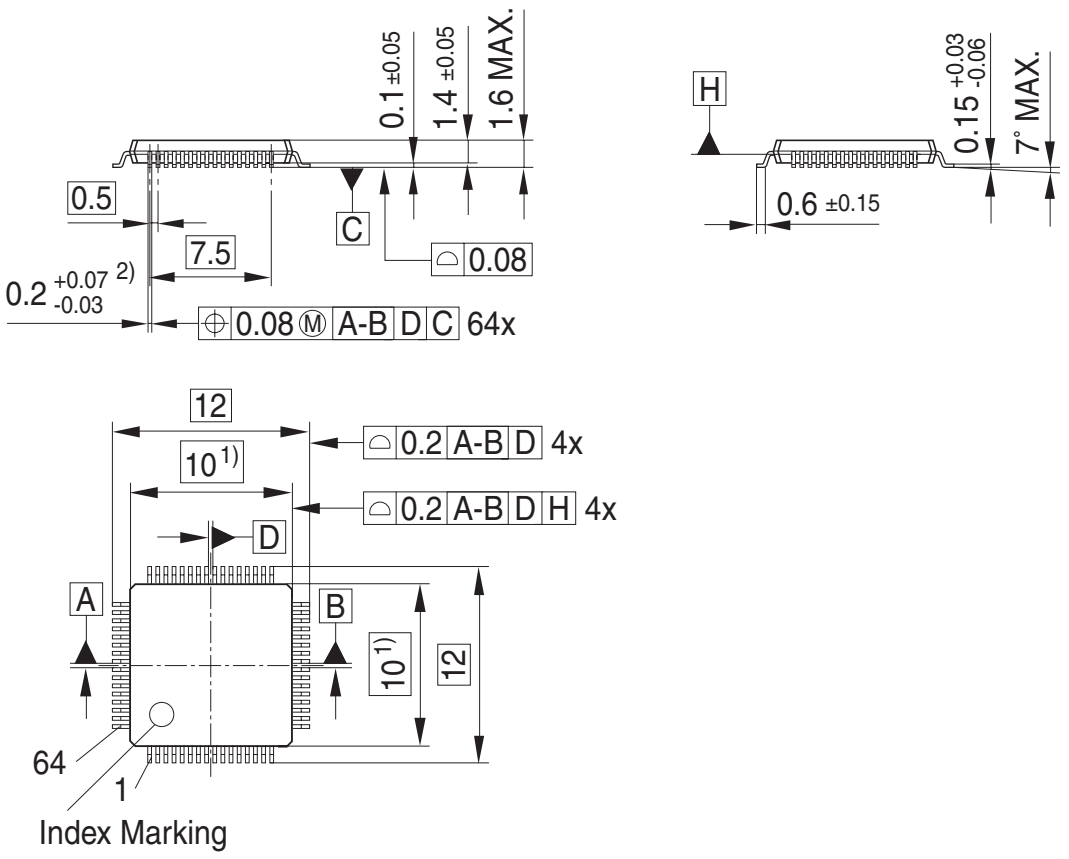

Figure 26 **PG-TQFP-64-17** (Plastic Green Thin Quad Flat Package)

Dimensions in mm

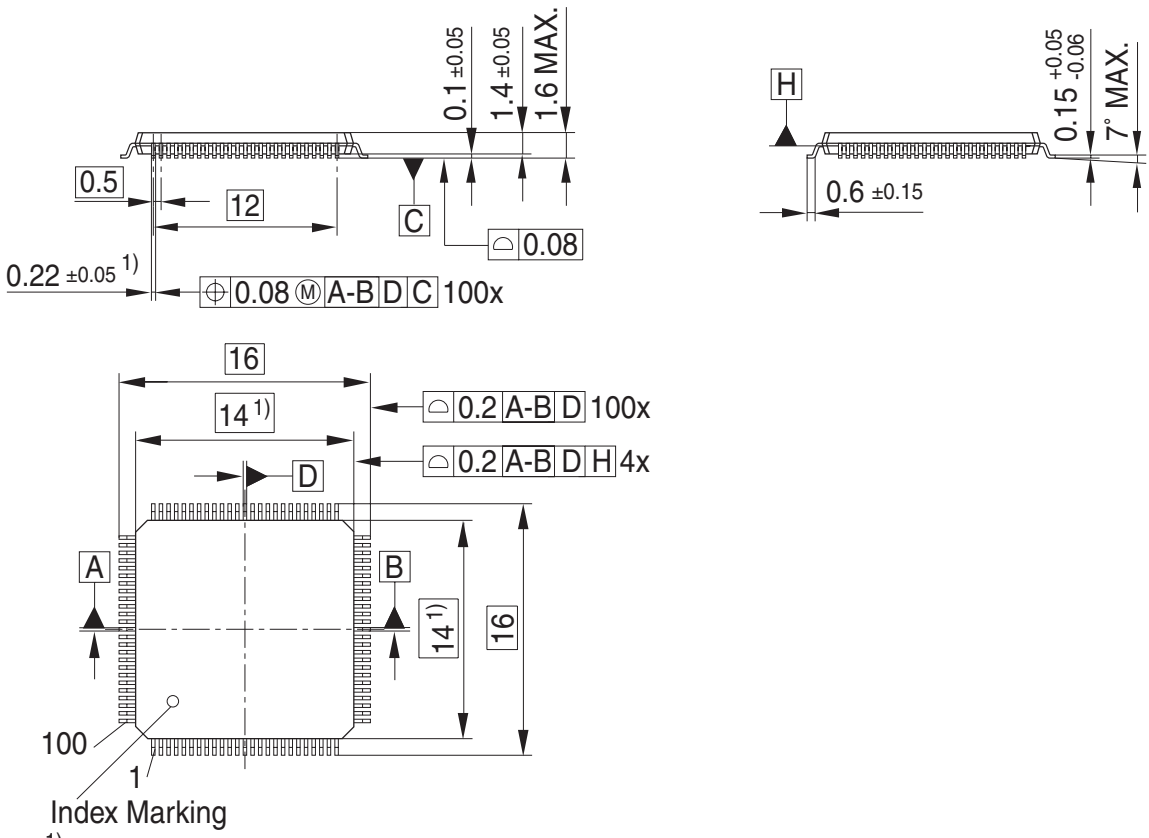

Figure 27 PG-TQFP-100-18 (Plastic Green Thin Quad Flat Package)

Dimensions in mm

TAPI Interface Function Call Synonyms

Table 41 lists synonyms for operation modes of the VINETIC® used in this document and the corresponding TAPI interface function calls. For details on the function calls see [4].

Table 41 TAPI Interface Function Call Synonyms

TAPI Interface Function Call	Synonym for Operation Modes
IFX_TAPI_LINE_FEED_ACTIVE	ACTIVE
IFX_TAPI_LINE_FEED_STANDBY	STANDBY
IFX_TAPI_LINE_FEED_HIGH_IMPEDANCE	HIGH_IMPED
IFX_TAPI_LINE_FEED_DISABLED	DISABLED
IFX_TAPI_LINE_FEED_RING_BURST	RING_BURST

Literature References

[1] VINETIC®-CPE Version 2.2 Product Overview Rev. 1.0, 2006-10-09

[2] VINETIC®-2CPE/-1CPE (PEB 3332/-3331) Version 2.2 Hardware Design Guide Rev. 1.0, 2006-08-16

[3] VINETIC®-CPE Prel. User's Manual System Description Rev. 2.1, in preparation

[4] TAPI User's Manual Programmer's Reference Rev. 1.4, 2007-03-13

[5] VINETIC®-CPE Device Driver User's Manual Programmer's Reference Rev. 1.2, 2006-09-01

[6] VINETIC®-CPE System Errata Sheet Rev. 2.0, 2006-08-24

[7] VINETIC®-CPE System Package Release Notes

Attention: Please refer to the latest revision of the documents.

Standards References

[8] ETSI Standard ES 202 971 V1.2.1, (2006-01), Access and Terminals (AT); Public Switched Telephone Network (PSTN); Harmonized specification of physical and electrical characteristics of a 2-wire analogue interface for short line interface

[9] ITU-T Recommendation Q.552, (11/2001), Transmission characteristics at 2-wire analogue interfaces of digital exchanges

[10] Telcordia Technologies GR-909-CORE Issue 2 December 2004, Generic Criteria for Fiber in the Loop Systems

Terminology

A	
A/D	Analog to digital
AAL2	ATM Adaption Layer 2
AC	Alternative Current
ADC	Analog Digital Converter
AITDF	Advanced Integrated Test and Diagnostic Functions
ALM	Analog Line Module
ATD	Answering Tone Detector
ATM	Asynchronous Transfer Mode
C	
CAS	Channel Associated Signaling
CNG	Comfort Noise Generation
Codec	Coder Decoder
CPE	Customer Premises Equipment
CRAM	Coefficient RAM
D	
DAA	Data Access Arangement
DAC	Digital Analog Converter
DC	Direct Current
DSP	Digital Signal Processor
DTMF	Dual Tone Multi Frequency
E	
EXP	Expander
F	
FRR	Frequency Response Receive filter
FRX	Frequency Response Transmit filter
FSK	Frequency Shift Keying
FTTH	Fiber to the Home
FXO	Foreign eXchange Office
FXS	Foreign eXchange Subscriber
G	
GPIO	General Purpose Input/Output
H	
HW	Hardware
I	
IAD	Integrated Access Device
ITU	International Telecommunication Union
IP	Internet Protocol
ISDN	Integrated Services Digital Network
J	
JTAG	Joint Test Action Group

L	
LSSGR	Local area transport access Switching System Generic Requirements
N	
NG-DLC	Next Generation Digital Loop Carrier
NT	Network Terminal
P	
PBX	Private Branch eXchange
PCM	Pulse Code Modulation
POTS	Plain Old Telephone Service
R	
RAM	Random Access Memory
RBS	Robbed Bit Signaling
RoHS	Reduction of Hazardous Substances (directive of the european parliament and by environmental initiatives of other countries worldwide)
RTCP	Real-time Transport Control Protocol
RTP	Real-time Transport Protocol
S	
SLIC	Subscriber Line Interface Circuit (same for all versions)
SOHO	Small Office/Home Office
T	
TDM	Time Division Multiplexing
TG	Tone Generator
TH	Transhybrid Balancing
TS	Time Slot
TTX	Teletax (Metering)
U	
UTD	Universal Tone Detection
UTG	Universal Tone Generator
V	
VAD	Voice Activity Detection
VINETIC®	Voice and Internet Enhanced Telephony Interface Concept
VINETICOS	Voice and Internet Enhanced Telephony Interface Concept Coefficients Calculation Software
VoATM	Voice over ATM
VoDSL	Voice over DSL
VoIP	Voice over IP
W	
WLL	Wireless Local Loop
X	
xDSL	(all flavors of) Digital Subscriber Line

w w w . i n f i n e o n . c o m

Published by Infineon Technologies AG