

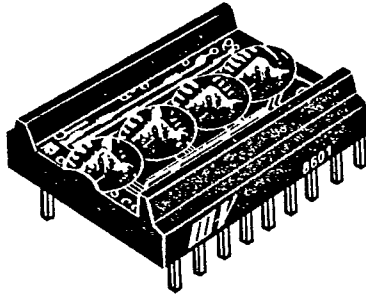
F.19-36

**ALPHANUMERIC  
INTEGRATED DISPLAY**DL2416  
TSM2416

T-41-37



THREE-FIVE SYSTEMS, INC.

**FEATURES**

- Internal Memory, Decoder, Multiplexer & Driver
- 17th Segment for Improved Punctuation Marks
- End-Stackable
- Microprocessor Bus Compatible
- Compatible TTL Inputs and Power Supply
- 4 Red Characters Magnified to 0.160"
- Wide Viewing Angle  $\pm 50^\circ$
- 64-Character ASCII Format
- Rugged Package—Totally Plastic Encapsulated
- Independent and Asynchronous Digit Access
- Independent Cursor Function
- Memory Clear and Display Functions
- Intensity Coded for Uniform Displays

**ABSOLUTE MAXIMUM RATINGS**

Voltage at Any Pin:  $-0.3V$  to  $V_{CC} + 0.3V$   
 Operating Voltage Range ( $V_{CC}$ ):  $3.0V$  to  $6.0V$   
 Operating Temperature:  $-40^\circ C$  to  $85^\circ C$   
 Storage Temperature:  $-40^\circ C$  to  $85^\circ C$   
 Relative Humidity at  $60^\circ C$ : 90%  
 Absolute Maximum  $V_{CC}$ :  $6.5V$

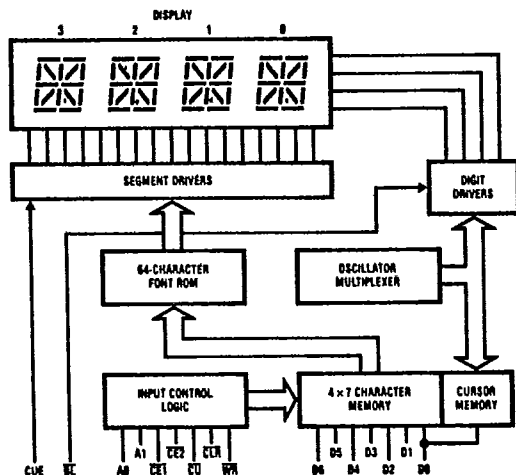
**DESCRIPTION**

The DL2416/TSM2416 has four 17 segment alphanumeric display digits and an internal CMOS driver. The four 17 segment monolithic LEDs are magnified by an immersion bubble lens system.

The integrated CMOS drive chip has memory to store four 7-bit ASCII words (corresponding to the four digits), an ASCII to 17 segment alphanumeric ROM decoder, and multiplexing and drive circuitry to drive the four 17 segment monolithic digits. Inputs and power supply requirements are TTL compatible. Data can be entered directly from a microprocessor bus without additional interface circuitry. Data can be written asynchronously through the seven bit data bus into a digit location addressed by the two-bit address bus.

Two or more DL2416/TSM2416s can be assembled in series by connecting data lines in parallel to the data bus. Similarly, address lines are connected in parallel to the address bus. Write and cursor lines are also parallel. Two chip enables are used to select the desired 4-digit group in up to four individual displays (up to sixteen digits). For displays requiring more than 4 displays (16 digits), extended addresses can be obtained with a 1 or N decoder IC.

The cursor function causes 16 of the 17 segments of a digit to light without disturbing the contents of the memory for that digit. When the cursor is removed, the character previously displayed returns. A cursor enable CUE is provided for flexibility of control.

**BLOCK DIAGRAM**

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# ALPHANUMERIC INTEGRATED DISPLAY

## DL2416/TSM2416

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### DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Conditions	-40°C			25°C			85°C			Units
			Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
V <sub>CC</sub>	Supply Voltage	V <sub>CC</sub> = 5.0V				4.5						V
I <sub>CC</sub>	Supply Current—4 Digits on (10 Seg/Dig)	V <sub>CC</sub> = 5.0V		75	150		65	120		50	90	mA
I <sub>CC(CUR)</sub>	I <sub>CC</sub> Cursor (16 Seg/Dig)	V <sub>CC</sub> = 5.0V, V <sub>IN</sub> = 0		95	180		85	160		65	140	mA
I <sub>CC(BL)</sub>	I <sub>CC</sub> Blank	V <sub>CC</sub> = 5.0V, WR = 5.0V, V <sub>IN</sub> = 0		1.0	2.7		0.9	2.4		0.6	2.1	mA
I <sub>IL</sub>	Input Current, Max.	V <sub>CC</sub> = 5.0V, V <sub>IN</sub> = 0.8V		30	120		25	100		20	80	μA
V <sub>IL</sub>	Input Voltage, Low	V <sub>CC</sub> = 5.0V ± 0.5V			0.8			0.8			0.8	V
V <sub>IH</sub>	Input Voltage, High	V <sub>CC</sub> = 5.0V ± 0.5V	2.4			2.4			2.4			V

### AC TIMING CHARACTERISTICS

Guaranteed Minimum Timing at Specified Temperatures at V<sub>CC</sub> = 4.5V.

Symbol	Parameter	-40°C	25°C	85°C	Units
t <sub>AS</sub>	Address Set Up Time	240	300	360	ns
t <sub>WD</sub>	Write Delay Time	45	60	75	ns
t <sub>W</sub>	Write Time	195	240	285	ns
t <sub>DS</sub>	Data Set-Up Time	80	100	120	ns
t <sub>DH</sub>	Data Hold Time	40	50	60	ns
t <sub>AH</sub>	Address Hold Time	0	0	0	ns
t <sub>CLR</sub>	Clear Time	0.8	1.0	1.2	μs
t <sub>CES</sub>	Chip Enable Set-Up Time	240	300	360	ns
t <sub>ACC</sub>	Access Time	280	350	420	ns
t <sub>CEH</sub>	Chip Enable Hold Time	0	0	0	ns

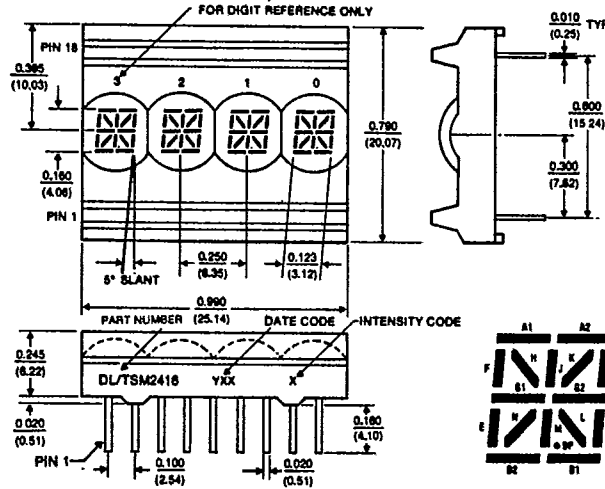
### OPTICAL CHARACTERISTICS

T<sub>A</sub> = 25°C

Parameter	Conditions	Min	Typ	Max	Units
Luminous Intensity per Digit	V <sub>CC</sub> = 5.0V, 8 Segs On	0.5	1.0		mcd
Intensity Matching, Within a Digit	V <sub>CC</sub> = 5.0V		±33		%
Off-Axis Viewing Angle	V <sub>CC</sub> = 5.0V		±50		degrees
Digit Size			160		mils
Peak Wavelength	V <sub>CC</sub> = 5.0V		655		nm

- | Pin No. | Electrical Connection |
|---------|-----------------------|
| 1       | CE1 Chip Enable 1     |
| 2       | CE2 Chip Enable 2     |
| 3       | CLR Clear             |
| 4       | CUE Cursor Enable     |
| 5       | CU Cursor Select      |
| 6       | WR Write              |
| 7       | A1 Digit Select       |
| 8       | A0 Digit Select       |
| 9       | V <sub>CC</sub>       |
| 10      | GND                   |
| 11      | D0 Data Input         |
| 12      | D1 Data Input         |
| 13      | D2 Data Input         |
| 14      | D3 Data Input         |
| 15      | D6 Data Input         |
| 16      | D5 Data Input         |
| 17      | D4 Data Input         |
| 18      | BL Blanking           |

### PHYSICAL DIMENSIONS



DIMENSIONS: INCHES  
(Millimeters)

TOLERANCES: 0.XXX ± 0.010  
(X.XX ± 0.25)



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INTEGRATED DISPLAYS

# ALPHANUMERIC INTEGRATED DISPLAY DL2416/TSM2416

F-19-36  
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## FUNCTION DESCRIPTION

Control						Address		Data Input							Digit	Digit	Digit	Digit	
BL	CE1	CE2	CUE	CU	WR	CLR	A1	A0	D6	D5	D4	D3	D2	D1	D0	3	2	1	0
H	X	X	L	X	H	H			Previously Loaded Display							F	O	U	R
H	H	X	L	X	X	H	X	X	X	X	X	X	X	X	X	F	O	U	R
H	X	H	L	X	X	H	X	X	X	X	X	X	X	X	X	F	O	U	R
H	L	L	L	H	L	H	L	L	H	L	L	L	H	L	H	F	O	U	R
H	L	L	L	H	L	H	L	H	H	L	L	H	H	H	L	F	O	N	E
H	L	L	L	H	L	H	H	L	H	L	L	H	L	L	H	F	I	N	E
H	L	L	L	H	L	H	H	H	H	L	L	H	H	H	L	N	I	N	E
L	X	X	X	X	H	H	X	X	Blank Display										
H	L	L	L	H	L	H	H	H	Clears Character Displays							L	I	N	E
H	X	X	L	X	H	L	X	X	See Character Code							See Character Set			
H	L	L	L	H	L	H	X	X											

**Loading Data**—Data entry may be asynchronous and random. CE1 and CE2 must be held low and CU must be held high to enable data entry. The data code (D0-D6), which selects one of the 64-character sets and digit address

(A0-A1) are held stable while WR is held low. This stores the appropriate character from the character set into the digit specified by A0 and A1. This data is maintained for that digit until new data is entered. X = Don't care.

Control						Address		Data Input							Digit	Digit	Digit	Digit	
BL	CE1	CE2	CUE	CU	WR	CLR	A1	A0	D6	D5	D4	D3	D2	D1	D0	3	2	1	0
H	X	X	L	X	H	H			Previously Loaded Display							B	E	A	R
H	X	X	H	X	H	H			Display Previously Stored Cursors							B	E	A	R
H	L	L	H	L	L	H	L	L	X	X	X	X	X	X	H	B	E	A	☒
H	L	L	H	L	L	H	L	H	X	X	X	X	X	X	H	B	☒	☒	☒
H	L	L	H	L	L	H	H	H	X	X	X	X	X	X	H	☒	☒	☒	☒
H	L	L	H	L	L	H	H	L	X	X	X	X	X	X	L	☒	E	☒	☒
H	X	X	L	X	H	H			Disable Cursor Display							B	E	A	R
H	L	L	L	L	L	H	H	H	X	X	X	X	X	X	L	B	E	A	R
H	X	X	H	X	H	H			Display Stored Cursor							B	E	☒	☒

**Entry Into Cursor Memory**—This is accomplished by setting the CE1 and CE2 inputs—as well as the CU input—low. The cursor memory consists of 4 bits corresponding to the four digits, each one addressable by way of the A0 and A1 inputs. Once the address and data are stable, the WR input must go high and the cursor memory will respond to the D0 input. That is, if D0 is high, a cursor will be written and if D0 is low, the cursor will be erased.

CLR will not erase a cursor. A cursor will only be displayed when CUE is high and the cursor function can be bypassed by tying CUE low. A flashing cursor can be implemented by pulsing CUE; this results in alternately displaying the cursor and the character originally written in that digit. Cue will not alter the contents of either the cursor or data memory.

Note: Cursor must be cleared during power up.

X = Don't care.

**Illegal Code**—If an illegal ASCII code is entered as the data code (i.e., D6 = D5) the display will automatically be blanked for the corresponding digit.

ing CLR low for 1 μs. This will not clear the cursor memories.

**Initializing and Clearing the Display**—To initialize the device after power-up, enter a legal data code set (D6 ≠ D5), and then clear cursors for each digit. Alternately, all internal data memories can be cleared by hold-

**Display Blanking**—In addition to blanking of the display by loading a blank or space into each digit data memory, this may be accomplished by setting the display blank input BL low. This will not affect the contents of either the data or cursor memories.



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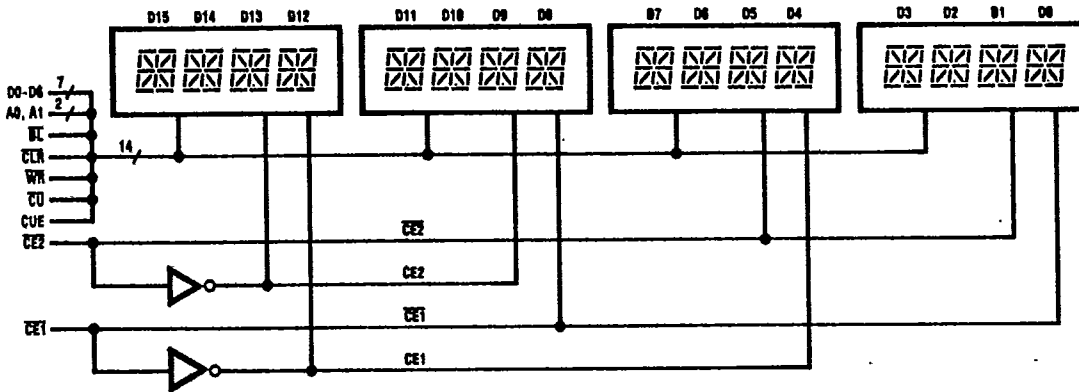
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## TYPICAL APPLICATION CIRCUIT



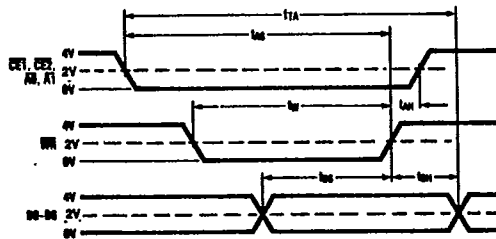
Interconnect for ≤ 16 Digit Systems

INTEGRATED  
DISPLAYS

## CHARACTER SET

CHARACTER SET	D0				D1			
	L	H	L	H	L	H	L	H
L H L L	.	"	4	5	6	7	8	9
L H L H	<	>	*	+	-	.	/	
L H H L	0	1	2	3	4	5	6	7
L H H H	8	9	-	/	\	=	\	?
H L L L	A	F	B	C	D	E	F	G
H L L H	H	I	J	K	L	M	N	O
H L H L	P	Q	R	S	T	U	V	W
H L H H	X	Y	Z	[	\	]	^	_

## TIMING DIAGRAM



The DL2416/TSM2416 is a CMOS device and normal precautions should be taken to avoid static damage.



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