4-Bit Bidirectional Universal Shift Register

- Buffered clock and control inputs
- Shift left and shift right capability
- Synchronous parallel and serial data transfers
- Easily expanded for both serial and parallel operation
- Asynchronous Master Reset
- Hold (do nothing) mode

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (Total)
74194	36MHz	39mA
74LS194A	36MHz	15mA
74S194	105MHz	85mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGES V_{CC} = 5V ±5%; T_A = 0°C to +70°C	MILITARY RANGES V_{CC} = 5V ±10%; T_A = −55°C to +125°C
Plastic DIP	N74194N • N74LS194AN N74S194N	
Plastic SO	N74LS194AD • N745194D	
Ceramic DIP		S54194F • S54LS194AF S54S194F
Flatpack		S54194W • S54LS194AW S54S194W
LLCC		S54194G

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	54/74	54/74S	54/74LS
All	Inputs	1ul	1Sul	1LSul
Q_0-Q_3	Outputs	10ul	10Sul	10LSul

NOTE
Where a 54/74 unit load (ul) is understood to be 40μA I_{IH} and −1.6mA I_{IL}, a 54/74S unit load (Sul) is 50μA I_{IH} and −2.0mA I_{IL}, and 54/74LS unit load (LSul) is 20μA I_{IH} and −0.4mA I_{IL}.

DESCRIPTION

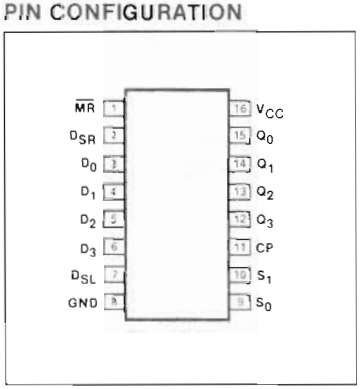
The functional characteristics of the '194 4-Bit Bidirectional Shift Register are indicated in the Logic Diagram and Function Table. The register is fully synchronous, with all operations taking place in less than 20ns (typical) for the 54/74 and 54LS/74LS, and 12ns (typical) for 54S/74S, making the device especially useful for implementing very high speed CPUs, or for memory buffer registers.

The '194 design has special logic features which increase the range of application. The synchronous operation of the device is determined by two Mode Select inputs, S_0 and S_1. As shown in the Mode Select Table, data can be entered and shifted from left to right (shift right, $Q_0 \rightarrow Q_1$, etc.) or, right to left (shift left, $Q_3 \rightarrow Q_2$, etc.) or, parallel data can be entered, loading all 4 bits of the register simultaneously. When both S_0 and S_1 are LOW, existing data is retained in a hold (do nothing) mode. The first and last stages provide D-type Serial Data inputs (D_{SR}, D_{SL}) to allow multistage shift right or shift left data transfers without interfering with parallel load operation.

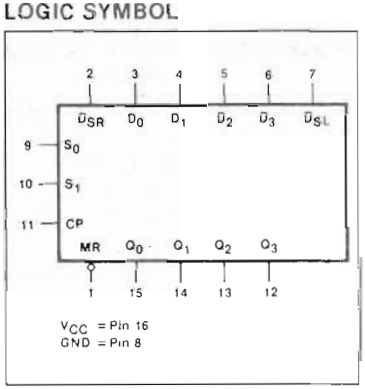
Mode Select and Data inputs on the 54S/74S194 and 54LS/74LS194A are edge-triggered, responding only to the LOW-to-HIGH transition of the Clock (CP). Therefore, the only timing restriction is that the Mode Control and selected Data inputs must be stable one setup time prior to the positive transition of the clock pulse. The Mode Select inputs of the 54/74194 are gated with the clock and should be changed from HIGH-to-LOW only while the Clock input is HIGH.

The four parallel data inputs (D_0-D_3) are D-type inputs. Data appearing on D_0-D_3 inputs when S_0 and S_1 are HIGH is transferred to the Q_0-Q_3 outputs respectively, following the next LOW-to-HIGH transition of the clock. When LOW, the asynchronous Master Reset ($\overline{MR}$) overrides all other input conditions and forces the Q outputs LOW.

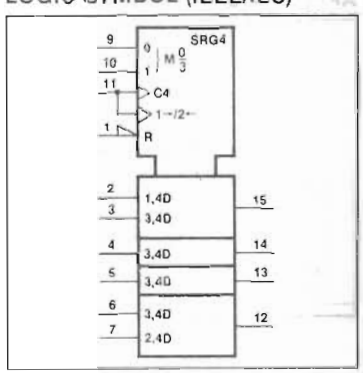
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



MODE SELECT—FUNCTION TABLE

OPERATING MODE	INPUTS							OUTPUTS			
	CP	$\overline{MR}$	S_1	S	D_{SR}	D_{SL}	D_n	Q_0	Q_1	Q_2	Q_3
Reset (clear)	X	L	X	X	X	X	X	L	L	L	L
Hold (do nothing)	X	H	l[a]	l[a]	X	X	X	q_0	q_1	q_2	q_3
Shift Left	↑	H	h	l[a]	X	l	X	q_1	q_2	q_3	L
	↑	H	h	l[a]	X	h	X	q_1	q_2	q_3	H
Shift Right	↑	H	l[a]	h	l	X	X	L	q_0	q_1	q_2
	↑	H	l[a]	h	h	X	X	H	q_0	q_1	q_2
Parallel Load	↑	H	h	h	X	X	d_n	d_0	d_1	d_2	d_3

H = HIGH voltage level

h = HIGH voltage level one setup time prior to the LOW to HIGH clock transition

L = LOW voltage level

l = LOW voltage level one setup time prior to the LOW-to-HIGH clock transition

$d_n(q_n)$ = Lower case letters indicate the state of the referenced input (or output) one setup time prior to the LOW to-HIGH clock transition.

X = Don't care

↑ = LOW-to-HIGH clock transition

NOTES

a. The HIGH-to-LOW transition of the S_0 and S_1 inputs on the 54/74194 should only take place while CP is HIGH for conventional operation

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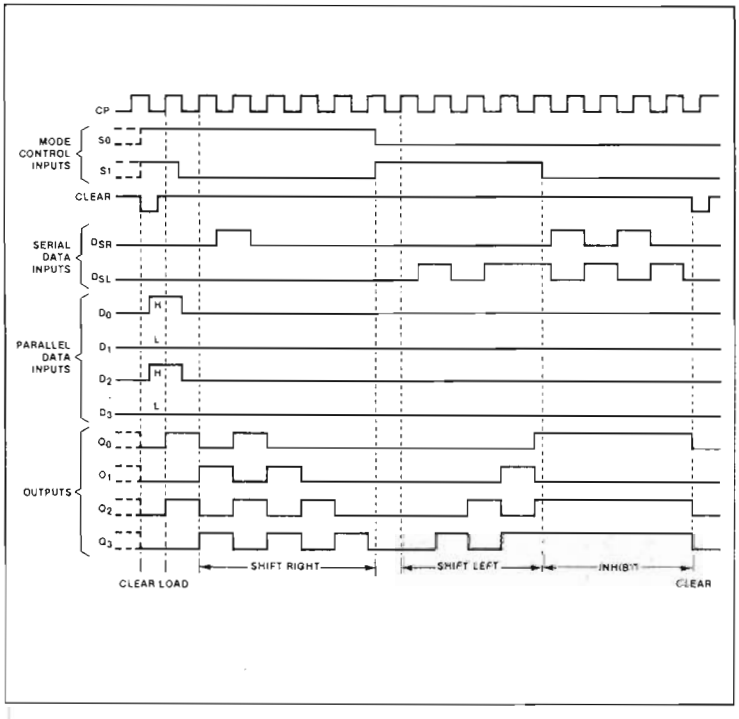
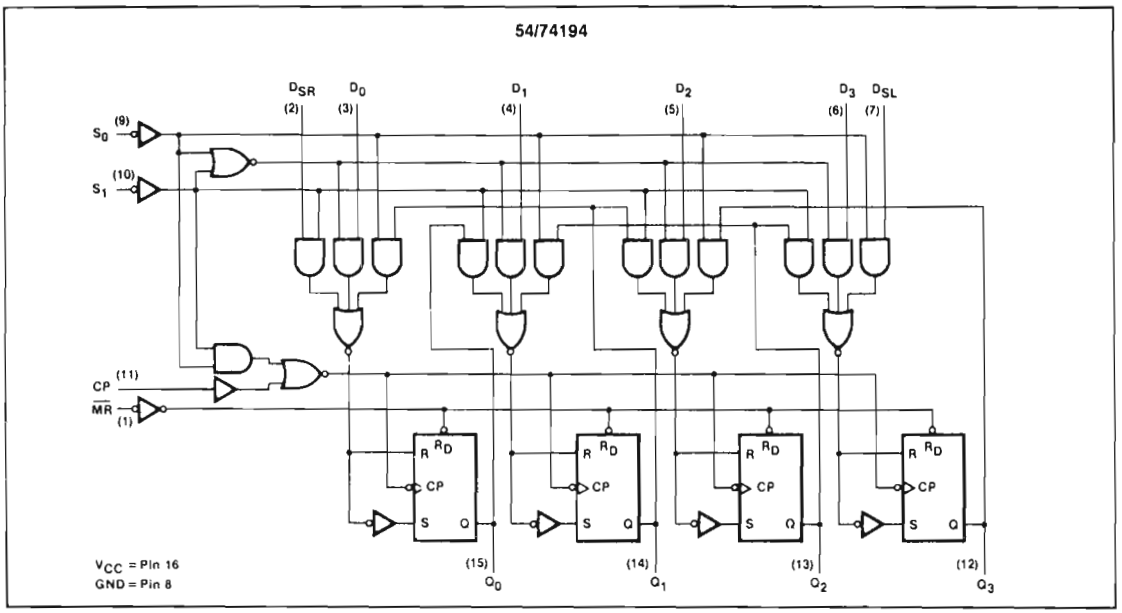
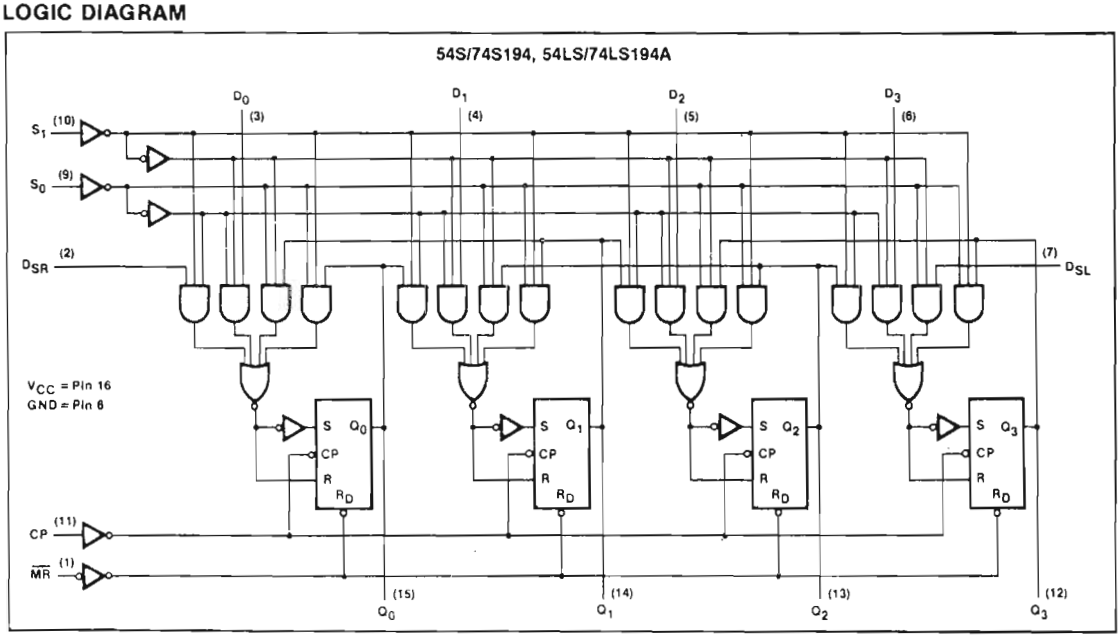
TYPICAL CLEAR, LOAD, RIGHT-SHIFT, LEFT-SHIFT, INHIBIT AND CLEAR SEQUENCES



LOGIC DIAGRAM



LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

	PARAMETER	54	54LS	54S	74	74LS	74S	UNIT
V_{CC}	Supply voltage	7.0	7.0	7.0	7.0	7.0	7.0	V
V_{IN}	Input voltage	−0.5 to +5.5	−0.5 to +7.0	−0.5 to +5.5	−0.5 to +5.5	−0.5 to +7.0	−0.5 to +5.5	V
I_{IN}	Input current	−30 to +5	−30 to +1	−30 to +5	−30 to +5	−30 to +1	−30 to +5	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +V_{CC}	−0.5 to +V_{CC}	−0.5 to +V_{CC}	−0.5 to +V_{CC}	−0.5 to +V_{CC}	−0.5 to +V_{CC}	V
T_A	Operating free-air temperature range	−55 to +125			0 to 70			°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER			54/74			54/74LS			54/74S			UNIT
			Min	Nom	Max	Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply voltage	Mil	4.5	5.0	5.5	4.5	5.0	5.5	4.5	5.0	5.5	V
		Com'l	4.75	5.0	5.25	4.75	5.0	5.25	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage		2.0			2.0			2.0			V
V_{IL}	LOW-level input voltage	Mil			+0.8			+0.7			+0.8	V
		Com'l			+0.8			+0.8			+0.8	V
I_{IK}	Input clamp current				−12			−18			−18	mA
I_{OH}	HIGH-level output current				−800			−400			−1000	μA
I_{OL}	LOW-level output current	Mil			16			4			20	mA
		Com'l			16			8			20	mA
T_A	Operating free-air temperature	Mil	−55		+125	−55		+125	−55		+125	°C
		Com'l	0		70	0		70	0		70	°C

NOTE
V_{IL} = +0.7V MAX for 54S at T_A = +125°C only.

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER		TEST CONDITIONS[1]			54/74194			54/74LS194A			54/74S194			UNIT
					Min	Typ[2]	Max	Min	Typ[2]	Max	Min	Typ[2]	Max	
V_{OH}	HIGH-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX, I_{OH} = MAX		Mil	2.4	3.4		2.5	3.5		2.5	3.4		V
				Com'l	2.4	3.4		2.7	3.5		2.7	3.4		V
V_{OL}	LOW-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX	I_{OL} = MAX	Mil		0.2	0.4		0.25	0.4			0.5[5]	V
				Com'l		0.2	0.4		0.35	0.5			0.5	V
			I_{OL} = 4mA	74LS					0.25	0.4				V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}					− 1.5			− 1.5			− 1.2	V
I_I	Input current at maximum input voltage	V_{CC} = MAX	V_I = 5.5V				1.0						1.0	mA
			V_I = 7.0V							0.1				mA
I_{IH}	HIGH-level input current	V_{CC} = MAX	V_I = 2.4V				40							μA
			V_I = 2.7V							20			50	μA
I_{IL}	LOW-level input current	V_{CC} = MAX	V_I = 0.4V				− 1.6			− 0.4				mA
			V_I = 0.5V										− 2.0	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX		Mil	− 20		− 57	− 20		− 100	− 40		− 100	mA
				Com'l	− 18		− 57	− 20		− 100	− 40		− 100	mA
I_{CC}	Supply current[4] (total)	V_{CC} = MAX				39	63		15	23		85	135	mA

NOTES

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. I_{OS} is tested with V_{OUT} = + 0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
4. With all outputs open, D_I inputs grounded and 4.5V applied to S_0, S_1, $\overline{MR}$ and the serial inputs, I_{CC} is tested with a momentary ground, then 4.5V applied to CP
5. V_{OL} = + 0.45V MAX for 54S at T_A = + 125°C only.

AC CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

PARAMETER		TEST CONDITIONS	54/74 C_L = 15pF, R_L = 400Ω		54LS/74LS C_L = 15pF, R_L = 2kΩ		54S/74S C_L = 15pF, R_L = 280Ω		UNIT
			Min	Max	Min	Max	Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1	25		25		70		MHz
t_{PLH} t_{PHL}	Propagation delay Clock to output	Waveform 1		22 26		22 26	4.0 4.0	12 16.5	ns
t_{PHL}	Propagation delay $\overline{MR}$ to output	Waveform 2		37		30		18.5	ns

NOTE

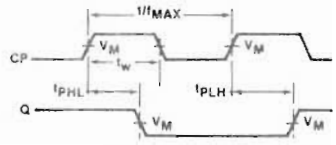
Per industry convention, f_{MAX} is the worst case value of the maximum device operating frequency with no constraints on t_r, t_f, pulse width or duty cycle.

AC SETUP REQUIREMENTS T_A = 25°C, V_{CC} = 5.0V

PARAMETER		TEST CONDITIONS	54/74		54LS/74LS		54S/74S		UNIT
			Min	Max	Min	Max	Min	Max	
t_W(H)	Clock pulse width, HIGH	Waveform 1	20		20		7		ns
t_W(L)	$\overline{MR}$ pulse width, LOW	Waveform 2	20		20		12		ns
t_s	Setup time, Data to Clock	Waveform 3	20		20		5.0		ns
t_h	Hold time, Data to Clock	Waveform 3	0		0		3.0		ns
t_s(L)	Setup time LOW, S_n to CP[a]	Waveform 4	30		30		11		ns
t_s(H)	Setup time HIGH, S_N to CP	Waveform 4	30		30		11		ns
t_h	Hold time, S_n to CP	Waveform 4	0		0		3.0		ns
t_{rec}	Recovery time, $\overline{MR}$ to CP	Waveform 2	25		25		9.0		ns

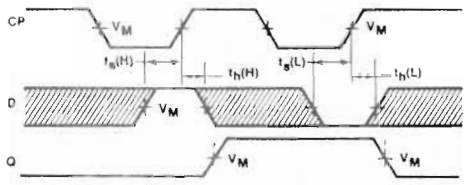
AC WAVEFORMS

CLOCK TO OUTPUT DELAYS AND CLOCK PULSE WIDTH



Waveform 1

DATA SET-UP AND HOLD TIMES

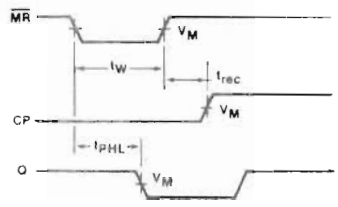


Waveform 3

V_M = 1.5V for 54S/74S; V_M = 1.3V for 54LS/74LS

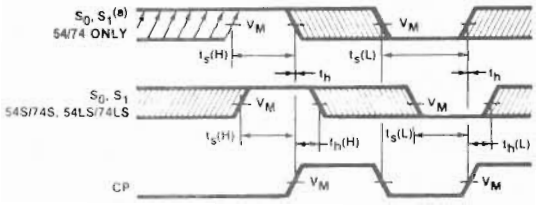
The shaded areas indicate when the input is permitted to change predictable output performance

MASTER RESET PULSE WIDTH, MASTER RESET TO OUTPUT DELAY & MASTER RESET TO CLOCK RECOVERY TIME



Waveform 2

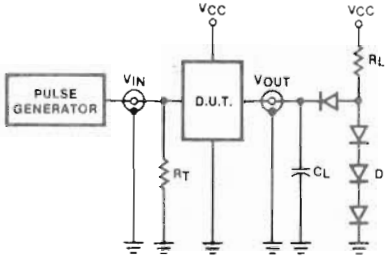
SETUP AND HOLD TIMES FOR S_0 AND S_1 INPUTS



Waveform 4

TEST CIRCUITS AND WAVEFORMS

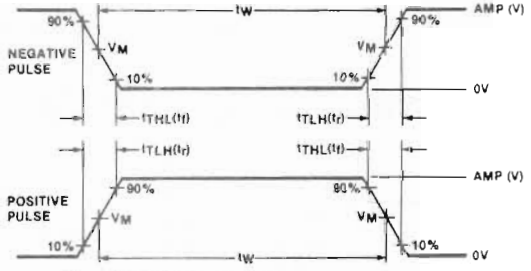
TEST CIRCUIT FOR 54/74 TOTEM-POLE OUTPUTS



DEFINITIONS

R_L = Load resistor to V_{CC}; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
D = Diodes are 1N916, 1N3064, or equivalent.
t_{TLH}, t_{THL} Values should be less than or equal to the table entries.

INPUT PULSE DEFINITIONS



V_M = 1.3V for 54LS/74LS; V_M = 1.5V for all other TTL families.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54/74	3.0V	1MHz	500ns	7ns	7ns
54LS/74LS	3.0V	1MHz	500ns	15ns	6ns
54S/74S	3.0V	1MHz	500ns	2.5ns	2.5ns