

M74ALS175P

6249827 MITSUBISHI (DCTL LOGIC)

91D 12439 D

QUADRUPLE D-TYPE FLIP FLOP WITH RESET

T-46-07-05

DESCRIPTION

The M74ALS175P is a semiconductor integrated circuit consisting of four D-type positive edge-triggered flip-flop circuits with common clock input T and direct reset input $\overline{R_D}$ and discrete data inputs D.

FEATURES

- Positive edge-triggering
- Clock and direct reset inputs common to all four circuits
- Q and $\overline{Q}$ outputs
- Wide operating temperature range ($T_a = -20 \sim +75^\circ\text{C}$)

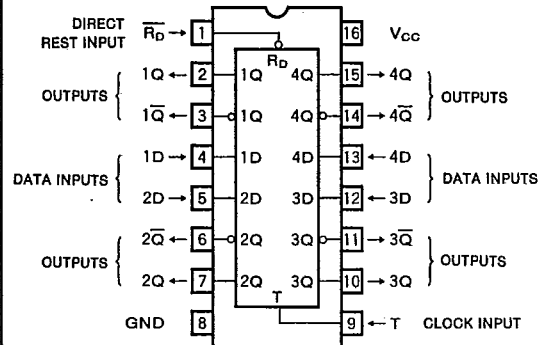
APPLICATION

General purpose, for use in industrial and consumer equipment.

FUNCTIONAL DESCRIPTION

When T changes from low-level to high-level, the D signal just before the change appears in the output Q and $\overline{Q}$ in accordance with the function table. When $\overline{R_D}$ is low-level, all Q and $\overline{Q}$ outputs are set low, and high respectively, irrespective of the other inputs. When use as a D-type flip-flop, $\overline{R_D}$ should be maintained in high-level.

PIN CONFIGURATION (TOP VIEW)



Outline 16P4

FUNCTION TABLE (Note 1)

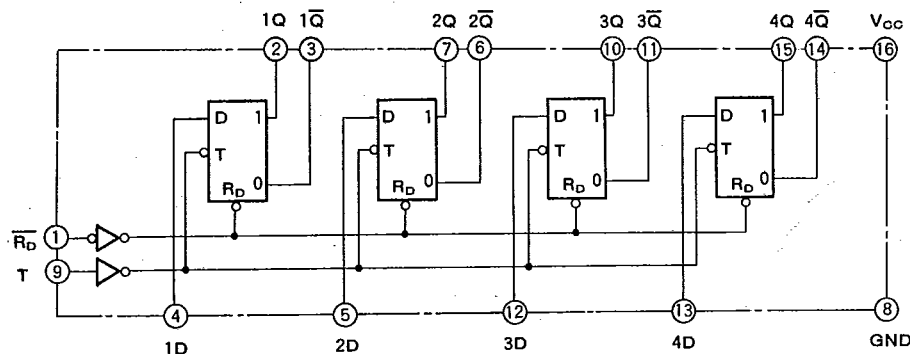
Inputs			Outputs	
$\overline{R_D}$	T	D	Q	$\overline{Q}$
L	X	X	L	H
H	↑	H	H	L
H	↑	L	L	H
H	L	X	Q^0	$\overline{Q}^0$

Note 1. X : Irrelevant

↑ : Transition from low to high level (positive edge trigger)

Q^0 : Level of Q before the indicated steady-state input conditions were established.

LOGIC DIAGRAM



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ABSOLUTE MAXIMUM RATINGS ($T_A = -20 \sim +75^\circ\text{C}$, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		$-0.5 \sim +7$	V
V_I	Input voltage		$-0.5 \sim +7$	V
V_O	Output voltage	High-level state	$-0.5 \sim V_{CC}$	V
T_{opr}	Operating free-air ambient temperature range		$-20 \sim +75$	$^\circ\text{C}$
T_{stg}	Storage temperature range		$-65 \sim +150$	$^\circ\text{C}$

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Limits			Unit
		Min	Typ	Max	
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8	V
I_{OH}	High-level output current	0		-0.4	mA
I_{OL}	Low-level output current	0		8	mA
T_{opr}	Operating free-air ambient temperature range	-20		+75	$^\circ\text{C}$

ELECTRICAL CHARACTERISTICS ($T_A = -20 \sim +75^\circ\text{C}$, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ *	Max	
V_{IC}	Input clamp voltage	$V_{CC}=4.5\text{V}$, $I_{IC}=-18\text{mA}$			-1.2	V
V_{OH}	High-level output voltage	$V_{CC}=4.5 \sim 5.5\text{V}$, $I_{OH}=-0.4\text{mA}$	$V_{CC}-2$			V
V_{OL}	Low-level output voltage	$V_{CC}=4.5\text{V}$, $I_{OL}=4\text{mA}$		0.25	0.4	V
		$I_{OL}=8\text{mA}$		0.35	0.5	
I_I	Input current with maximum voltage	$V_{CC}=5.5\text{V}$, $V_I=7\text{V}$			0.1	mA
I_{IH}	High-level input current	$V_{CC}=5.5\text{V}$, $V_I=2.7\text{V}$			20	μA
I_{IL}	Low-level input current	$V_{CC}=5.5\text{V}$, $V_I=0.4\text{V}$			-0.1	mA
I_O	Output current	$V_{CC}=5.5\text{V}$, $V_O=2.25\text{V}$	-30		-112	mA
I_{CC}	Supply current	$V_{CC}=5.5\text{V}$ (Note 2)		9	14	mA

* : All typical values are at $V_{CC}=5\text{V}$, $T_A=25^\circ\text{C}$.

Note 2. The supply current is measured at $D=\overline{R_D}=0\text{V}$, $T=4.5\text{V}$.

SWITCHING CHARACTERISTICS

Symbol	Parameter	Test conditions/Limits (Note 3)									Unit	
				$V_{CC}=4.5\sim 5.5V$								
				$C_L=50pF$								
				$R_L=500\Omega$								
				$T_A=25^{\circ}C$				$T_A=0\sim 70^{\circ}C$		$T_A=-20\sim +75^{\circ}C$		
		Input	Outputs	Typ	Min	Typ *	Max	Min	Typ *	Max		
f_{max}	Maximum clock frequency	T	$Q, \overline{Q}$		50	65		45	65		MHz	
t_{PLH}	Propagation time	$\overline{R_D}$	$\overline{Q}$	8	5	10	18	5	10	19	ns	
t_{PHL}			Q	13	8	15	23	8	15	24		
t_{PLH}		T	$Q, \overline{Q}$	6.5	3	9	15	3	9	16	ns	
t_{PHL}			$Q, \overline{Q}$	12	5	14	19	5	14	20		

* : All typical values are at $V_{CC}=5\text{V}$, $T_A=25^\circ\text{C}$.

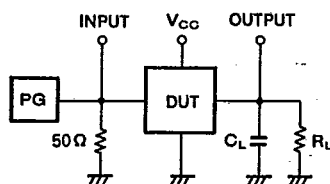
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91D 12441 D

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Note 3. Measurement circuit



(1) The pulse generator (PG) has the following characteristics:

$$PRR \leq 1\text{MHz}$$

$$t_r = 2\text{ns}, t_f = 2\text{ns}$$

$$V_{IH} = 3.5\text{V}, V_{IL} = 0.3\text{V}$$

$$\text{duty cycle} = 50\%$$

$$Z_o = 50\Omega$$

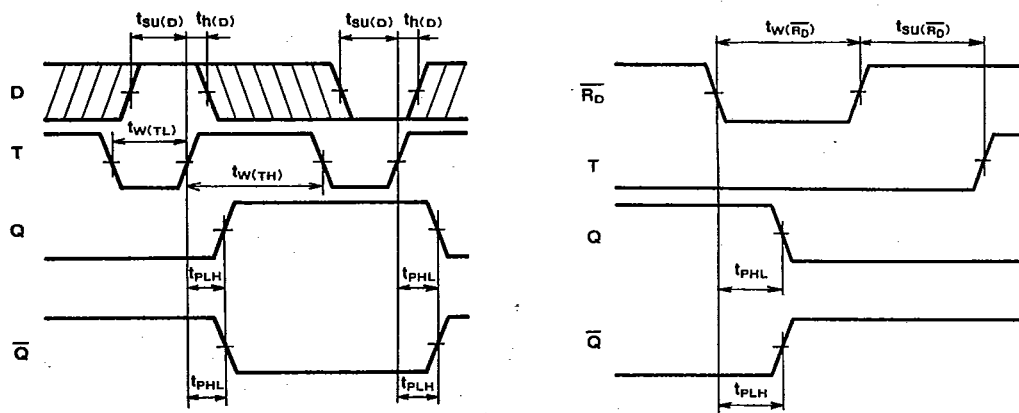
(2) C_L includes probe and jig capacitance.

TIMING REQUIREMENTS ($V_{CC} = 4.5 \sim 5.5\text{V}$, $C_L = 50\text{pF}$, $R_L = 500\Omega$)

Symbol	Parameter		Limits						Unit
			T _a =0~70℃			T _a =-20~+75℃			
			Min	Typ *	Max	Min	Typ *	Max	
t _{W(TH)}	Pulse width	T "H"	10	4		11	4		ns
t _{W(TL)}		T "L"	10	6		11	6		
t _{W(R_D)}		R _D "L"	10	5		11	5		
t _{su(D)}	Setup time before T↑	1D~4D	10	5		11	5		ns
t _{su(R_D)}		R _D "H" (Inactive)	6	3		7	3		
t _{h(D)}	Hold time after T↑	1D~4D	0	-3		1	-3		ns

* : All typical values are at $V_{CC} = 5\text{V}$, $T_a = 25^\circ\text{C}$

† : Transition from low to high.

TIMING DIAGRAM (Reference level = 1.3V)


Note 4. The shaded areas indicate the period when the input is permitted to change for predictable output performance.

PACKAGE OUTLINES

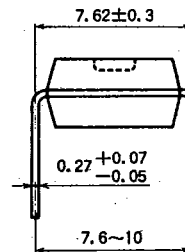
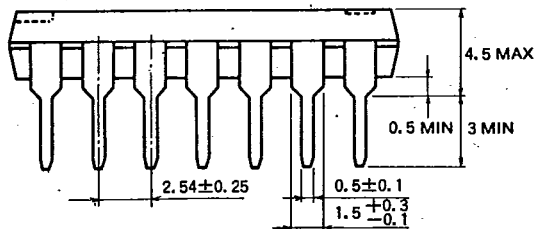
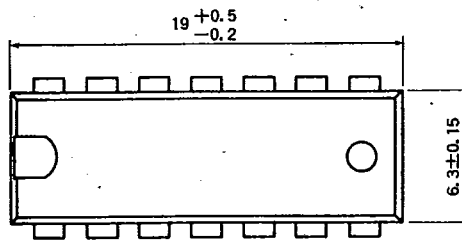
MITSUBISHI {DGTL LOGIC}

91D 12323

D T-9020

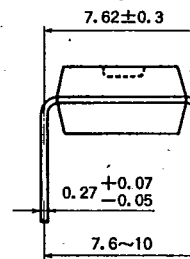
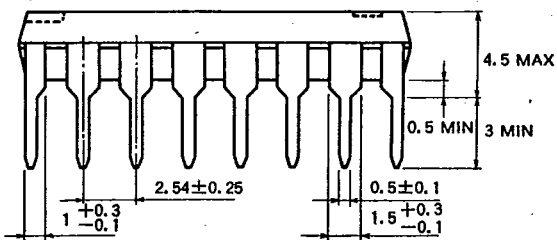
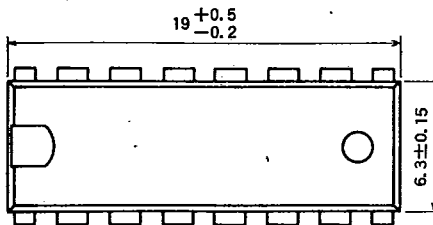
TYPE 14P4 14-PIN MOLDED PLASTIC DIP

Dimension in mm



TYPE 16P4 16-PIN MOLDED PLASTIC DIP

Dimension in mm



PACKAGE OUTLINES

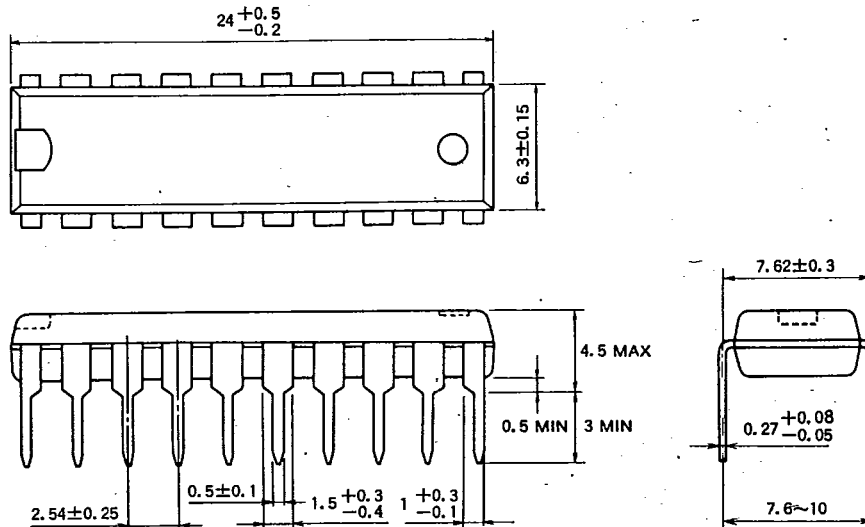
91D 12324

D *T-90-20*

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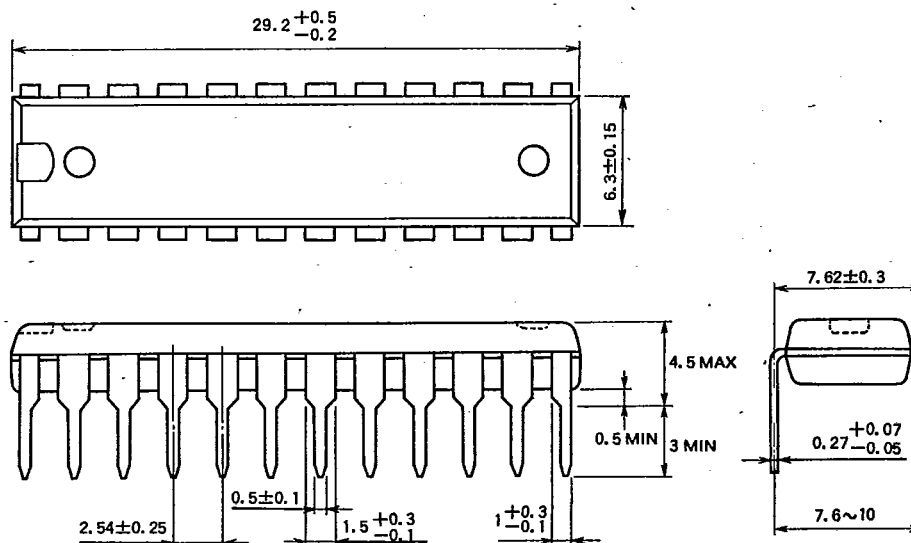
TYPE 20P4 20-PIN MOLDED PLASTIC DIP

Dimension in mm



TYPE 24P4D 24-PIN MOLDED PLASTIC DIP

Dimension in mm



TYPE DESIGNATION TABLE

MITSUBISHI (DGTL LOGIC)

91D D

6249827 0012784 7

T-90-20

ALSTTL SERIES SOP TYPE DESIGNATION TABLE

Type		Circuit function	Package Outlines
M74ALS00ADP	*	Quadruple 2-Input Positive NAND Gate	14P2P
M74ALS02DP	*	Quadruple 2-Input Positive NOR Gate	14P2P
M74ALS04ADP	*	Hex Inverter	14P2P
M74ALS05ADP	**	Hex Inverter with Open Collector Output	14P2P
M74ALS08DP	*	Quadruple 2-Input Positive AND Gate	14P2P
M74ALS09DP	**	Quadruple 2-Input Positive AND Gate with Open Collector Output	14P2P
M74ALS10ADP	*	Triple 3-Input Positive NAND Gate	14P2P
M74ALS11ADP	*	Triple 3-Input Positive AND Gate	14P2P
M74ALS20ADP	**	Dual 4-Input Positive NAND Gate	14P2P
M74ALS27DP	**	Triple 3-Input Positive NOR Gate	14P2P
M74ALS30ADP	**	Single 8-Input Positive NAND Gate	14P2P
M74ALS32DP	*	Quadruple 2-Input Positive OR Gate	14P2P
M74ALS37ADP	**	Quadruple 2-Input Positive NAND Buffer	14P2P
M74ALS38ADP	**	Quadruple 2-Input Positive NAND Buffer with Open Collector Output	14P2P
M74ALS74ADP	*	Dual D-Type Positive Edge-Triggered Flip-Flop with Set and Reset	14P2P
M74ALS109ADP	**	Dual J-K Positive Edge-Triggered Flip-Flop with Set and Reset	16P2P
M74ALS112ADP	*	Dual J-K Negative Edge-Triggered Flip-Flop with Set and Reset	16P2P
M74ALS131DP	**	3-Line to 8-Line Decoder/Demultiplexer with Address Register	16P2P
M74ALS138DP	*	3-Line to 8-Line Decoder/Demultiplexer	16P2P
M74ALS153DP	**	Dual 4-Line to 1-Line Data Selector/Multiplexer with Strobe	16P2P
M74ALS157DP	*	Quadruple 2-Line to 1-Line Data Selector/Multiplexer	16P2P
M74ALS161BDP	**	Synchronous Presettable 4-Bit Binary Counter with Direct Reset	16P2P
M74ALS163BDP	**	Fully Synchronous Presettable 4-Bit Binary Counter	16P2P
M74ALS169BDP	**	Synchronous 4-Bit Binary Counter	16P2P
M74ALS174DP	*	Hex D-Type Positive Edge-Triggered Flip-Flop with Reset	16P2P
M74ALS175DP	**	Quadruple D-Type Positive Edge-Triggered Flip-Flop with Reset	16P2P
M74ALS193DP	**	Synchronous Presettable Up/Down 4-Bit Binary Counter	16P2P
M74ALS240ADWP	*	Octal Buffer/Line Driver with 3-State Output (Inverted)	20P2V
M74ALS244ADWP	*	Octal Buffer/Line Driver with 3-State Output (Noninverted)	20P2V
M74ALS245ADWP	**	Octal Bus Transceiver with 3-State Output (Noninverted)	20P2V
M74ALS245A-1DWP	**	Octal Bus Transceiver with 3-State Output (Noninverted)	20P2V
M74ALS257DP	*	Quadruple 2-Line to 1-Line Data Selector/Multiplexer with 3-State Output	16P2P
M74ALS273DWP	**	Octal D-Type Positive Edge-Triggered Flip-Flop with Reset	20P2V
M74ALS299DWP	**	8-Bit Universal Shift/Storage Register with 3-State Output	20P2V
M74ALS373DWP	**	Octal D-Type Transparent Latch with 3-State Output	20P2V
M74ALS374DWP	**	Octal D-Type Positive Edge-Triggered Flip-Flop with 3-State Output	20P2V
M74ALS533DWP	**	Octal D-Type Transparent Latch with 3-State Output (Inverted)	20P2V
M74ALS534DWP	**	Octal D-Type Positive Edge-Triggered Flip-Flop with 3-State Output (Inverted)	20P2V
M74ALS561ADWP	**	Synchronous Presettable 4-Bit Binary Counter with 3-State Output	20P2V
M74ALS569ADWP	**	Synchronous Up/Down 4-Bit Binary Counter with 3-State Output	20P2V
M74ALS573ADWP	**	Octal D-Type Transparent Latch with 3-State Output (Noninverted)	20P2V
M74ALS574ADWP	**	Octal D-Type Positive Edge-Triggered Flip-Flop with 3-State Output (Noninverted)	20P2V
M74ALS640ADWP	**	Octal Bus Transceiver with 3-State Output (Inverted)	20P2V
M74ALS642ADWP	**	Octal Bus Transceiver with Open Collector Output (Inverted)	20P2V
M74ALS645ADWP	**	Octal Bus Transceiver with 3-State Output (Noninverted)	20P2V
M74ALS1034DP	**	Hex Noninverting Buffer	14P2P

*: New product **: Under development

6249827 MITSUBISHI (DGTL LOGIC)

91D 12785 D

MITSUBISHI ALSTTLs

DESCRIPTION

MITSUBISHI (DGTL LOGIC)

91D D

6249827 0012785 9 MIT3

T-90-20

DESCRIPTION

The ALSTTL SOP (Small Outline Package) devices are identical in all respects except for their package outlines to DIP (Dual Inline Package).

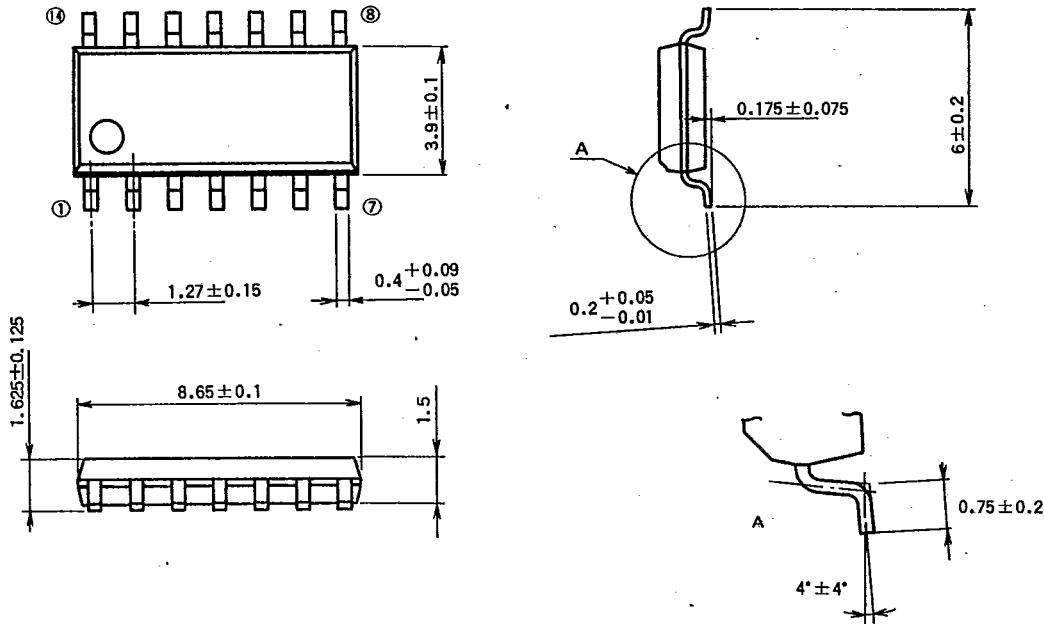
MITSUBISHI ALSTTLs
PACKAGE OUTLINES

MITSUBISHI (DGTL LOGIC) 91D D ■ 6249827 0012786 0 ■ MIT3

T-90-20

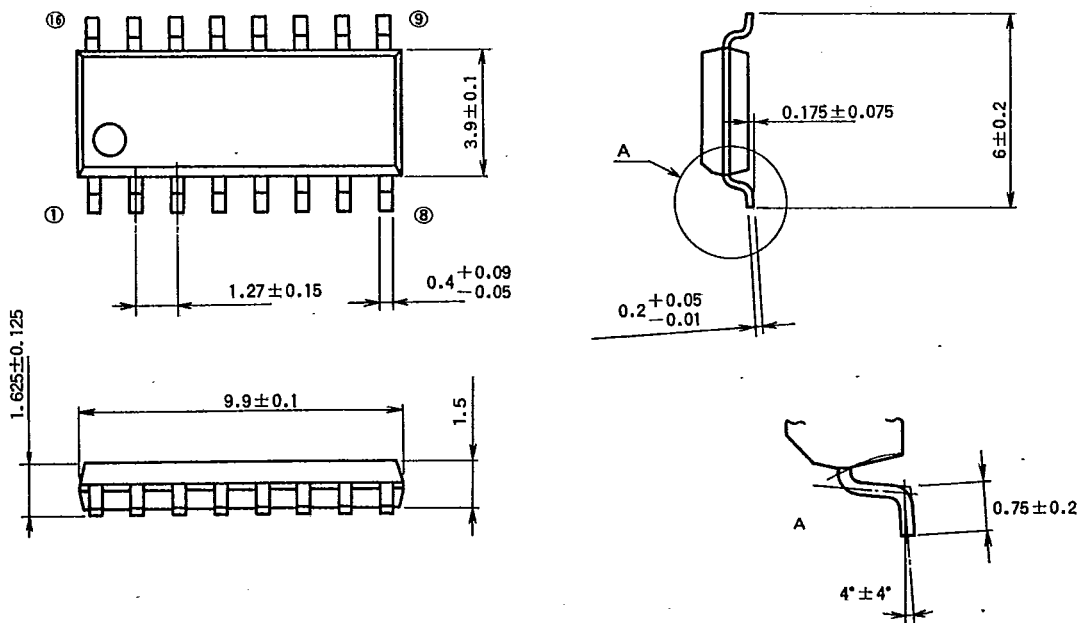
TYPE 14P2P 14-PIN MOLDED PLASTIC SOP (JEDEC 150mil body)

Dimension in mm



TYPE 16P2P 16-PIN MOLDED PLASTIC SOP (JEDEC 150mil body)

Dimension in mm



MITSUBISHI ALSTTLs
PACKAGE OUTLINES

MITSUBISHI (DGTL LOGIC)

91D D ■ 6249827 0012787 2 ■ MIT3

T-90-20

